TABLE OF CONTENTS

The Schottky Diode Mixer
Jack H. Lepoff, Hewlett-Packard (J-3) 53

Choosing the Right Crystal and Oscillator for the Application
Brian Rose, Q-Tech Corp. (C-1) 89

High Reliability Electromechanical Switching
J. Hoffman & H.C. Bell, Jr., Wavecom/Loral (O-4) 125

Microprocessor Control Considerations for
Modern RF Signal Generators
Ted J. Dudziak, Wavetek Indiana (K-3) 133

Everything You Wanted to Know About Tuning Diodes
John C. Howe, Motorola, Inc. (T-5) 139

Microware: An Interactive Microwave Filter Design Program
Michael K. Ferrand, Microlab/FXR (H-2) 151

A Practical Approach to the Design of
Voltage Tuneable Lowpass and Bandpass Filters
Bruce R. Long, ISC Defense Systems (H-2) 161

RF Design Evaluation Made Easier Through Automated Control
S.M. Mussman, Wavetek Indiana (K-3) 171

OOK, FSK and PSK Data Receivers Using an AM-FM Receiver IC
Jon Grosjean, Woodstock Engineering (Q-5) 181

A Thick Film Hybrid Transmitter for Cellular Telephone
Pekka Mikkola, Nokia-Mobira Oy (O-5) 187

DESIGN: A Program for the Automated Synthesis of Broadband
Matching Networks Between Complex Terminations
S.E. Sussman-Fort, Spefco Software (P-4) 193

Developing Non-Linear Oscillator Models Using Linear Design Tools
U.L. Rohde, Communications Consulting Corp. (P-4) 201

Logarithmic Amplifiers
Tom Munson, Plessey Semiconductors (A-1) 215

Linear FM Modulator
Jerry Iseli, Texas Instruments (D-1) 223

EW Applications of High Resolution Compressive Receivers
Merrill M. Apter, Andersen Laboratories, Inc. (R-5) 229

Digital-RF Interfacing — The Story of a Marriage
Robert W. Sproul, Lorch Electronics (K-3) 237

RF Bipolar Parameter Extraction for
Modeling Class C Amplifier Response
P. Sanders, A. Wood,
Motorola Semiconductor Product Sector (F-2) 243

How to Specify PIN Diode Switches
Raymond L. Sicotte, American Microwave Corp. (O-4) 253

A Low Noise Fiber Optics Receiver/Amplifier in VHF Range
Lajos Burgyan, Signetics Corp. (R-5) 267

A Thermally Tuned VCO
Albert Helfrick, Dowty RF Industries, Inc. (E-2) 275

Computer-Aided Design of a Bipolar Transistor Amplifier
Steven Hamilton, Judy Guild, Krin Henderson, EEsof (F-2) 279

Low-Noise Preamplifier Design for NMR
Otward Mueller, William A. Edelstein,
G.E. Corporate Research & Development (L-3) 291

A Complex Impedance Meter
Carl G. Lodstrom, Dow-Key Microwave (E-2) 297

Efficiency of Envelope-Tracking RF Power Amplifier Systems
Frederick H. Raab, Ph.D.,
Green Mountain Radio Research Co. (G-2) 303

Direct Single Sideband Modulation
of Transmitter Output Switcher Stages
F.G. Tinta, General Instrument (T-5) 313

PIN Diodes and the Theory of Microwave Operation
J.F. White, M/A-COM (O-4) 325

Design Considerations for the Development
of Internally Matched FETs
Mahesh Kumar, Bert. S. Hewitt,
Microwave Semiconductor Corp. (M-4) 351

Low Noise Oscillator Design
Art Upham, Hewlett-Packard (N-4) 359

Broadband GaAs Monolithic Amplifiers and Their Applications
Terence J. Cummings, California Eastern Labs (A-1) 379

A Solid State HF Transmitter for Over-The-Horizon (OTH) Radar
Fuat Agi, M/A-COM MPD, Donald J. Hoft, M/A-COM (B-1) 385

A HF High Dynamic Range Amplifier Using Feedforward Techniques
Jean Yamas, Locus, Inc. (B-1) 389

Coaxial Cable Leakage
Brian E. Shreve, Delta Electronics (Q-5) 399

Design and Analysis of Fourth and
Fifth Order Indirect Synthesizer Loops
James W. Maben, Sanders Assoc. (I-3) 407

Development of a C-Band Power Module
for the Morelos Mexican Satellite System
Arturo Velasquez, Arturo Serrano,
CICESE Research Center (B-1) 419

Phase Noise Intermodulation and Dynamic Range
Peter E. Chadwick, Plessey Semiconductors (R-5) 431

Advances in Single Chip Frequency Synthesizers
P.E. Chadwick, Plessey Semiconductors (I-3) 441

HF/VHF/UHF Power Static Induction Transistor Performance
R. Regan, S. Butler, E. Bulat, A. Varallo, M. Abdollahian, F. Rock,
GTE Labs, Inc. (G-2) 447

A High Performance SAW Filterbank Achieves 60 dB Rejection
C. Lanzl, W. Ossman, R. Bernardo,
Andersen Laboratories (D-1) 451

Bandpass and Bandstop Filter in the 100 to 1000 MHz Frequency
Range, or "The Search for Q"
R.V. Snyder, RS Microwave Co., Inc. (S-5) 463

A Phase Lock Loop That Works — Almost
Michael F. Black, Texas Instruments (I-3) 475

Construction Tips and Environment for Dielectric Resonator Circuits
Lynn Carpenter, Pennsylvania State University (C-1) 487

Non-Linearity Effects in RF Circuits
David Leiss, Lynn Olsen, Besser Associates, Inc. (F-2) 495

A Crystal Controlled Frequency & Amplitude Calibrator
Dan Baker, Tektronix (E-2) 505

General Price Determinants for RF & Microwave Filters
R.A. Wainwright, Cir-Q-Tel, Inc. (S-5) 509

A New Double-Balanced Mixer of
High Dynamic Range Improves System Performance
Aubrey Jaffer, Bertronics (J-3) 511

The Tactical Miniature Crystal Oscillator (TMXO)
T.S. Payne, R.E. Lowell, Piezo Technology (C-1) 517

Design Considerations for SAWR Oscillators
Katherine L. Feldmann, Watkins-Johnson (D-1) 531

Monolithic RF Amplifiers for Hybrid Applications
Jerry Schappacher, Harris Microwave (A-1) 543

The Schottky Diode Mixer

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INTRODUCTION

A major application of the Schottky diode is the production of the difference frequency when two frequencies are combined or mixed in the diode. This mixing action is the result of the non-linear relationship between current and voltage, usually expressed as

$$I = I_s\left(e^{\frac{q(V-IR_s)}{nkT}} - 1\right)$$

The series resistance, R_s, is a parasitic element representing bulk resistance of the semiconductor and contact resistance. It is sometimes confused with dynamic resistance which is the sum of the series resistance and the resistance of the junction where the frequency conversion takes place. The ideality factor, n, is unity for an ideal diode and less than 1.1 for a silicon Schottky diode.

Variations in n are not important for n less than 1.1. The effect of saturation current, Is, is very important when the level of local oscillator power is low. This will be demonstrated by comparing results of mixing with diodes having different values of saturation current. Although temperature, T, is seen in the exponential and is present in a more complicated manner in saturation current, the effect on mixing efficiency is less than 0.5 dB for 100 degrees C change in temperature. Electron charge, q, and Boltzmann constant, k, may be combined in the equation

$$I = I_s\left(e^{\frac{V-IR}{.026}} - 1\right) \qquad (1)$$

Conversion Loss

Mixing efficiency is measured by the conversion loss, the ratio of signal input power to intermediate frequency output power. The intermediate frequency is the difference between the signal frequency and the local oscillator frequency. The diode may also generate the sum of these two frequencies. In this case the mixer may be called an upconverter. For a given local oscillator frequency, the difference frequency may be produced by two signal frequencies - one above the l.o. frequency and one below. Of course noise is also contributed at these two frequencies. In some cases, the mixer is designed to respond to both these frequencies. A mixer of this type is called a double sideband mixer. More commonly the mixer is designed to respond to one of these inputs. Since noise comes from botn frequencies the double sideband mixer is better - typically 3 dB better.

Noise figure is another measure of mixing efficiency. This is the ratio of signal to noise ratio at the input to signal to noise ratio at the output. Single and double sideband definitions apply to noise figure also. In some applications noise figure and conversion loss are essentially equal. However, noise figure includes diode noise which becomes significant at intermediate frequencies in the audio range (1/f noise). In these applications noise figure may be much larger than conversion loss.

Another complication of noise figure is the effect of the amplifier following the mixer. Diode manufacturers include the effect of a 1.5 dB noise figure IF amplifier in the mixer noise figure. Mixer manufacturers do not include this amplifier in the mixer noise definition. In this paper diode efficiency will be measured by conversion loss.

Parasitic Losses

The diode equivalent circuit of Figure 1 shows the presence of two elements that degrade performance by preventing the incoming signal from reaching the junction resistance where the mixing takes place. The effect of junction capacitance and series resistance was studied by comparing conversion loss data measured with three diodes covering a wide range of these parameters. The 5082-2800 is a general purpose diode, typically used in switching circuits. The 5082-2817 is a 2 GHz mixer diode. The 5082-2755 is a 10 GHz detector diode. Figure 2 shows the conversion loss measured at 2 GHz for these three diodes.

The 5082-2800 general purpose diode has a conversion loss several dB worse than that of the other diodes. This is expected because this diode has a higher junction capacitance. The behavior of the low capacitance 5082-2755 detector diode is more interesting. At local oscillator power levels below -3 dBm the conversion loss is better than the loss of the 5082-2817 mixer diode, but at higher power levels it is worse.

A good approximation to the effect of junction capacitance and series resistance on conversion loss is:

$$L_1 = 1 + \frac{R_s}{R_j} + \omega^2 C_j^2 R_s R_j \qquad (2)$$

This is the ratio of available power to the power delivered to the junction resistance, R_j, using the diode equivalent circuit of Figure 1. The value of junction capacitance varies with voltage as

$$C_j = \frac{C_o}{\sqrt{1 - \frac{V}{0.6}}} \qquad (3)$$

where 0.6 is a typical value of barrier voltage.

The relative values of conversion loss in Figure 2 may be explained by these equations. Zero bias capacitances for the three diodes were measured to be 0.84 pF, 1.29 pF, and 0.13 pF for the -2817, -2800, and -2755 diodes respectively.

At a local oscillator power level of 1 milliwatt the forward current is about 1 millliampere. Using the corresponding forward voltages, C_j is computed for the three diodes. Assuming a junction resistance of 150 ohms, reasonable values of series resistance may be chosen to make the relative values of L_1 correspond to the relative measured values.

The familiar junction resistance equation $R_j = \frac{26}{I}$ does not apply for I= rectified current. It refers to I= DC bias current. When

rectified current is 1 mA, instantaneous current varies over forward and reverse values. Junction resistance is very large when the current is negative so the average junction resistance is larger than predicted by this equation.

Diode	C (pF)	R (ohms)	L (dB)
2817	1.3	6	1.07
2800	2.2	16	4.68
2755	0.28	50	1.47

At -3 dBm the 2817 and 2755 curves cross, with the 2800 loss 4.5 dB higher. This relative loss can be explained by raising R to 235 ohms and decreasing the capacitance values.

Diode	C (pF)	L (dB)
2817	1.12	1.2
2800	2.1	5.7
2755	0.23	1.2

These values of C_j and R_s were chosen to illustrate the effect on conversion loss. Since saturation currents are different for these diodes and junction resistances may be different, the actual values of C_j and R_s may be somewhat different.

Equation 2 shows the loss behavior with frequency. At low frequencies the loss is independent of frequency and capacitance. Choosing a low value of series resistance provides the best diode. At high frequencies low capacitance becomes more important than low series resistance because capacitance is squared in the equation. Figure 3 shows L_1 vs frequency for the 5082-2835 diode with R_s = 6 ohms and C_j = 1.0 pF and for the HSCH-5310 diode with R_s = 17 ohms and C_j = 0.1 pF. The lower capacitance makes the -5310 the better diode at microwave frequencies while the lower resistance makes the -2835 the better diode at low frequencies.

The Effect of Barrier Voltage

The type of metal deposited on silicon to form a Schottky barrier influences the barrier voltage which is involved in the *saturation current* determining the forward current. We use the term low barrier for diodes with low values of voltage for a given current (usually 1 mA). We have previously shown the effect of barrier voltage on the variation of junction capacitance with forward voltage.

Figure 4 shows the measurement of conversion loss for three diodes having a range of barrier potential values.

Diodes	Barrier Potential
5082-2817	0.64
5082-2835	0.56
HSCH-3486	0.35

At low LO power levels the lower barrier diodes have better performance, significantly better for the lowest barrier diode, the HSCH-3486. At higher power levels this diode loses its advantage because of higher series resistance. The 5082-2835 has lower capacitance and lower series resistance so its performance is better than the 5082-2817 at all power levels. The maximum rated power level of 150 mW is not high enough to demonstrate the increase in conversion loss seen at high power levels for the other diodes.

Effects of DC Bias and Local Oscillator Power Level

Figure 5 shows the conversion loss of a 5082-2817 mixer diode measured at 2 GHz. The top curve was measured without DC bias. Optimum DC bias was applied at each level for the bottom curve. The curves meet at the optimum local oscillator level where bias does not help. Below this level forward bias is used. Above this level reverse bias is used to reduce the rectified current.

At low levels of LO power, the conversion loss degrades rapidly unless DC bias is used. At -10 dBm the degradation is about 7 dB from the performance at the standard 0 dBm power level. Replacing the lost LO power with DC bias recovers about 6 dB of the degradation.

At high levels of LO power the performance degrades again. This is caused by the rapid increase of junction capacitance. Reverse bias reduces the current and the capacitance, restoring the diode performance.

Effect of Load Resistance

Figure 6 shows the effect of mixer load resistance on conversion loss. At low local oscillator power levels the effect is similar to the barrier effect. More rectified current flows with smaller load resistance so performance is better. At higher power levels the degradation due to higher capacitance appears first with the lower load resistances. As a result the optimum value of load resistance increases with LO power level. At +9 dBm 100 ohms becomes better than 10 ohms. AT +19.5 dBm 400 ohms becomes better than 100 ohms. The load circuit can be designed to provide the optimum resistance as the local oscillator power level changes.

HARMONIC DISTORTION

Sums and differences of multiples of the two mixing frequencies are produced in the mixing diode. These frequencies appear as spurious responses in the output. This effect was studied by setting the signal frequency at 2 GHz and the power at -30 dBm. The local oscillator was then set at various frequencies to produce harmonic mixing with a difference frequency of 30 MHz. Local oscillator power was one milliwatt. Then the local oscillator was set at 2 GHz and the signal frequency varied. The output levels in dB below fundamental mixing are shown in Figure 7. The diode was placed in a 50 ohm untuned coaxial mount.

The output levels of the mi products, mixing of the signal fundamental with multiples of the local oscillator, are much higher than

the in products, mixing of the local oscillator fundamental with multiples of the signal. For example, the 2x1 output is 5 dB below fundamental. Figure 5 shows that this level of fundamental mixing corresponds to a local oscillator level of -8 dBm. The doubling efficiency was about 8 dB. The 1x2 output is 16 dB below fundamental mixing. This corresponds to a signal level of -46 dBm. The doubling efficiency is 16 dB for the lower level signal frequency. Although fundamental mixing in Figure 5 was measured in a tuned system and the data of Figure 7 was measured in an untuned system, this analysis nevertheless gives a comparison of multiplying at the one milliwatt and one microwatt power levels. Mixing of signal multiples above 2 with local oscillator multiples above the fundamental produced outputs below the -100 dBm sensitivity of the receiver.

Harmonic Mixing

While harmonic products are usually considered spurious, in some designs the desired output is the result of harmonic mixing. This is a valuable mixer technique when the frequency is so high that it is difficult to generate the local oscillator power. Hewlett-Packard Application Note 991, "Harmonic Mixing With the HSCH-5500 Series Dual Diode" describes a technique using the 2nd harmonic of the local oscillator with little loss of efficiency compared to fundamental mixing. Mixers using the 6th, 8th, and 10th harmonics are used to extend the range of Hewlett-Packard spectrum analyzers to 60 GHz.

Two Tone Distortion

Harmonic distortion may be suppressed by a band pass filter at the mixer input. When the distortion is caused by

$$m f_{LO} - n f_s = f_{if}$$

the unwanted frequency is

$$f_s = \frac{m}{n} f_{LO} - \frac{f_{if}}{n} \qquad (4)$$

The narrowest filter required corresponds to $m = n = 2$ with a rejection bandwith equal to the intermediate frequency.

Two tone distortion is the result of two unwanted signals mixing with each other and the local oscillator to produce an intermediate frequency output. The equation is

$$f_{LO} - mf_1 + nf_2 = f_{if} \qquad (5)$$

Third order two tone intermod may correspond to $m = 2$, $n = 1$. In this case the correct intermediate frequency is produced when the desired signal f_s equals $2f_1 - f_2$. The unwanted frequencies may be arbitrarily close to the desired frequency so the problem cannot be solved with a filter.

Third order two tone distortion in a 5082-2817 diode was investigated with a local oscillator frequency of 1.94 GHz and input

frequencies of 2 GHz and 1.985 GHz. The intermediate frequency was 2 x 1.985 - 2 - 1.94 = 0.03 GHz. The measure of distortion is the input intercept point, the power level where the line of output vs input power for the desired mixing intersects the extension of the spurious line. This is shown in Figure 8. Since the desired output is linear, the suppression of the spurious output is 2A and input intercept is input power plus half the suppression.

With the help of this relationship the intercept point was measured as a function of local oscillator power level. The results are shown in Figure 9. At higher local oscillator power levels the desired output increases while the spurious output decreases. This raises the suppression and the intercept point. At lower levels both desired output and spurious decrease so the intercept point levels off to a constant value.

Tuning for Better Sensitivity

The ideal mixer should convert all of the signal power to output power at the desired output frequency. However, it is customary to test diodes in a broadband mixer circuit. In this test no attempt is made to recover the power lost in the unwanted output frequencies. Because of these losses and the losses in the diode parasitics, an efficiency of about 35% is usually achieved.

Special circuits have been developed to improve this figure to come closer to the ideal 100% efficiency. The most serious spurious response, called the image response, produces an output at the frequency $2f_{LO} - f_s$. Image recovery mixers are designed to recover this lost power. Two dB improvement has been reported. By properly terminating harmonics up to the third, conversion loss under 2 dB was obtained with a Hewlett-Packard beam lead diode.

MULTIPLE DIODE MIXERS

Although the intermediate frequency may be produced by mixing in a single diode, very few mixers are made this way. The problems generated by using a single diode include radiation of local oscillator power from the input port, loss of sensitivity by absorption of input power in the local oscillator circuit, loss of input power in the intermediate frequency amplifier, and the generation of spurious output frequencies by harmonic mixing. Some of these problems may be solved by circuit techniques but these circuits often introduce new problems. Most mixers use multiple diode techniques to better solve these problems.

Early mixer designs prevented loss of signal power in the local oscillator circuit by loosely coupling the local oscillator power to the mixer diode. This technique is wasteful of local oscillator power and it sends as much power to the input, possibly an antenna, as it sends to the diode. This local oscillator radiation could be interpreted as a target return when received by a radar. This problem may be alleviated by using

a directional coupler to send the local oscillator power to the mixer diode. Coupling must be loose so that LO power is still wasted.

A balanced mixer (Figure 10) provides a better solution. The hybrid circuit splits the LO power to the two diodes with little coupling to the antenna. A low pass filter is needed to prevent loss of power to the intermediate frequency amplifier. Additional advantages are reduction of LO noise and harmonic mixing. LO noise is rejected because two signals originating in the same port produce IF outputs that cancel. This is a property of the hybrid circuit. Similarly, even order harmonics of either the LO or the signal produce cancelling outputs.

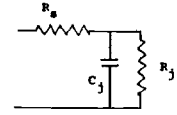
In the double balanced mixer (Figure 11) even order harmonics of both the LO and the signal frequency are rejected. This mixer does not require a low pass filter to isolate the IF circuit. The three ports are isolated from each other by the symmetry of the circuit. These mixers usually cover a broader band than the others. Ratios as high as 1000:1 are available. Microwave equivalents of these mixer circuits are available. Bandwidth ratios as high as 40:1 are available at microwave frequencies.

Intermodulation distortion is reduced when local oscillator power is increased. Several design techniques are used to allow higher drive.

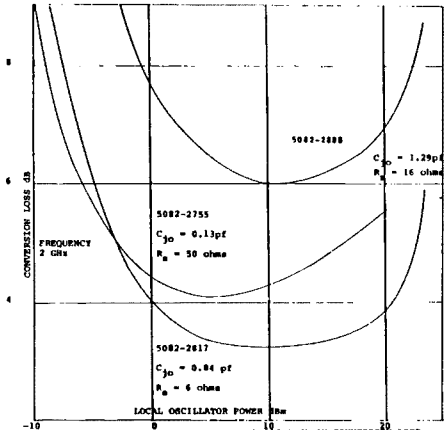
A higher barrier diode may be used to retain linear response at higher drive levels. More than one diode may be used in each arm of the ring in a double balanced mixer. This permits higher drive level without overheating the diodes. Two rings may also be used to increase the local oscillator level. This technique is also used for image tuning described earlier.

Summary:

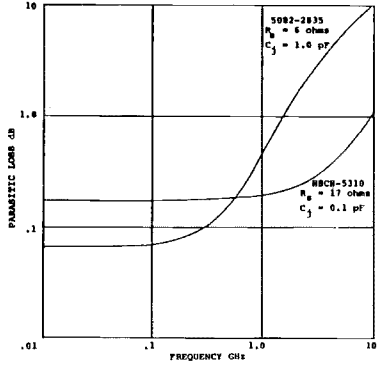
Schottky diode mixing efficiency is related to both diode parameters and circuit parameters. Diode parameters studied include capacitance, resistance, and barrier voltage. Circuit parameters include DC bias and load resistance. Harmonic response and third order two tone intermodulation were also studied.



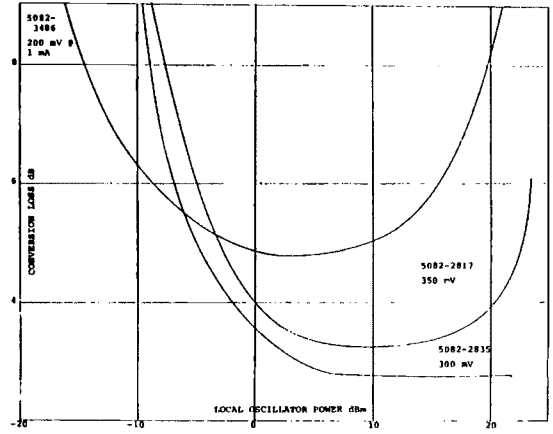
EQUIVALENT CIRCUIT
FIGURE 1



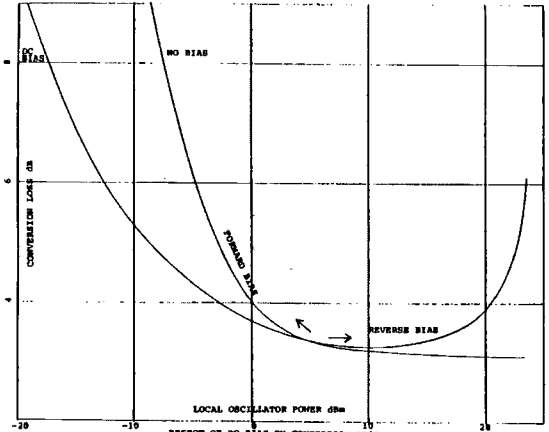
EFFECT OF CAPACITANCE AND SERIES RESISTANCE ON CONVERSION LOSS
FIGURE 2



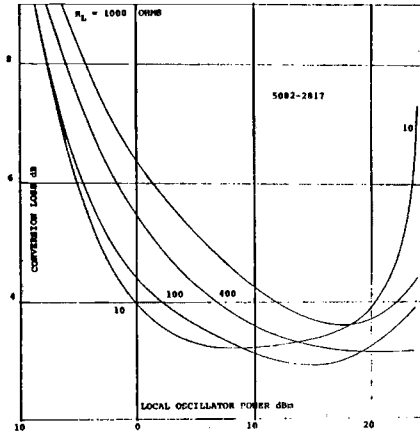
PARASITIC LOSS
FIGURE 3



EFFECT OF BARRIER
ON CONVERSION LOSS
FIGURE 4



EFFECT OF DC BIAS ON CONVERSION LOSS
FIGURE 5



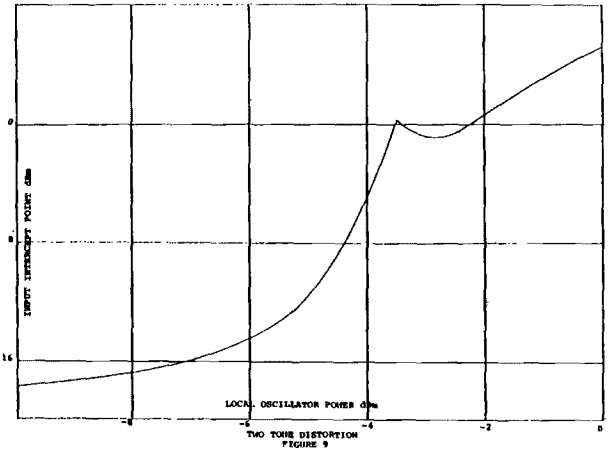
EFFECT OF LOAD RESISTANCE ON CONVERSION LOSS
FIGURE 6

SIGNAL				
4	43	42	X	X
3	21	56	X	X
2	16	45	38	39
1	0	5	13	19
	1	2	3	4

LOCAL OSCILLATOR

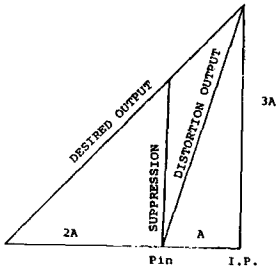
HARMONIC DISTORTION

FIGURE 7



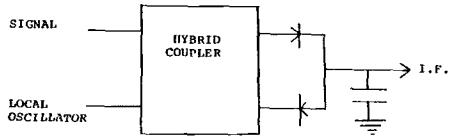
TWO TONE DISTORTION

FIGURE 9



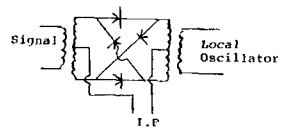
INTERCEPT POINT

FIGURE 8



BALANCED MIXER

FIGURE 10



DOUBLE BALANCED MIXER

FIGURE 11

CHOOSING THE RIGHT CRYSTAL AND OSCILLATOR FOR THE APPLICATION

by

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Some of the considerations which go into a decision on the choice and design of crystals and crystal oscillators are listed below:

1. Fundamental versus overtone mode crystal.
2. Parallel mode versus series mode.
3. VHF crystal versus multiplier chain.
4. Uncompensated versus TCXO or OCXO.
5. Trimable versus no trim adjustment.
6. Solder sealed package versus hybrid.
7. Voltage control required.
8. Stringent short term stability requirements.
9. Tight ageing requirements.
10. Start-up time.
11. Radiation requirements.
12. Shock and vibration rquirements.
13. Low current (battery operated).
14. Low parts count. Gate Oscillator.

In order to organize some of the above considerations, this paper arbitrarily begins with a 20 MHz , fundamental mode crystal in an HC-18 holder, to be used in an oscillator driving a receiver local oscillator chain to 400 MHz.
The characteristics of this crystal and its circuit are described and some of the options and considerations of the list are compared to this 20 MHz example.

FREQUENCY STABILITY

Assume that the oscillator has a temperature stability of $\pm$40 PPM (parts per million) over the temperature range of -40°C to +85°C. To this must be added an ageing factor. One can conservatively assume 2 PPM ageing the 1st year of operation and a life time ageing factor of 4PPM. Using these assumptions, the worst case frequency error will be 40 + 4 or 44 PPM.

In Hertz;

$$20 * 10^{6} * 44 * 10^{-6} = 880 \text{ Hz},$$

and at the end of the x20 multiplier chain

$$20 \times 880 = 17{,}600 \text{ Hz}.$$

This frequency error would be tolerable if this fictitious local oscillator was part of a receiver with a 200 kHz I.F. bandwidth. If, however, the bandwidth were only 2 kHz,a 17600 Hz error in the local oscillator would be excessive. The narrow band assumption will be made in order to see where it leads the

oscillator design. The maximum error must now be restricted to about 200 Hz, or

Df, PPM = 200/400 = 0.5 PPM

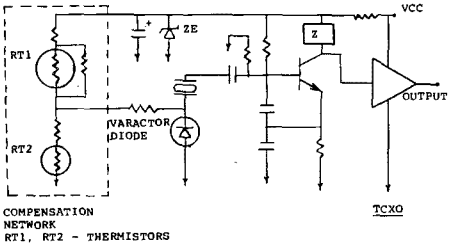
This new requirement forces the design to either a much more stable crystal oscillator, or to a system in which the oscillator is locked to a stable master reference. These two approaches will be considered next.

TCXO's and OCXO's

(Temperature Compensated Crystal Oscillator and Oven Controlled Crystal Oscillators)

Before considering the two options of TCXO and OCXO, the questions of ageing and setability must be addressed. If the receiver must operate without adjustment throughout its life, then ageing will probably determine the quality of crystal oscillator required (and therefore the price, size and D.C. power). If the frequency of the oscillator can be corrected by electrical or mechanical adjustment to remove frequency error due to ageing, the frequency accuracy *will be dominated by temperature* rather than age. TCXO's and OCXO's will be considered with this assumption.

Briefly, a TCXO corrects the crystal frequency versus temperature characteristic by means of a compensation network which applies a correction voltage to a varicap diode in series with the crystal. An OCXO addresses the problem by controlling the temperature of the crystal with a miniature oven. Simplified schematics of a typical TCXO and OCXO are shown in Figure 1.



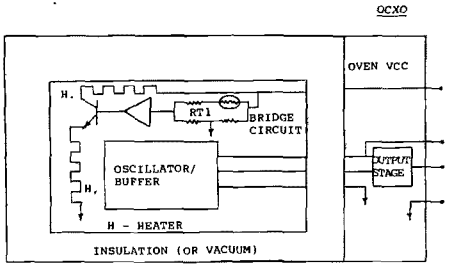


Figure 1, Simplified TCXO and OCXO

The new specification of .5 PPM puts the requirement somewhere in the gray area between TCXO's and OCXO's. Low cost, commercial TCXO's typically meet ±1 PPM over 0°C to 50°C. The example oscillator's specification and temperature range puts the design near the border of the best that can be done with a TCXO, and consequently it would be a costly unit. OCXO's easily provide stabilities of $\pm 1 \times 10^{-8}$ over the required temperature range, and provide ageing rates less than 1×10^{-9} per day.

However, ovenized units are larger, heavier, and consume much more power than non-oven types. Representative specifications are shown in Table 1. Notice that some compromises may have to be made between requirements, performance, and price.

PHASE LOCKED SYSTEM

As an alternative, assume that this system already contains a stable master oscillator at 5 MHz. The basic crystal oscillator can then be locked to this master using a phase locked loop. Figure 2 illustrates the circuitry involved. Notice that a varactor in series with the crystal has been added in order to be able to pull (frequency shift) the frequency to exactly four times the reference 5 MHz.

Some notes concerning phase locking a crystal oscillator are appropriate.

1. The gain constant of a crystal controlled oscillator, KO, in Hertz per volt, is typically three to four orders of magnitude

TABLE 1 -- TYPICAL OCXO AND TCXO

SPECIFICATION	OCXO	TCXO
Frequency	5 or 10 MHz	5 to 50 MHz
Output Level	1 Vrms into 50 ohms	sinewave, TTL, or CMOS
Harmonic Distortion	-40 dBc	-20 dBc
Frequency Adjustment	+2.5 PPM minimum coarse mechanical. ±2x10E-7 fine ±1 PPM voltage control	±2x10E-6 minimum
Input Voltage	+ 12 V.D.C., ±10%	+ 12 V.D.C., ±5%
Frequency Stability vs Input Voltage	±3x10E-9 for ±10%	±2x10E-7 for ±5%
Frequency Stability vs Load	±1x10E-9 for ±10%	±2x10E-7 for ± 2:1 VSWR
Frequency Stability vs Temperature	±5x10E-9 -20°C to +75°C	±5x10E-7 -20°C to +60°C
Warm-Up Time	±1x10E-7 in 15 mins ±1x10E-8 in 20 mins	< 1 second
Aging Rate	1x10E-9/24 hours	1x10E-8/24 hours
Short Term Stability	3x10E-11 r.m.s Tau = 1 sec	1x10E-9 r.m.s Tau = 1 sec
Input Current	340ma. at turn-on 135ma. at 25°C 225ma. at -20°C	15 ma.
Size	2" x 2" x 4"	1" x 2" x 0.5"

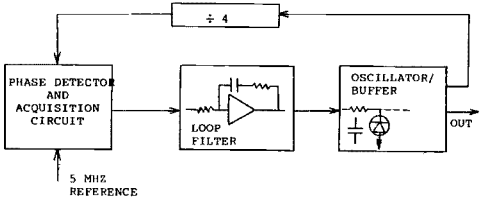


Figure 2, Phase Locking

less than that for a VCO (voltage controlled oscillator). The 20 MHz example would have an average KO of 500 Hz per volt.

2. The loop bandwidth for a phase locked loop using a crystal controlled oscillator is typically 10 to 200 Hz. Very much narrower bandwidths may cause loop phase jitter problems. Wider bandwidths are limited by frequency response roll-off caused by the narrow band nature of the oscillator.

3. The crystal oscillator must be capable of being pulled, or slewed, by an amount equal to its' temperature and ageing frequency error. This assumes that the master oscillator drift is negligible. The TCXO and the phase locked oscillator both require electronic tuning, by means of a varactor diode, or varicap. It is appropriate to discuss varactor tuning in more detail, before discussing overtone crystal oscillators because overtones have very limited "pullability."

VCXO (VOLTAGE CONTROLLED CRYSTAL OSCILLATOR

The equivalent circuit for a crystal is shown in Figure 3.

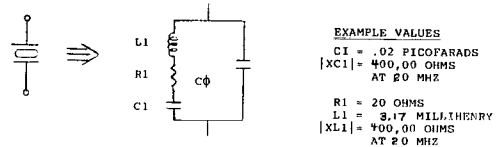


Figure 3, CRYSTAL EQUIVALENT CIRCUIT

L1, C1 and R1 represent the piezoelectric coupled mechanical resonator characteristics. CO is the capacitor formed by the crystal electrodes. Typical values for the 20 MHz crystal are shown. When the crystal is part of a complete circuit,as shown in Figure 4, oscillation occurs at a frequency above F1, where the crystal series arm presents a net inductive reactance, resonant with the capacitors and inductors in the circuit.

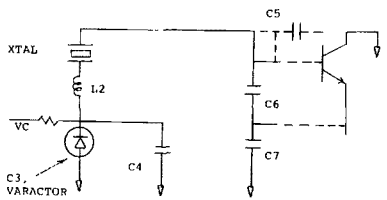


Figure 4, CRYSTAL AND CIRCUIT

The resonant frequency of the complete circuit can be calculated for any particular set of values by writing the appropriate equations for the resonant frequency and solving. This is conveniently done on a computer. Seven cases have been calculated and presented in Table 2 for typical circuit values.

In Table 2 the values of C1, C4, C6/C7, L2 and the varactor parameters (C3) are varied to show the effect on frequency pulling and linearity. A control voltage range of 1 volt to 10 volts is assumed. The frequency data is listed as; (1) PPM away from crystal series arm resonance, (2) the 1 V to 10 V frequency delta, (3) The frequency voltage sensitivity in PPM per volt, at the ends of the range.

In case 1, the difference in sensitivity at 1 V and 10 V is extreme. This results from the varactor capacity-voltage characteristic and from the loss of sensitivitiy as the crystal is pulled further from resonance. Case 2 is like Case 1 except that C1 has been halved. It is seen that the delta F is also reduced by 2, showing the direct dependence of "pullability" on C1. This is discussed in the section on overtone operation. Notice that the difference in 1 V to 10 V sensitivity is not as extreme in case 2 because the crystal is not pulled as far from series resonance. Case 3 shows that C4 reduces pulling and degrades linearity.

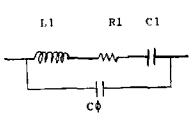
In Case 4 the varactor 4 volt value is changed from 30 picofarads to 16 picofarads, resulting in greater pullability and better linearity. Cases 5, 6, and 7 use a hyperabrupt varactor (gamma = .8) instead of the abrupt junction one. This yields improvement in pulling and linearity. Finally, Case 7 shows that the addition of a three microhenry series inductor (L2) further increases pulling. One note of caution. Reducing the varactor capacity results in an increase of the circuit parallel loss. In Case 6, for example, unless the crystal resistance is suitably low, the circuit may stop oscillating at 10 volts.*

* This topic is addressed in the paper "Maximizing Crystal Oscillator Frequency Stability" Session R-2, r.f. expo 66.

THE OVERTONE CRYSTAL AND OSCILLATOR

It might be asked of the model local oscillator chain, "Why start at 20 MHz?" "Why not use a 5th overtone crystal at 100 MHz, save a lot of multiplication and move the close in spurious out by a factor of 5"?

For the original stability assumption of ± 40 PPM, this might be an attractive choice. With a tight frequency tolerance, it is not, and to see why, the overtone *equivalent* circuit will be examined. Shown in Figure 5 below is the equivalent circuit of the same 20 MHz crystal, but for the 3rd or 5th overtone mode:



LI =3.17mH; R1 = 10 TO 100 OHMS

C1; 3rd OVERTONE = $\frac{C1,\ FUND.}{9}$

$\approx$ .0022 PFD.

5th OVERTONE = $\frac{CI,\ FUND.}{25}$

$\approx$ .0008 PFD.

Figure 5, OVERTONE EQUIVALENT CIRCUIT

It is seen that the inductance remains the same, while C1 is reduced by a factor N^2, where N is the overtone, 3, 5, 7*, 9* etc. Consequently, the "pullability" of an overtone crystal is reduced by approximately the overtone number squared, compared to the fundamental mode. Typical pullability for a 60 MHz 3rd overtone would be on the order of ±30 PPM, and for a 100 MHz 5th overtone, ±10 PPM. Clearly, there is not enough pull range to use these modes in the TCXO or phase locked examples described here.

* Higher than 5th are relatively rare.

SHORT TERM STABILITY

Thus far, those systematic changes in frequency have been discussed which are due to factors such as temperature and time. Oscillator frequency is also perturbed by random, noise-like factors, and these perturbations typically are important for disturbances with time constants from microseconds to seconds. This short term stability is measured in the time domain where some type of frequency counter is the key instrument, and in the *frequency domain*, where spectral analysis of one form or another is used.

In many of these measurements it is necessary to use two oscillators, either with a small frequency offset, or locked together in a phase locked system. Some typical time domain values are listed in Table 1.

OTHER TOPICS IN CRYSTAL AND OSCILLATOR SELECTION

1. Clock oscillators: Miniature, self contained crystal oscillator and output buffer combinations. These hybrid units are available with output frequencies from sub-Hertz to 150 MHz. Outputs are compatible with standard logic families, TTL, CMOS, ECL. Militarized units are available with stabilities of ±50 PPM

over the temperture range -55° C to +125° C.

2. Low power oscillators: Oscillators for battery operated equipment must sometimes operate on less than one milliampere. Using AT cut crystals in the low megahertz range and special circuits this kind of requirement can be met while retaining the advantage of the AT cut crystals. For outputs in the tens of kilohertz, where looser frequency tolerances or narrower temperature ranges obtain, tuning fork crystal oscillators are available with current drains in the tens of microamperes.

3. AGC: Simple AGC control of the oscillator operating point provides many advantages. Low crystal power dissipation, important for good ageing, can be achieved while avoiding circuit start-up problems sometimes associated with very low power operation.

SUMMARY

Choosing a crystal and crystal oscillator circuit requires matching between the requirements of the application and the characteristics of the oscillator. If the oscillator must be pulled more than 10 or 20 PPM, a fundamental crystal in the 10 to 25 MHz range is probably indicated. If the ultimate in temperature stability, ageing and close-in noise is the object, a 3rd or 5th overtone, 5 MHz, ovenized unit is indicated. For small size, low cost, and nominal AT cut stability, a clock oscillator might meet the objectives.

If VHF or UHF outputs are needed a 3rd or 5th overtone crystal oscillator, operating up to 150 MHz might simplify the design.

TABLE 2 - VCXO

	CIRCUIT PARAMETERS C3, VARACTOR									FREQUENCY PULLING DELTA F, PPM				
CASE	C1	C0	4V.C	GAMMA	C4	C5	C6/C7	L2		1V	10V	DELTA	DF/DV (1V)	DF/DV (10V)
1	.02	5	30	.5	0	2	100	0		322	519	197	38	4
2	.01	5	30	.5	0	2	100	0		161	259	98	19	7
3	.02	5	30	.5	20	2	100	0		284	363	79	20	4
4	.02	5	15	.5	0	2	100	0		447	753	306	65	20
5	.02	5	15	.8	0	2	100	0		379	858	479	87	34
6	.02	5	15	.8	0	2	50	0		488	912	424	76	30
7	.02	5	15	.8	0	2	100	3		-5	680	685*	130	45

* Even greater pulling can be accomplished with a more complex circuit.

High Reliability Electromechanical Switching

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Abstract

Recent developments and industry trends in electromechanical switching are presented. Switch life, measured in millions of cycles per switch position, is compared between what is obtainable in the laboratory and what switch manufacturers will guarantee. The maximum frequency of operation, recently extended from 18 to 26.5 Ghz, can be expected to reach 40 Ghz soon, with the connector performance being the critical factor. Switch configurations of the single-pole n-throw and transfer types are standard, and new configurations include the "S-switch" and n-port matrix switches. Drivers are available with TTL and optional BCD decoders built into the switch. Switch design and fabrication techniques are focussed on high reliability, including materials and processes for spacecraft and operating vibration levels up to 82 g_{rms}.

Introduction

When the subject of high reliability electromechanical switches comes up, the first question that is usually asked is "why electromechanical switches in the age of solid state?" Comments then follow about the lower reliability of components with moving parts. The purpose of this paper is to present performance characteristics of electromechanical switches currently available that are accurately described by the term "high reliability."

Besides having no moving parts, solid-state switches have the advantages of very fast switching time and small size. The disadvantages of solid state switches generally include higher loss, less isolation, higher SWR, lower power handling, and higher price. Also, solid state switches do not offer many of the options that are available with electromechanical switches.

The type of switches described will be limited to those with coaxial RF connectors only.

Switch Operation

The functional block diagram of an electromechanical switch is shown in Figure 1. The actuator provides the necessary mechanical forces to perform the switching functions, which take place in the RF head. The key parts of the actuator are at least one solenoid (including a coil and plunger), and rockers and springs as required by

the actuation mode. The RF head includes the RF connectors, center conductor probes, and reeds (contacts).

The driver circuit may be internal or external to the switch, and provides the selected actuation voltages. Optional indicator circuits permit external monitoring of the switch position and operation.

Figures 2 through 4 illustrate the common types of actuation available in an electromechanical switch. In the latching configuration (Figure 2) the switch remains in a position until a new control voltage is applied to another position. In the normally open configuration (Figure 3) no position is connected until power is applied, and the position is disconnected when power is removed. In a failsafe switch (Figure 4) one position will remain connected whenever power is removed.

Design Reliability

The industry standard guaranteed switch life currently being offered by switch manufacturers is one million cycles per position. Much longer life has been obtained in the laboratory, including a Wavecom SP6T switch which performed for more than 27 million cycles per position.

Actuator. The actuator subassembly is the most critical part of the electromechanical switch from a reliability standpoint. Referring to Figure 2, the actuator must provide a vertical force with no horizontal component. Any horizontal force will cause chatter, wear, stress, fatigue, and eventual failure of the switch. A properly designed solenoid has parts which are independent of each other, resulting in a minimum of interference, and is capable of 150 million cycles with no impairment of function.

Reed. The second most important part of the switch is the reed, which provides the electrical contacts. Two processes must be performed correctly on the reeds: heat treating and gold plating. These processes are usually developed and maintained in a proprietary status by each switch manufacturer. In achieving the 27 million cycles per position mentioned above, there was no change in insertion loss.

Temperature. The parts of a switch which are affected the most by temperature extremes are springs and solenoid coils. Standard spring steel will stiffen at -54 deg C and will soften and lose tension at +120 deg C. A special corrosion-free spring material which stiffens at -100 deg C and softens at +370 deg C may be used instead. Coils may be constructed to function from -85 to +190 deg C. Using these techniques, an electromechanical switch will operate from -60 to +135 deg C with no degradation in loss, SWR, or isolation.

Vibration. Wavecom switches in a normally-open multi-position configuration have passed operating tests with up to 82 g_{rms} random vibration.

Spacecraft. The manufacture of high reliability switches for space systems may require more material traceability and process

Options

Internal terminations. All positions may be independently terminated in 50 ohms, with a 1.5 SWR maximum and 5 watts CW dissipation to 26.5 Ghz, .

Indicators. As a result of recent improvements in indicator circuits, the same lifespan is now possible for indicators as for the RF switch. Typically after a million cycles, the indicator DC resistance is less than 0.5 ohm.

Driver logic. Most switch applications now involve computer control. Electromechanical switches can interface to IEEE 488, MP-IB, BCD/CMOS and TTL logic. In effect, almost any type of electronic interface is possible, either internal or external. The driver circuits can also control other circuits besides the switch.

Configurations. Figures 8-11 show the details of SP2T failsafe and latching switches, and SP6T failsafe and normally open switches. These are representative of conventional configurations. Options in these types of switches include normally open with failsafe to position 1, break before make, and either electronic or mechanical make before break (capable of hot switching).

Figure 12 is a schematic of the common transfer switch, which permits switching between the combinations 1-3, 2-4 and 1-2, 3-4. A more general type is the "S-switch" shown in Figure 13. This adds the combination 1-4, 2-3 to those of the transfer switch.

Another type of configuration is called a matrix switch (not to be confused with a switch matrix), as shown in Figure 14. The center position is a dummy one that has no external connection. By appropriate actuation, any two external ports can be connected to each other through the center, with all other ports open or terminated internally. Variations are possible such as adding reeds between adjacent ports, which allows the simultaneous connection of certain port pairs.

Applications

Because of the increasing reliability and performance of electromechanical switches, they are now being used routinely in high-reliability space, airborne, missile and ground systems. They continue to be widely used in test equipment, instrumention and communication systems.

control than is required for other applications. Depending on system requirements, some materials and parts may be prohibited due to outgassing or radiation sensitivity. Taking these into account, electromechanical switches are well-suited for space applications.

Performance

RF characteristics. Single-pole switches with two through six positions and SMA connectors are capable of the following performance through 26.5 Ghz:

SWR	1.5 maximum
Insertion loss	0.5 db maximum
Isolation	60 db to 18 Ghz
	50 db to 26.5 Ghz

Swept-frequency performance data are shown in Figures 5-7.

Until recently, the industry standard performance was only up to 18 Ghz. This was extended to 26.5 Ghz through careful refinement of the design. The high frequency SWR performance is determined by the electrical characteristics of the connector and the RF cavity (see Figure 8). The SMA connectors used are very rigid and not susceptable to damage from many matings, and they perform better than APC 3.5 mm or K connectors through 26.5 Ghz. Sources of discontinuities which affect the SWR are the transitions from the coax probes to the reed, and the teflon guide pins in the sides of the RF cavity. By experimentally matching out these discontinuities, and by maintaining close mechanical tolerances in fabrication, good SWR performance is possible.

The absolute upper frequency limit is determined by the isolation, which results from the waveguide-below-cutoff characteristic of the RF cavity. As more switch poles and positions are added, the high frequency performance suffers due to the size of the RF cavities. The maximum operating frequency for some representative production switches are

2P2T	24 Ghz
SP8T	19.5 Ghz
SP10T	18 Ghz
SP12T	12 Ghz

Using new designs, switches in the pre-production stage include SP2T, 2P2T, SP4T and SP6T configurations which operate up to 40 Ghz.

Switching. The industry standard switching time has been 20 ms. This has been reduced to less than .7 ms for normally open and 2.5 ms for latching modes. A switching time of less than 1 ms can be expected in the near future.

Power handling. The power handling capability of electromechanical switches is limited usually by that of the RF connector.

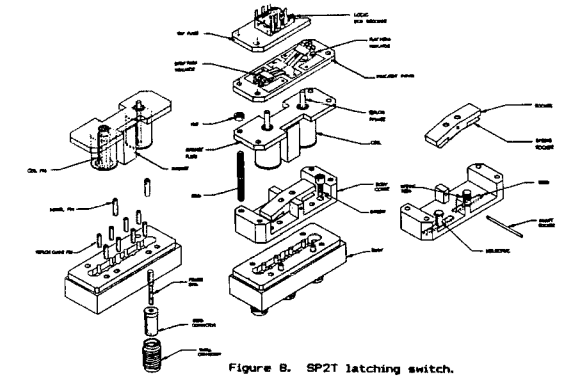

Figure 8. SP2T latching switch.

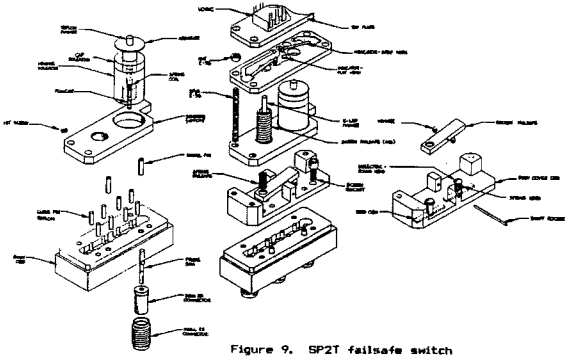

Figure 9. SP2T failsafe switch

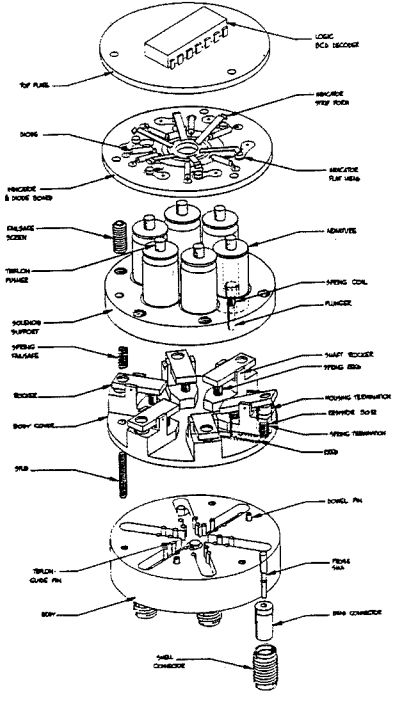

Figure 10. SP6T failsafe switch with terminations.

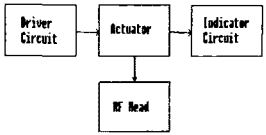

Figure 1. Functional block diagram.

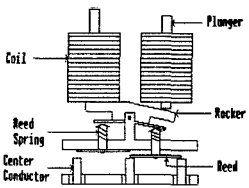

Figure 2. Latching switch.

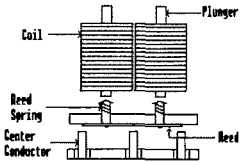

Figure 3. Normally open switch.

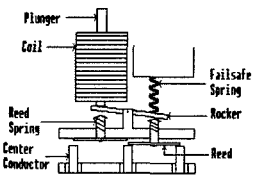

Figure 4. Failsafe switch.

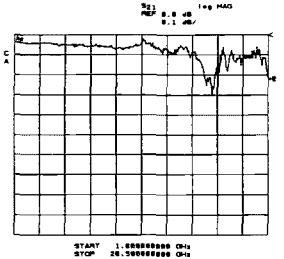

Figure 5. Insertion loss plot.

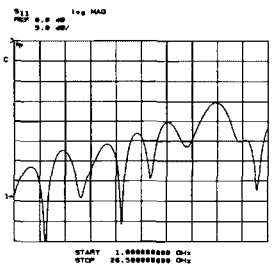

Figure 6. Return loss plot.

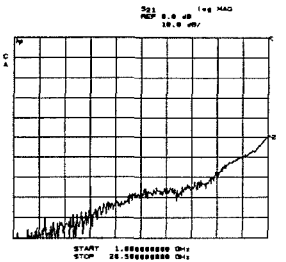

Figure 7. Isolation plot.

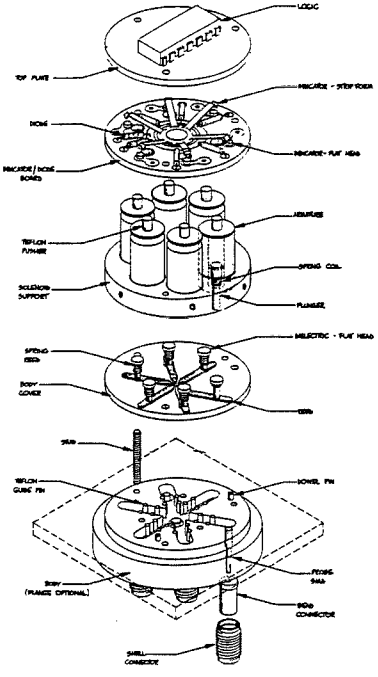

Figure 11. SP6T normally open switch.

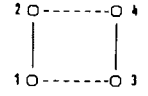

Figure 12. Transfer switch schematic.

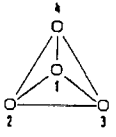

Figure 13. "S-switch" schematic.

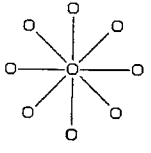

Figure 14. Matrix switch schematic.

Microprocessor Control Considerations for Modern RF Signal Generators

by
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Since the introduction of the microprocessor in the early 70's, there have been many improvements in technology. These improvements have allowed the microprocessor and its associated control elements to be more frequently incorporated into electronic designs. This paper examines some of these improvements and discusses them in the context of a new RF signal generator design.

The most significant improvements affected the microprocessor itself. Improvements in manufacturing lead to more efficient chip layouts and faster speeds which allowed more high-level functions to be included in the basic device. Figure 1 illustrates this by showing the types of functions which are now available in a single package. The resulting reduced chip count allows for a more cost effective design. In addition, the single-chip microprocessor now creates the possibility of including high-level control in the lowest levels of a design. For an RF design which includes a VCO, the high-level functions can include frequency control, linearity correction, leveling, calibration, and dynamic loop compensation. There is a device specifically made for TV tuner control which includes a simple phase detector and frequency prescaler.

Additional ROM/EPROM allows for more code to be written which means more control features. On-bosrd RAM usually satisfies the software engineers programming requirements. In addition, a portion of the RAM can usually be battery backed up so that information such as calibration data can be retained during power-down conditions. The serial port is useful for providing a simple interface to other microprocessors in the design. A programmable timer is important in providing those valuable delays associated with real-world events such as settling times associated with narrow loop bandwidths. In addition to delays, the timer function usually includes an event count feature. This may be useful for control event timing during a digital sweep. The I/O ports provide a simple parallel interface to control elements such as D/A converters, counters, and storage registers. They may also be used to implement a simple serial data-bus.

In more recent devices, EEPROM has been included allowing for non-volatile data storage without the battery mentioned above. There is, however, still a limitation on the number of write cycles for these storage elements. EEPROM should still be used only for storing data which is infrequently modified, e.g. calibration data.

The A/D converter opens a whole range of possibilities such as a comprehensive self-test and diagnostics as well as calibration of detected RF level and modulation circuitry.

CMOS technology appears to be dominating over older technologies such as bipolar (TTL) and RMOS. The small geometries are allowing for faster speeds while retaining the overall low power advantage over the older technologies. In addition, a total CMOS design allows for fully static operation. This means that the timing element or oscillator of a digital element can be stopped

without affecting the state of the digital operation. HCMOS is the nomenclature for high-speed low-power digital devices.

Improvements in microprocessor design are not limited to the hardware. Although the Von Neumann architecture is still retained, instructions have been added to the traditional microprocessor control set.

Software Engineers routinely set and clear flag and status indicators just as Hardware Engineers utilize single bit control mechanisms like those required by analog transmission gates and relay controls. The System or Product Engineer will want to group the non-byte control lines into logically grouped, however, highly mixed byte elements to keep the hardware count low. This means a lot of software activity on a bit basis. Bit orientated instructions which SET, CLEAR and TEST/BRANCH are now available which allow more efficient programming and faster throughput. These instructions were traditionally accomplished by AND'ing and OR'ing a mask byte to the desired control register. The mask byte would affect the desired bits of the control register.

As mentioned previously, HCMOS technology allows for fully static operation. Two instructions (STOP and WAIT) have been added to take advantage of this. WAIT causes the microprocessor to halt operation while the on-board oscillator remains on. STOP halts the microprocessor operation but shuts off the on-board oscillator. The microprocessor returns to full operation through its INTERRUPT facility. The microprocessor resumes operation when a restart or wake-up signal is applied to the interrupt pin of the microprocessor. These instructions provide two important operational advantages: 1) extremely low power consumption and 2) no interference to surrounding circuitry (conducted) or the external (radiated) environment while in the STOP or WAIT modes.

When designing an RF signal generator there are two major control considerations which affect the overall instrument performance. The first is the user interface (front-panel keyboard, display and GPIB) and the second is the overall control mechanism which manipulates the RF section (frequency, level and modulation). Attention to both of these areas is important to good overall user friendliness.

In general, it is considered to be good practice to keep the processing speed of a user orientated device below 100 msec. This will minimize an effect called "rubber-banding". This effect is noticed when the user modifies an instrument setting and does not notice an effect on the instrument operation until after the next setting has been obtained. If a spin knob or cursor keys are used on the front panel, the operator will overshoot the desired setting and will have to go through several iterations of adjustment to get to the desired operating point.

The Wavetek Model 2500 RF Signal Generator utilizes the Motorola MC146805E2 microprocessor and a serial data-bus control structure. The user interface is entirely interrupt driven except for the displays which use dedicated drivers for the custom LCD's.

Either a parallel or serial data-bus structure can be used when designing the control mechanism. Since the data-bus will be the mechanism for controlling both the front-panel operation and the RF sections, special

consideration was given to the selection to minimize conducted noise to the RF sections, reduce the device count for implemonting the data-bus, and maintain good overall throughput to ensure good user response. The serial data-bus easily satisfies the first two design criteria. There is an obvious 8:1 speed disadvantage over a byte orientated parallel data-bus. The real question is "How bad is it?" Measurements made on the Model 2500 show that the entire RF control structure of 112 bits or 14 bytes can be transmitted in less than 10 msec. Figure 2 shows a schematic of the data-bus and Figure 3 shows a flow-chart of the algorithm used to transmit the data.

Within the control circuitry of the RF section the 74HC595 shift register was the primary storage element. These devices were cascaded as necessary to complete the control strings. There are six (6) control strings and a strobe signal. Table I shows the partitioning of the control functions.

TABLE I. CONTROL FUNCTION STRINGS

- VCO Control
- Frequency Divider
- Modulation
- DDS Programming
- Output Level and FM Deviation Correction
- Status Data
- Register Strobe

TABLE II. STATUS INDICATORS

- 400 Hz Square Wave
- Frequency Calibration
- FM Over-Deviation
- Lo-Loop Unlock
- Main-Loop Unlock
- Reverse Power Protection Trip
- Unlevel

Several error conditions can be detected and indicated to the operator on the front-panel. Table II lists these as well as two additional status lines.

The 400 Hz clock line is read during the power-up sequence to determine if the frequency reference is operational. Since the 400 Hz output is the last output in the reference chain, this is just like taking its pulse. An error will also occur if the rear-panel switch is set to EXT REF and the external reference is not connected.

The other status line is used to implement a frequency self-calibration routine for each of the four VCO's. In this routine, each of the oscillators is calibrated and the results stored in the battery backed-up RAM. The entire frequency vs. voltage characteristic is measured for each oscillator. No external equipment is required.

Another contributor to generator performance is computational through-put. Microprocessors are not very good number crunchers. While this may seem contrary to the primary usage of a microprocessor, the existence of the floating-point coprocessor is evidence that the need exists for better arithmetic capability. The computation of a transcendental function should always be avoided. Floating-point multiply and divide routines should be used only when absolutely necessary while the use of add and subtract should be minimized. BCD representations are generally very acceptable even though they are inefficient for RAM storage. Binary representations are native to the microprocessor but are difficult to interpret as the result is usually always binary related and not in nice multiples of 10.

A good compromise is to perform any analog scaling required to give a "good" result. For instance the level control DAC is a 10 bit binary device with the LSB scaled for 1 mV RMS of RF output. This gives a 1 mV to 1.024 V control range. Logarithmic or dBm representations are obtained by first converting the dBm value to volts through the use of a precalculated look-up table. The binary result is then applied to the 10 bit DAC.

The frequency control is primarily BCD. This keeps the reference frequency an even value and simplifies the required arithmetic.

An interesting concern is the organization of the data strings. It is recommended that the data flow be from left to right or LSB shifted out first. This means that the most significant byte of a BCD control string will be the last to the transmitted in the serial string. Logical control string organization reduces the amount of manipulations required by the software to format the string before it is transmitted.

One method of improving the user response time would be to run the microprocessor clock at a faster rate. The MC146805E2 runs at a 4 MHz clock rate which results in a 1 MHz cycle time due to internal divide by 4 circuitry. HCMOS devices are running at toggle rates in excess of 30 MHz. Successful experiments were performed at a clock rate of 8 MHz or 2 MHz cycle times, however, the standard device is not guaranteed at those speeds. Faster parts could be selected by the manufacturer. Note that a change in processor speed affects the value of the delays produced by the microprocessor's timer element.

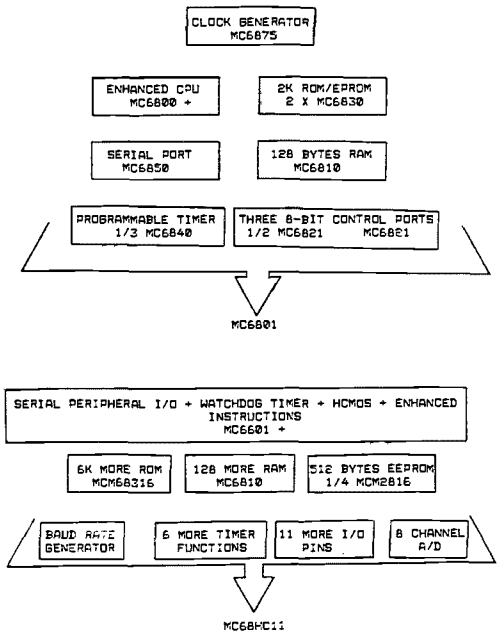
The Model 2500 utilizes a single microprocessor to handle both the front-panel operations as well as the RF control. The previously described clock directed serial data-bus performs the communication to each of the sections. An alternate approach would be to have two microprocessors, one for each of the required control functions. Communications between each microprocessor would take place with either a bi-directional serial or parallel data-bus. The Model 2500 does use an additional microprocessor to implement the standard GPIB communications feature. A parallel 8 bit bidirectional data-bus provides the data exchange mechanism. The handshake mechanism has been simplified for a two microprocessor implementation. However, a multiprocessor parallel data-bus structure has been conceptualized called Quick-bus. It provides a data exchange mechanism for up to 14 microprocessor controlled elements. There are some similarities to the VME bus operation, however the simplification makes a multiprocessor parallel data-bus practical for applications such as an RF signal generator or sweeper. The signaling and arbitration logic is realizable in a simple Programmable Array Logic (PAL) device.

The front-panel was designed for maximum flexibility and smooth operation. Two custom LCD displays with switchable EL back-lighting were used. The modulation and level displays were designed so they are interchangeable. The keyboard matrix is implemented with two MSI devices and can be expanded up to 64 elements. The spin-knob is a conductive plastic incremental encoder which sells in modest quantities for eight dollars. This is in contrast to the optical encoders which sell for 30 to 50 dollars. The keyboard and spin knob are serviced on demand through the interrupt service routine. The interrupt facility provides a minimum response time for the user.

The Model 2500 has full and state-of-the-art talker and listener implementation for the GPIB interface. The command set is very user friendly. It allows a verbose and essentially self-documenting command format for modern ATE and lab bench test systems. The implementation eliminates the vague and cryptic command sets present in current competitive RF signal generators. The talker function allows the full machine status to be obtained as well as a comprehensive reporting mechanism for functional errors.

The most important consideration in the control of RF designs is good communications between the RF and Software Design Groups. The communications mechanism should be a controlled document which both groups can comprehend. It will start with copies of the RF Designer's engineering notebook and end up being reformatted into a form that the Software Engineer can perform his design. The result should be one that either group can pick up and understand the control mechanism of RF sections.

I would like to acknowledge the efforts and contributions of the entire Model 2500 design team. In particular the RF Design Engineers for their patience with the Software Design efforts, the Software Engineers who worked through some difficult organizational situations, and the Mechanical Design Engineers who were the brunt of all the loose ends.


CLOCK GENERATOR MC6875
ENHANCED CPU MC6800 +
2K ROM/EPROM 2 X MC6830
SERIAL PORT MC6850
128 BYTES RAM MC6810
PROGRAMMABLE TIMER 1/3 MC6840
THREE 8-BIT CONTROL PORTS 1/2 MC6821 MC6821
MC6801
SERIAL PERIPHERAL I/O + WATCHDOG TIMER + HCMOS + ENHANCED INSTRUCTIONS MC6801 +
6K MORE ROM MCM68316
128 MORE RAM MC6810
512 BYTES EEPROM 1/4 MCM2816
BAUD RATE GENERATOR
6 MORE TIMER FUNCTIONS
11 MORE I/O PINS
8 CHANNEL A/D
MC68HC11

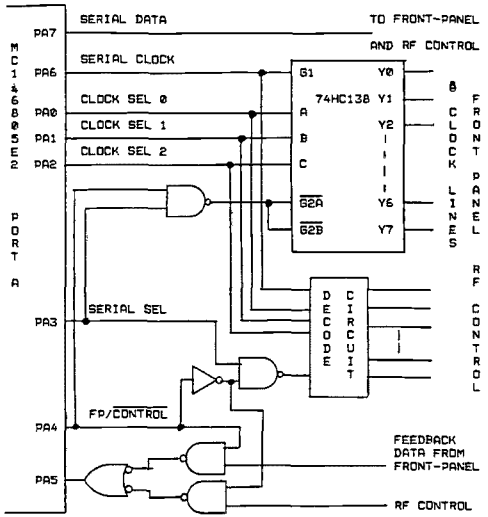


FIGURE 2 : MODEL 2500 SERIAL DATA-BUS STRUCTURE

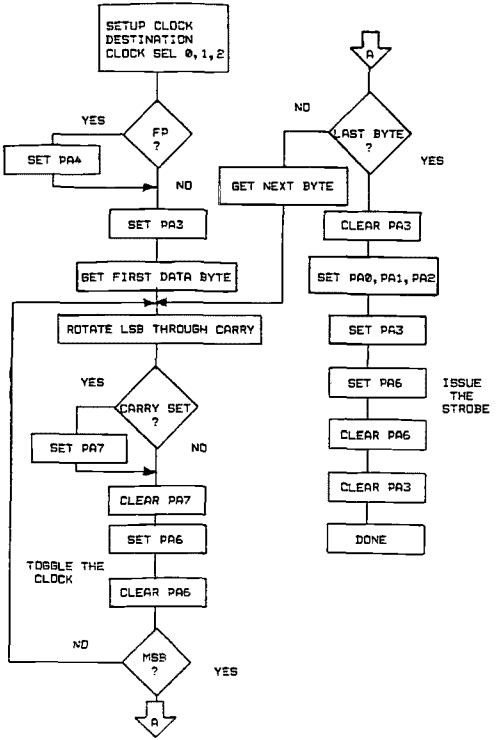


FIGURE 3 : MODEL 2500 SERIAL DATA-BUS CONTROL

EVERYTHING YOU WANTED TO KNOW ABOUT TUNING DIODES

by
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INTRODUCTION

Voltage variable capacitors or tuning diodes are best described as diode capacitors employing the junction capacitance of a reverse biased PN junction. There is a wide range of available capacitances and different device types. The capacitance of these devices varies inversely with the applied reverse bias voltage.

Tuning diodes have several advantages over the more common variable capacitor. They are much smaller in size and lend themselves to circuit board mounting. They are available in most of the same capacitance values as air variable capacitors. Tuning diodes offer the designer the unique feature of remote tuning.

SIMPLIFIED THEORY

A tuning diode is a silicon diode with very uniform and stable capacitance versus voltage characteristics when operated in its reverse biased condition. In accordance with semiconductor theory, a depletion region is set up around the PN junction. The depletion layer is devoid of mobile carriers. The width of this depletion region is dependent upon doping parameters and the applied voltage. Figure 1A shows a PN junction with reverse bias applied, while Figure 1B shows the analogy, a parallel plate capacitor. The equation for the capacitance of a parallel plate capacitor given below predicts the capacitance of a tuning diode.

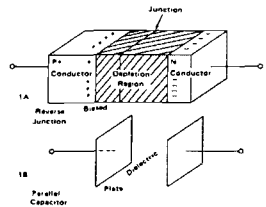


FIGURE 1 - Tuning Diode Capacity Analogy

$$C = \frac{\epsilon A}{d} \qquad (1)$$

where ϵ = dielectric constant of silicon equal to $11.8 \times \epsilon_0$

$\epsilon_0 = 8.85 \times 10^{-12}$ F/m

A = Device cross sectional area

d = Width of the depletion layer.

The depletion layer width d may be determined from semiconductor junction theory.

The more accepted method of determining tuning diode capacitance is to use the defining formula for capacitance.

$$C = \frac{dQ}{dV} \tag{2}$$

The charge, Q per unit area, is defined as:

$$Q = \epsilon E \tag{3}$$

where E = Electric field

So we have capacitance per unit area:

$$c = \frac{C}{A} = \epsilon \frac{dE}{dV} \tag{4}$$

Norwood and Shatz use these ideas to develop a general formula:

$$c = \left[\frac{q B \epsilon}{(m+2)(V+\phi)} \right]^{1/m+2} \tag{5}$$

m = Impurity exponent

c = Capacitance per unit area

Lumping all the constant terms together, including the area of the diode, into one constant, C_D we arrive at:

$$C_J = \frac{C_D}{(V+\phi)^{\gamma}} \tag{6}$$

where γ = Capacitance Exponent, a function of impurity exponent

ϕ = The junction contact potential ($\approx$0.7 Volts)

The capacitance constant, C_D, can be shown to be a function of the capacitance at zero voltage and the contact potential. At room temperature we have:

$$C_D = C_o(\phi)^{\gamma} \tag{7}$$

C_o = Value of capacitance at zero voltage

The simple formula given in Eq. 6, very accurately predicts the voltage-capacitance relationship of tuning diodes. There are many detailed derivations of junction capacitance, so further explanation is not necessary in this paper.

The capacitance of commercial tuning diodes must be modified by the case capacitance.

The equation then becomes:

$$C = C_C + C_J \tag{8}$$

where

C_C = Case capacitance typically 0.1 to 0.25 pF

C_J = Junction capacitance given by equation 6.

TUNING RATIOS/MANUFACTURING PROCESSES

The tuning or capacitance ratio, TR, denotes the ratio of capacitance obtained with two values of applied bias voltage. This ratio is given by the following expression for the tuning diode junction.

$$TR = \frac{C_J(V_2)}{C_J(V_1)} = \left[\frac{V_1+\phi}{V_2+\phi}\right]^{\gamma} \quad (9)$$

where $C_J(V_1)$ = Junction capacitance at V_1

$C_J(V_2)$ = Junction capacitance at V_2

where $V_1 > V_2$

In specifying T/R, some tuning diode data sheets use four volts for V_2. However, in order to achieve larger tuning ratios, the devices may be operated at slightly lower bias levels with some degradation in the Q specified at four volts. (See the discussion of Q versus voltage in the circuit Q section, later in this paper.) Furthermore, care must be taken when operating tuning diodes at these low reverse bias levels to avoid swinging the diode into forward conduction upon application of large ac signals. These large signals may also produce distortion due to capacitance modulation effects.

Since the effects of ϕ and case capacitance, C_C, are usually small, Eq. 9 may be simplified to the following for most design work:

$$TR = \frac{C(V_{min})}{C(V_{max})} = \left[\frac{V_{max}}{V_{min}}\right]^{\gamma} \quad (10)$$

The frequency ratio is equal to the square root of the tuning ratio. This tunable frequency ratio assumes no stray circuit capacitance.

Another parameter of importance is γ, the capacitance exponent. Physically, γ depends on the doping geometry employed in the diode. Varactor diodes with γ values from 1/3 to 2 can be manufactured by various processing techniques. The types of junctions, their doping profiles, and resulting values of γ are shown in Figure 2. These graphs show the variation of the number of acceptors (N_A) and the number of donors (N_D) with distance from the junction.

Abrupt junctions are the easiest to manufacture. This type of junction gives a γ of approximately 1/2 and a tuning ratio on the order 3 with the specified voltage range. Therefore the corresponding frequency range which may be tuned is about 1.7 to 1.0. A typical example is the 1N5441A:

$C(V_2) = C_{(30\ V)} = 2.34$ pF

$C(V_1) = C_{(4\ V)} = 6.8$ pF

$TR = 2.9$

$\gamma = 0.47$

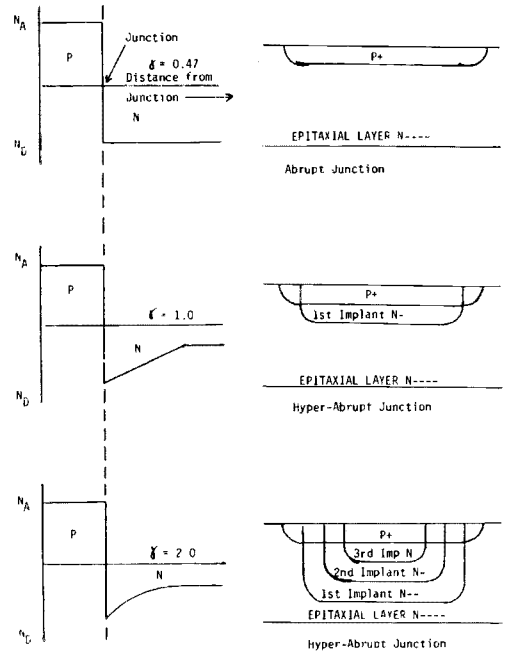
The subscripts on the capacitance refer to the bias voltage applied.

In many applications such as tuning the television channels or the AM broadcast bands, a wider frequency range is required. In this event, the circuit designer must use a tuning diode with a hyper-abrupt junction. The hyper-abrupt junction TD has a γ of one or two and much larger turnable frequency range than does the abrupt junction TD. Table 1 shows typical types of tuning diodes available and their unique characteristics. Figure 2 also shows the processing steps necessary to achieve the desired capacitance exponent. To produce an abrupt junction a P_+ diffusion forms the anode in an epitaxial layer which is the cathode. To produce a hyper-abrupt junction

Device Series	Capacitances Available	Tuning Ratio	Tuning Voltage	γ	Freq. Ratio	Junction Type
1N5139	6.8-47 pF	2.9-3.4	4-60 V	0.47	1.7-1.85	Abrupt
1N5441A	6.8-100 pF	2.9-3.1	2-30 V	0.47	1.7-1.75	Abrupt
MV105G	10 pF	4.5	3-25 V	1.0	2.12	Hyper-Abrupt
MV3102	22 pF	5.0	3-25 V	1.0	2.25	Hyper-Abrupt
MV209	29 pF	5.5	3-25 V	1.0	2.35	Hyper-Abrupt
MV1403	120-250 pF	12	2-10 V	2.0	3.5	Hyper-Abrupt
MVAM108	500 pF	16	1-8 V	2.0	4	Hyper-Abrupt

TABLE 1

with a γ of 1.0 it is necessary to "grade" the epitaxial layer with an ion impant. This produces a tuning diode with a tuning ratio of 4 to 6 when a supply voltage of 25 volts is available. The final challenge to tuning diode designer is to produce a junction with a tuning ratio in excess of 10 with a supply voltage of only 10 volts or less. For this characteristic a hyper-abrupt junction with a γ = 2.0 is required. It is produced by "grading" this epitaxial layer with a triple ion implant. The ability of the manufacturer to place these implants in the epitaxial layer in a repeatable manner as well as the uniformity of the epitaxial layer determines the consistency of the device to device C-V curve.



EXAMPLE 2 - Doping Profiles and Manufacturing Processes for Common Types of Tuning Diodes

CIRCUIT Q

Popular types of mechanical tuning capacitors often have Q's on the order of a thousand or greater. The Q of tuned circuits using these capacitors is generally dependent only on the coil. When using a tuning diode, however, one must be conscious of the tuning diode Q as well. The Q of the tuning diode is not constant being dependent on bias voltage and frequency. The Q of tuning diode capacitors falls off at high frequencies, because of the series bulk resistance of the silicon used in the diode. The Q also falls off at low frequencies because of the back resistance of the reverse-biased diode.

The equivalent circuit of a tuning diode is often described as shown:

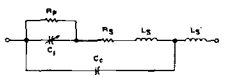


FIGURE 3 - Equivalent Circuit of a Tuning Diode

where

R_p = Parallel resistance or back resistance of the diode

R_S = Bulk resistance of the silicon in the diode

L_S' = External lead inductance

L_S = Internal lead inductance

C_C = Case capacitance

Normally we may neglect the lead inductance and case capacitance. This results in the simplified circuit of Figure 4.

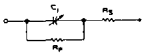


FIGURE 4 - Simplified Equivalent Circuit of A Tuning Diode

The tuning diode Q may be calculated with equation 11.

$$Q = \frac{2\pi f C R_p^2}{R_s + R_p + (2\pi f C)^2 R_s R_p^2} \qquad (11)$$

This rather complicated equation is plotted in Figure 5 for RS = 1.0 ohm,

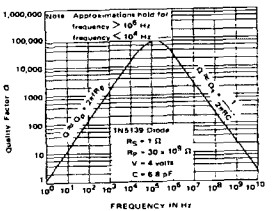


FIGURE 5 - Graph of Q versus Frequency

$R_p = 30 \times 10^9$ ohms, at V = 4 volts and C = 6.8 pF, typical for a 1N5139 tuning diode at room temperature.

At frequencies above several MHz, the Q decreases directly with increasing frequency by the simpler formula given below:

$$Q \approx Q_S = \frac{1}{2\pi f C R_s} \quad \text{(High Frequency Q)} \qquad (12)$$

The emphasis today is on decreasing R_s so better high frequency Q can be obtained. At low frequencies Q increases with frequency since only the component resulting from R_p, the back resistance of the diode, is of consequence.

$$Q \approx Q_p = 2\pi f C R_p \quad \text{(Low frequency Q)} \qquad (13)$$

Q is also dependent on voltage and temperature. Higher reverse bias voltage yields a lower value of capacitance, and also since R_s decreases with increasing bias voltage, the Q increases with increasing voltages. Similarly, low reverse bias voltages accompany larger capacitances, and lower Q's. Increasing temperature also lowers the Q of tuning diodes. As the junction temperature increases, the leakage current increases, lowering R_p. There is also a slight decrease in R_s with increasing temperature, but the effects of the decreasing R_p are greater and this causes the Q to decrease. The effects of temperature and voltage on the Q of a 1N5139 at 50 MHz are plotted in Figure 6.

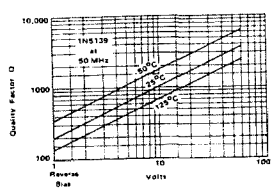
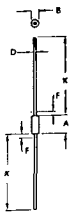


FIGURE 6 - Q versus Reverse Bias and Temperature

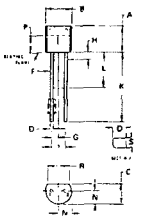
PACKAGE CONSIDERATIONS

Tuning diodes are available in a variety of packages. Two common ones are the axial lead DO204AA, previously referred to as the DO7 and the radial lead TO226AC, sometimes called the two lead TO92. The DO204AA is a hermetically sealed glass package wheras the TO226AC is a plastic encapsulated one. Figures 7 and 8 show the form and dimensional analysis of these two packages. The cost of a tuning diode



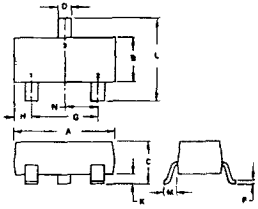
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	38.10	1.000	1.500

FIGURE 7 - DO204AA Dimensional Analysis



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	—	1.27	—	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

FIGURE 8 - TO226AC Dimensional Analysis



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
R	0.89	1.02	0.0350	0.0401

FIGURE 9 TO236AA Dimensional Analysis

package is a function of its piece parts cost and its adaptability toward automation in the assembly process. Because of its relatively expensive piece parts and non-adaptability toward automated assembly the DO204AA is the most expensive tuning diode package, but it does provide a hermetically sealed environment for the tuning diode die. On the other hand, the TO226AC has much less expensive piece parts and is very highly adaptable to automated assembly, but it is not a hermetically sealed package. Tuning diodes are also now available in a surface mount package. This package is available in the TO236AA (standard profile) and TO236AB (low profile) configurations. This package is also commonly known as SOT23. Figure 9 shows the form and dimensional analysis of the package. Due to size constraints about the largest capacitance tuning diode available in the package is 33 pF. This barrier will surely be broken by the development of larger surface mount packages. At this time the cost of a surface mount package is somewhat higher than that of the two lead TO92, but because the surface mount package is highly adaptable to automated assembly it is expected that as the use of surface mount packages increases this volume will reach the point where the piece parts cost of the package will approach that of the two lead TO92.

MANUFACTURER'S DATA SHEETS

This section will discuss the information available to the designer from typical

manufacturer's data sheets. Figure 10 shows the first page of a data sheet for an abrupt junction TD. It normally includes basic type information, maximum ratings and package mechanical information. Figure 11 shows the second page of this data sheet. Information on this page concentrates on electrical characteristics and parameter test methods, as well as including the first graph of a typical characteristic - normalized capacitance versus temperature at various reverse bias voltages. Figure 12 shows the third page of the data sheet. It includes the graphs of most interest to the designer. These include: diode capacitance versus reverse voltages, (C-V curve) figure of merit (Q) versus reverse voltage at a fixed frequency and versus frequency at a fixed voltage, reverse current versus reverse bias voltage for three temperatures and forward voltage versus forward currents. Figure 13 shows the first page of a data sheet for a hyper-aburpt junction tuning diode. It includes primarily the same information as on the first page of the data sheet for the abrupt junction tuning diode. Figure 14 shows the second page of this data sheet. It again includes a table of electrical characteristics, but in this case also shows a C-V curve and a graph of figure of merit (Q) versus voltage at a fixed frequency. A useful comparison is the C-V curve of the abrupt junction diode versus that of the hyper-abrupt junction diode.

VVC

SILICON EPICAP[A] DIODES

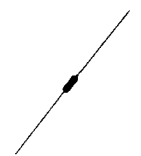
. . . epitaxial passivated abrupt junction tuning diodes designed for electronic tuning, FM, AFC and harmonic generation applications in AM through UHF ranges, providing solid-state reliability to replace mechanical tuning methods.

- Excellent Q Factor at High Frequencies
- Guaranteed Capacitance Change – 2.0 to 30 V
- Guaranteed Temperature Coefficient
- Capacitance Tolerance – 10%, 5.0%, and 2.0%
- Complete Typical Design Curves

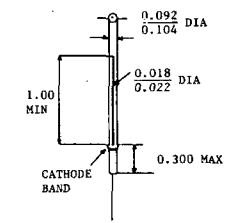
VOLTAGE-VARIABLE CAPACITANCE DIODES

6.8 – 100 pF
30 VOLTS

DS 8526



DO-7 GLASS



CASE 51
DO-7

** MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Operating Junction Temperature Range	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

** Indicates JEDEC Registered Data

FIGURE 10

**ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic – All Types	Test Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	BV_R	30	-		Vdc
Reverse Voltage Leakage Current	V_R = 25 Vdc, T_A = 25°C V_R = 25 Vdc, T_A = 150°C	I_R	-	-	0.02 20	μAdc
Series Inductance	f = 250 MHz, lead length = 1/16"	L_S	-	4.0	10	nH
Case Capacitance	f = 1.0 MHz, lead length = 1/16"	C_C	0.1	0.17	0.25	pF
Diode Capacitance Temperature Coefficient (Note 6)	V_R = 4.0 Vdc, f = 1.0 MHz	TC_C	-	300	400	ppm/°C

Device	C_T, Diode Capacitance* V_R = 4.0 Vdc, f = 1.0 MHz, pF			TR, Tuning Ratio C_J@C30 f = 1.0 MHz		Q, Figure of Merit V_R = 4.0 Vdc f = 50 MHz
	Min (Nom -10%)	Nom	Max (Nom +10%)	Min	Max	Min
1N5441A	6.1	6.8	7.5	2.5	3.1	450
1N5442A	7.4	8.2	9.0	2.5	3.1	450
1N5443A	9.0	10.0	11.0	2.6	3.1	400
1N5444A	10.8	12.0	13.2	2.6	3.1	400
1N5445A	13.5	15.0	16.5	2.6	3.1	400
1N5446A	16.2	18.0	19.8	2.6	3.1	350
1N5447A	18.0	20.0	22.0	2.6	3.1	350
1N5448A	19.8	22.0	24.2	2.6	3.2	350
1N5449A	24.3	27.0	29.7	2.6	3.2	350
1N5450A	29.7	33.0	36.3	2.6	3.2	350
1N5451A	35.1	39.0	42.9	2.6	3.2	300
1N5452A	42.3	47.0	51.7	2.6	3.2	250
1N5453A	50.4	56.0	61.6	2.6	3.3	200
1N5454A	61.2	68.0	74.8	2.7	3.3	175
1N5455A	73.8	82.0	90.2	2.7	3.3	175
1N5456A	90.0	100.0	110.0	2.7	3.3	175

*To order devices with C_T Nom ±5.0%, or ±2.0% add Suffix B or C respectively.

**Indicates JEDEC Registered Data.

PARAMETER TEST METHODS

1. L_S, Series Inductance
L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter or equivalent).

2. C_C, Case Capacitance
C_C is measured on an open package at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

3. C_T, Diode Capacitance
$(C_T + C_C + C_J)$ C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

4. TR, Tuning Ratio
TR is the ratio of C_T measured at 2.0 Vdc divided by C_T measured at 30 Vdc.

5. Q, Figure of Merit
Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency, and substituting in the following equations:

$$Q = \frac{2\pi fC}{G}$$

(Boonton Electronics Model 33A5B or equivalent).

6. TC_C, Diode Capacitance Temperature Coefficient
TC_C is guaranteed by comparing C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = 65°C with C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = -65°C in the following equation, which defines TC_C:

$$TC_C = \frac{|C_{T(+65°C)} - C_{T(-65°C)}|}{85 - (-65)} \cdot \frac{10^6}{C_{T@25°C}}$$

Accuracy limited by C_T measurement to ±0.1 pF.

– NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE

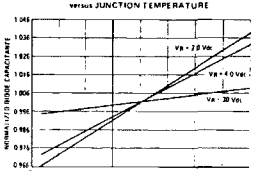
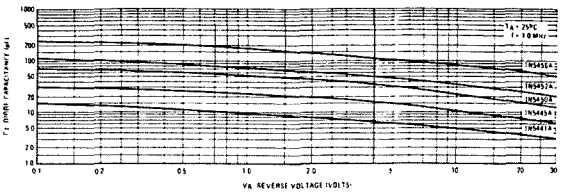


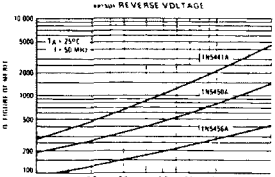
FIGURE 11

TYPICAL DEVICE PERFORMANCE

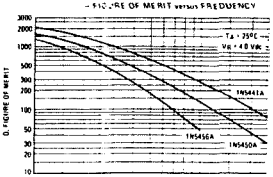
– DIODE CAPACITANCE versus REVERSE VOLTAGE



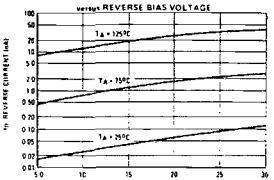
– FIGURE OF MERIT versus REVERSE VOLTAGE



– FIGURE OF MERIT versus FREQUENCY



– REVERSE CURRENT versus REVERSE BIAS VOLTAGE



– FORWARD VOLTAGE versus FORWARD CURRENT

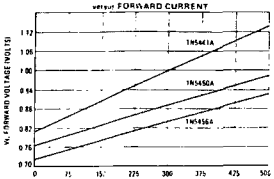


FIGURE 12

MVAM108 MVAM109 MVAM115 MVAM125

VVC

SILICON TUNING DIODE

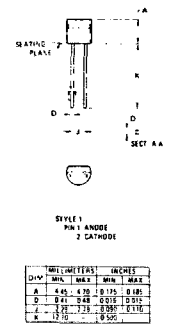
designed for electronic tuning of AM receivers and high capacitance, high tuning ratio applications

- High Capacitance Ratio — C_R = 15 (Min), MVAM 108, 115, 125
- Guaranteed Diode Capacitance — C_t = 440 pF (Min) — 560 pF (Max) @ V_R = 1.0 Vdc, f = 1.0 MHz MVAM108, MVAM115, MVAM125
- Guaranteed Figure of Merit — Q = 150 (Min) @ V_R = 1.0 Vdc, f = 1.0 MHz

TUNING DIODES WITH VERY HIGH CAPACITANCE RATIO

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Reverse Voltage	MVAM108	V_R	12	Volts
	MVAM109		15	
	MVAM115		18	
	MVAM125		28	
Forward Current		I_F	50	mA
Power Dissipation @ T_A = 25°C; Derate Above 25°C		P_D	280; 2.8	mW; mW/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	-65 to +125	°C



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.45	4.70	0.175	0.185
D	0.41	0.48	0.016	0.019
K	12.70	7.75	0.050	0.110

CASE 182-03

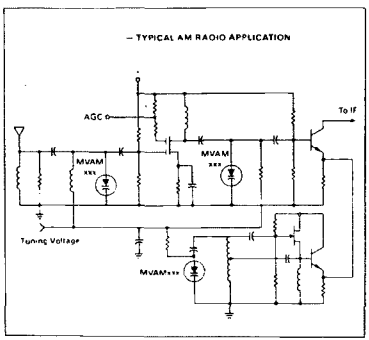


FIGURE 13

Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.

DS80168

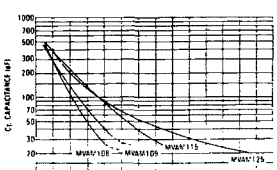
MVAM108 ● MVAM109 ● MVAM115 ● MVAM125

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted; Each Device)

Characteristic — All Types		Symbol	Min	Typ	Max	Unit
Breakdown Voltage (I_R = 10 μAdc)	MVAM108	$V_{(BR)R}$	12	–	–	Vdc
	MVAM109		15	–	–	
	MVAM115		18	–	–	
	MVAM125		28	–	–	
Reverse Current		I_R				nAdc
(V_R = 8.0 V)	MVAM108		–	–	100	
(V_R = 9.0 V)	MVAM109		–	–	100	
(V_R = 15 V)	MVAM115		–	–	100	
(V_R = 25 V)	MVAM125		–	–	100	
Diode Capacitance Temperature Coefficient (1) (V_R = 1.0 Vdc, f = 1.0 MHz, T_A = -40°C to +85°)		TC_C	–	435	–	ppm/°C
Case Capacitance (f = 1.0 MHz, Lead Length = 1/16")		C_C	–	0.18	–	pF
Diode Capacitance (2) (V_R = 1.0 Vdc, f = 1.0 MHz)	MVAM108, 115, 125	C_t	440	500	560	pF
	MVAM109		400	460	520	
Figure of Merit (f = 1.0 MHz, Lead Length = 1/16")		Q	150	–	–	–
Capacitance Ratio (f = 1.0 MHz)	MVAM108	C1/C8	15	–	–	–
	MVAM109	C1/C9	12	–	–	
	MVAM115	C1/C15	15	–	–	
	MVAM125	C1/C25	15	–	–	

Notes:
(1) The effect of increasing temperature 1.0°C at any operating point is equivalent to lowering the effective tuning voltage 1.25 mV. The percent change of capacitance per °C is nearly constant from -40°C to +100°C.
(2) Upon request, diodes are available in matched sets. All diodes in a set can be matched for capacitance to 3 or 2.0 pF (whichever is greater) at all points along the specified tuning range.

— CAPACITANCE versus REVERSE VOLTAGE



— FIGURE OF MERIT

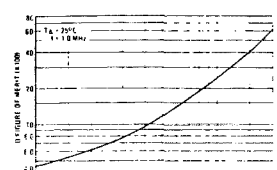


FIGURE 14

SPECIFYING TUNING DIODES

Three common methods of specifying tuning diodes for a particular design application are as follow:

1. Specify a nominal capacitance ± the maximum allowed variation in percent at the lowest voltage which is to be used and a capacitance ratio minimum (and maximum if necessary) between the lowest voltage and highest voltage to be used in the design. This is the method found on most manufacturers' data sheets.
2. Specify a minimum and maximum capacitance at the lowest and highest voltages to be used in the design.
3. Specify a minimum and maximum capacitance at the lowest, the median, and highest voltages to be used in the design. This method enables the circuit designer to "tie down" the C-V curve of a hyper-abrupt junction tuning diode over a large voltage variation.

SUMMARY

Voltage variable capacitors commonly referred to as tuning diodes are rapidly replacing air capacitors in many applications. These devices offer many advantages over previously available variable capacitors, the major one, of course, is the ability to employ remote tuning which has made possible the electronically tuned radio. The circuit designer must be aware of the tuning range and Q limitations of tuning diodes in order to use these devices effectively. Also to be considered must be the package chosen and the cost thereof. A well constructed manufacturer's data sheet can provide the circuit designer with a wealth of information needed to aid him in his design, but the designer must realize that the manufacturer only specifies a capacitance at one voltage and a capacitance ratio between one pair of voltages. If necessary, the circuit designer must request these specifications for his own particular design voltages.

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2. Chang, Y.F., "Capacitance of p-n Junctions: Space Charge Capacitance." Journal of Applied Physics, 37:6, May 1966, pp. 2337-42.

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4. Gray, P.E.; DeWitt, D.; Boothroyd, A.; Gibbons, J., Physical Electronics and Circuit Models of Transistors. New York, John Wiley & Sons, 1964, pp. 8-54.

5. Warner, R.; Fordemwalt, J., Integrated Circuits, Design Principles and Fabrication, New York, McGraw-Hill, 1965, pp. 31-68.

6. Doug Johnson and Roy Hejhall, "Tuning Diode Design Techniques," Motorola Application Note AN-551.

7. George C. Onodera, "Method of Producing an Ion Implanted Tuning Diode," United States Patent #4,106,953, August 15, 1978.

MICROWARE

An Interactive Microwave Filter Design Program

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Microware is a microwave filter design program that enables the user to design filters in a logical, step by step manner. A brief outline, including a flow chart will be given followed by three examples.

Three common filter designs are now supported by the program. They are:

1. **Lumped Component Designs.** A majority of filter design in the frequency range below 1 GHz is of the lumped component type. Virtually any type of circuit configuration may be realized. The sub-program "LUMP" designs some of the more basic circuits. The types supported by this program are:

Tank, Mesch, Lowpass/Bandpass, 4 types of elliptical filters. Impedance and Nortons transforms can be applied to the prototype circuit. Filters can be designed by component value allowing "off the shelf" components to make up a large part of the circuit.

2. **Waveguide Filters.** An accurate design sub-program is included. "IPWG" is based on realizing a lumped circuit with waveguide elements. Currently the program only supports TE01 mode designs. With this, inductive coupled elements in the form of an iris or post may be used.

3. **Cavity Filters.** The third sub-program "INTCL" can design interdigital and combline filters. The user has a variety of options as to the size and electrical configuration. Both round rod and rectangular resonator designs are available. The user also has the option of tapped loading, short or open circuit transmission lines to transform in and out of the filter.

- MainMenu -
The Cornerstone of Microware

While there seems to be an abundance of analysis and optimization programs on the market, the first step, Synthesis is often neglected. In addition to this, many segments of our industry require specilized programs that may not be marketable. A few programs that do have synthesis capabilities are:

Compac - Has a built in synthesis package that lets the user design coupled lines, impedance matching transformers and filters. Available separately is a filter design kit, complex matching and PLL design.

EESof - Has a series of filter design programs by Wenzel/Erlinger Associates. PLL and complex match synthesis programs are also available.

Filsyn - Has the most comprehensive lumped element designs available. The user has the option of specifying all design parameters, including the location of the poles and zeros.

Other programs with design capabilities are available from DSI Software (microstrip and stripline coupled lines), Etron (various RF design programs) and the E.E Public Domain Library (many design programs in the public domain).

It was found that none of these programs provided all of the capabilities for our day to day needs. With this in mind the concept of an all purpose microwave filter design program was conceived. One of the foremost requirements was to provide an interactive environment so that the designs could be modified via software. This program consists of three different areas:

1. User inputs design criteria.
2. Edit Specs.
3. Electrical design

As the user procedes through the program they are guided with the "Windows" and pull down "Menus" familiar to user of the Macintosh. If, at any time the user exceeds the limits of the programs design capability the user is warned with a prompt. Next the specs that have been entered are presented on the screen. The user has the opportunity to change or delete them at this time. When satisfied the design specifications are written to a file named "INSPECS". At any time during the design procedure this can be recalled and changed. Now the program enters the electrical design stage. The normalized element values are calculated and then impedance and frequency scaled. The program now links with the desired sub-program. The Macintosh provides the most "User-Friendly" environment both for programming and design. While the terms "Windows", "menus" and "event-managers" might not be familiar to many electrical engineers, they are an integral part in the world of computer programming. When this program was first written, Microsoft Basic was one of the few languages available. Since beginning, the availability of C language compilers has provided a more flexible environment. A great part of the math routines have been converted to "C".

While the user proceeds through the program, menus document the

progress and the user can "pull" down a menu at any time and modify that particular specification. Much of the program can be executed with use of the "mouse", a graphic pointing device used in this program.

The Design Examples.

Three design examples will be given, all originating from the same main program. The user is offered a variety of design considerations and the program flows in a logical, straight-forward way. The three design examples given here are actual working designs now in production at Microlab/FXR. The management of Microlab/FXR is to be thanked for providing the design information for publication.

Example 1. Lumped Component Design.

This example is for a "Reflectionless" bandpass filter. Reflectionless in that the unit maintains a good VSWR over a much wider range then the bandpass filter. Required also was a flat group delay over the 3 dB bandwidth of the filter necessitating a Bessel Response. The design specifications are as follows:

Center Frequency: 300 MHz.

Bandwidth (3 dB): F_0 +/- 15 MHz. min. +/-18 MHz. max.

VSWR: ≤1.1:1 at F_0
≤1.3:1 from 250 - 350 MHz.

Group Delay: 20 +/- 2 nS. relative to a thru line
≤1.5 nS over 3 dB bandwidth

Insertion Loss: ≤1.0 dB at F_0

Stopband: ≥20 dB relative from D.C. -250 MHz. and 350 - 1000 MHz.

Figure II shows a functional diagram of the required circuit.

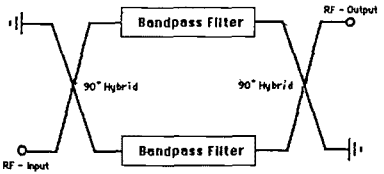


Figure II

To obtain a good VSWR over a bandwidth much wider then the passband of the filter a combination of two 3 dB hybrid couplers are used. The filters are separated by a line length via the coupled line of 90 degrees at center frequency (300 MHz.). When the filters are phase matched over their 3 dB bandwidth, reflection from either filter is absorbed by 50 ohm termination incorporated on either side of the coupler. Thus the input VSWR is determined by the accuracy that the two filters can be phase matched. This

technique is also used to phase match filters when only a scalar network analyzer is available. When first constructed two prototype filters and hybrid couplers were built. Then the filters were aligned and adjusted for best group delay response. With the appropiate connectors the two filters and couplers were put together. At this time it was necessary to match the filters to get the required VSWR response. The combination of VSWR and tight group delay variation requirements made this a difficult and time consuming procedure. An electrical schematic is shown below.

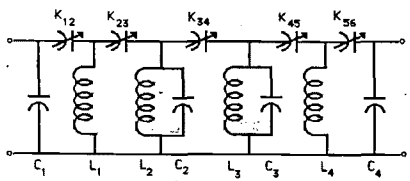


FIGURE III

Design Impedance: 50 Ω Transform to: 1329.91 Ω

Shunt Capacitor C_1= 51.57344 pF.
Series Capacitor C_2= 12.40538 pF.
Shunt Inductor L_1= 2.796390E-02 µH.

Coupling Capacitor K_{12}= .630816 pF.

Inductor L_2= 2.86628 µH. Capacitor C_3= 10 pF.

Coupling Capacitor K_{23}= 1.12957 pF.

Inductor L_3= 2.86628 µH. Capacitor C_4= 10 pF.

Coupling Capacitor K_{34}= 2.58944 pF.

Shunt Inductor L_4= 2.796390E-02 µH.
Series Capacitor C_5= 15.62833 pF.
Shunt Capacitor C_1= 27.76726 pF.

Transform to: 122.12335 Ω to 50 Ω

The responses of a typical production unit are shown in figure V.

Example 2. Interdigital Filter

This example shows the extreme bandwidths that can be achieved by this program. An equi-ripple bandwidth of 66% has been achieved in this design (program maximum is ~70%). In addition to the wide bandwidth, the VSWR and insertion loss specifications add to the difficulty of this requirement. The design specifications are as follows:

Passband Frequency: 8.0 - 16.0 GHz.

VSWR: ≤1.5:1 over passband

Insertion Loss: ≤0.6 dB. over passband

Stopband: ≥25 dB @ 6.4 GHz. and 20 GHz.

Power: 100 Watts Avg. 3 KW peak 1% Duty Cycle

This requirement for a wideband interdigital filter approaches the limits of both the electrical and physical designs currently available. The basis for interdigital filter design is widely documented (See Ref. 1-6). This program offers the user the option of designing with rectangular and round rods, rectangular giving the most efficient coupling for a given spacing and the round rod approach being less expensive to manufacture. A schematic is shown below:

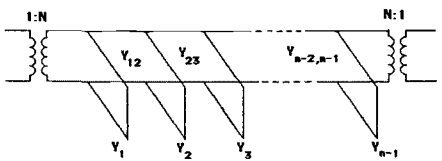


FIGURE IV

The filter was designed following the program prompts (see menus at the end of the article). The wideband design with rectangular bar resonators was used. To make the spacings between the bars practical, a high internal impedance and a large ratio of ground plane spacing to bar thickness was used. The printout containing the mechanical dimensions is shown below.

INTERDIGITAL / COMBLINE DESIGN

Bar Thickness: 0.02 ins.
Design Impedance: 50 Ω
Bar Length(1,N): 0.225 ins.
Cavity Width: 0.2459 ins.

Ground Plane Spacing: 0.300 ins.
Internal Impedance: 175 Ω
Bar Length (2,N-1): .200 ins.

k	C_k / e	Width (ins.)	$C_{k,k+1}$ / e	Spacing (ins.)
Bar (1)	3.2772	.1398		
Spacing (1,2)			2.0716	.0220
Bar (2)	.8419	.0343		
Spacing (2,3)			1.0040	.0532
Bar (3)	1.4699	.0556		
Spacing (3,4)			.9137	.0605
Bar (4)	1.5228	.0557		
Spacing (4,5)			.8839	.0634
Bar (5)	1.5413	.0557		
Spacing (5,6)			.8735	.0644
Bar (6)	1.5462	.0557		
Spacing (6,7)			.8735	.0644
Bar (7)	1.5413	.0557		
Spacing (7,8)			.8839	.0634
Bar (8)	1.5228	.0557		
Spacing (8,9)			.9137	.0605

Bar (9)	1.4699	.0556		
Spacing (9,10)			1.0040	.0532
Bar (10)	.8419	.0343		
Spacing (10,11)			2.0716	.0220
Bar (11)	3.2772	.1398		

The electrical response for a typical production unit is shown in figure VI

Example 3. Waveguide Filter

This example shows the accuracy which a waveguide filter with difficult stopband requirements can be realized. Adding to the difficulty of this design are the insertion loss and VSWR requirements.

Center Frequency: 15.1 GHz.

Bandwidth: .25 GHz.

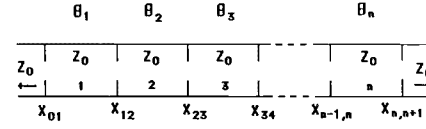
Insertion Loss: ≤0.3 dB over Passband

VSWR: ≤1.3:1 over passband

Stopband: ≥60 dB. @ 14.6 GHz. and 15.7 GHz.

This third requirement is for a low loss waveguide filter uses equations available from ref. 1-3. The user may choose to design with an inductive post or iris. The program includes corrections for the finite thickness of the post or irises. If the calculated reactance causes the thickness of the end posts to be less then 0.050 ins. the program will calculate an offset post.

The electrical circuit is shown below:



The user follows the program prompts and the print out of the mechanical dimensions are as follows.

Inductive Post Wavguide Design

Post Diameters

Post (1)= 0.100 Ins. Offset from C/L= .047
Post (2)=0.16295 ins.
Post (3)=0.16746 ins.
Post (4)=0.17001 ins.
Post (5)=0.17001 ins.
Post (6)=0.16746 ins.
Post (7)=0.16295 ins.
Post (8)=0.100 ins. Offset from C/L=.047

Post Spacings

Spacing (1,2)= 0.60709 ins.
Spacing (2,3)=0.67603 Ins.
Spacing (3,4)=0.68136 ins.
Spacing (4,5)=0.68136 ins.
Spacing (5,6)=0.67603 ins.

Spacing (6,7)=0.60709 ins.

References:

Interdigital and Combline Design

1. Conformal Transformation Combined with Numerical Techniques, with Application to Coupled-Bar Problems
Ralph Levy
IEEE Microwave Theory and Techniques. April 1980

2. Tapped-Line Coupled Transmission Lines with Applications to Interdigital and Combline Filters
Edward G. Cristal
IEEE Microwave Theory and Techniques. December 1975

3. A Study of the Phase and Filter Properties of Arrays of Parallel Conductors Between Ground Planes
JT Bolljohn
IEEE Microwave Theory and Techniques. March 1962

4. Coupled Circular Cylindrical Rods Between Parallel Ground Planes
Edward G. Cristal
IEEE Microwave Theory and Techniques. July 1964

5. Coupled Rectangular Bars Between Parallel Plates
William Getsinger
IEEE Microwave Theory and Techniques. June 1962

6. Microwave Filters, Impedance Matching Networks and Coupling Structures
Matthaei, Young & Jones
Artech House

Waveguide Design

1. Improved Single and Multiaperature Waveguide Coupling Theory, Including Explanation of Mutual Interactions
Ralph Levy
IEEE Microwave Theory and Techniques. April 1980

2. Waveguide Handbook
N. Marcuvitz
MIT Radiation Lab Series

3. Microwave Filters, Impedance Matching Networks and Coupling Structures
Matthaei, Young & Jones
Artech House

Lumped Componant Design

1. Handbook of Filter Synthesis
Anatol V. Zverev
Wiley-InterScience

2. Reference Data for Radio Engineers
ITT

3. Filtering in the Time and Frequence Domains
Blinchikoff and Zverev
Wiley-InterScience

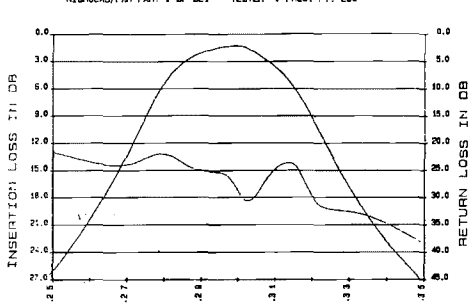


FIGURE V

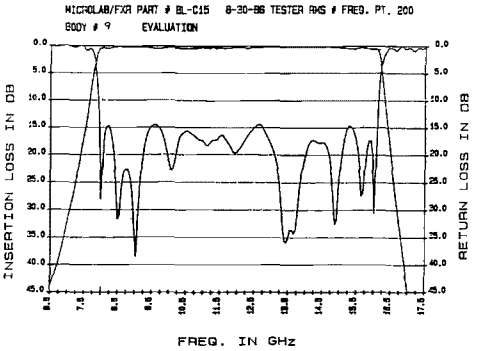
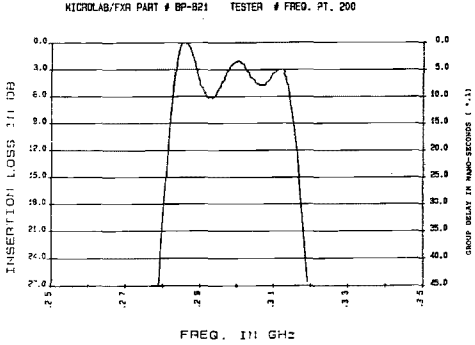
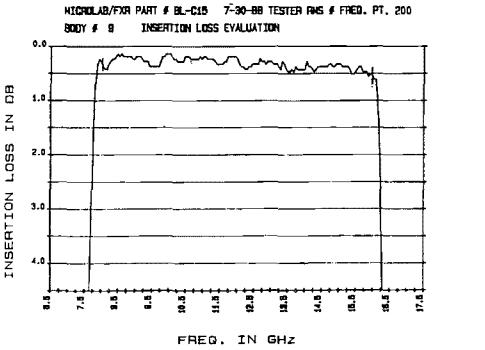


FIGURE VI





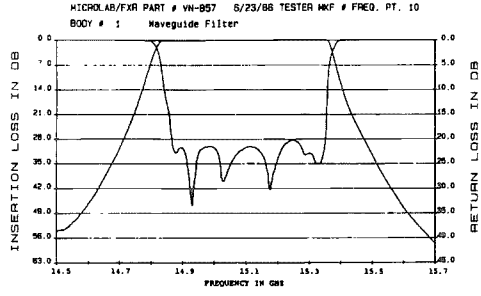

MICROLAB/FXR PART # VN-857 5/23/88 TESTER MKF # FREQ. PT. 10
BODY # 1 Waveguide Filter
INSERTION LOSS IN DB
RETURN LOSS IN DB
0.0
7.0
14.0
21.0
28.0
35.0
42.0
49.0
56.0
63.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
45.0
14.5
14.7
14.9
15.1
15.3
15.5
15.7
FREQUENCY IN GHz

FIGURE VII

A Practical Approach to the Design of Voltage Tunable Lowpass and Bandpass Filters

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Introduction

Many filters are used in RF systems. Most are fixed tuned but occasionally a tunable filter is required. A preselector in a receiver is one example. Tunable filters are also useful as tracking filters in frequency synthesizers, as variable IF filters in block conversion receivers and as variable post detection video filters. Tunable filters can be constructed by mechanically ganging tuning components to a common tuning shaft but this approach is bulky, expensive and not very adaptable to microprocessor control. Voltage tuned filters overcome these difficulties and are suitable in many applications. The control voltage can come from a front panel potentiometer, a microprocessor controlled DAC, or from another voltage controlled stage such as a voltage controlled oscillator allowing both stages to track one another.

This paper explores the design of voltage tuned lowpass and constant percentage bandwidth bandpass filters. Many filters are designed quite easily using tables of normalized component values. A lowpass filter design example is presented to emphasize the relationship between filter component values, impedance, and frequency. This relationship implies careful control of filter impedance is essential if the filter is to be tuned. With this understanding the lowpass filter is transformed into a tunable lowpass filter covering one octave with the help of a pair of impedance control networks.

Next this approach is extended to include constant percentage bandwidth bandpass filters. The paper concludes with a discussion of intermodulation performance, practical frequency and tuning range, and circuit modifications to improve realizability. Filters, tunable over at least one octave, from several hundred kilohertz to several hundred megahertz, can be successfully designed using this approach.

Filter Design Review

Textbook filter design usually involves finding the roots of the filter transfer function as the starting point for a classical circuit synthesis approach. While providing insight to the mathematical origins of the filter this approach has little to recommend it for day to day filter design.

It is simple to design most filters from standard tables. These tables consist of component values for filters normalized to one ohm, one radian per second and are available from several references including Williams and Zverev. Select from the table the component values for a prototype lowpass filter with the appropriate number of poles and of the desired filter family (Butterworth, Tschebyshev, Bessel, etc). Final component values are obtained by frequency and impedance scaling of the prototype values. Figure 1 shows a three pole, 20 MHz Butterworth lowpass filter and the prototype from which it was scaled.

A lowpass filter can be transformed into a highpass, bandpass, or bandstop filter and implemented with lumped LC components, or transmission

lines as required. Other transformations that rearrange component values to improve realization are also possible.

To transform a lowpass filter into a bandpass filter shunt inductors and series capacitors are added to resonate the shunt and series branches at the desired filter center frequency. The new filter retains the bandwidth and impedance of the original lowpass filter. A 60 MHz bandpass filter transformed from a 20 MHz lowpass filter has a passband extending from 50 to 70 MHz. The center frequency can be shifted by changing the values of the shunt inductors and series capacitor without affecting the filter bandwidth or impedance.

Tunable Lowpass Filter Design

This section of the paper develops an approach to the design of tunable lowpass filters which takes advantage of frequency and impedance scaling. The results will be applied later to the design of voltage tuned bandpass filters. Since frequency and impedance scaling go hand in hand to obtain filter component values careful control of filter impedance is necessary if the filter is tuned. What type of impedance control is required and how can it be incorporated into a practical design?

Let's look at a three pole Butterworth lowpass filter, tunable over an octave from 60 to 120 MHz with a 50 ohm input and output impedance. A 60 MHz filter is designed by frequency and impedance scaling of the Butterworth prototype (Figure 2a). The 120 MHz version of this filter is identical in form but has inductors and capacitors one half as large as its 60 MHz counterpart (Figure 2b).

The filter in Figure 2b can be converted into its 100 ohm equivalent (Figure 2a) by doubling the inductor value and halving the size of the capacitors. Notice the inductor in this filter is the same as the inductor in the 60 MHz 50 ohm filter.

A voltage tuned filter could be built if each of the filter components were replaced with its voltage variable equivalent. While voltage variable capacitors are widely available in the form of varactor diodes, voltage variable inductors are a bit of a problem.

Electrically variable inductors, relying upon the saturation of a ferrite core by a DC control current, are available; however, they are expensive, bulky and consume a large amount of control current. An ideal voltage tuned filter would use only varactor diodes as tuning elements.

The total variation required to tune a filter over an octave is four to one, half of the variation coming from the inductors, the other half from the capacitors. Fixing the inductor value and using varactors to tune the filter means the entire four to one tuning variation must come from the varactors. Something has to give, and as implied earlier that something is the filter impedance. Comparing Figures 2a and 2c shows that a fourfold reduction of the filter capacitors doubles both the filter frequency and impedance. Filter impedance variation as the filter is tuned is the price that must be paid for the convenience of fixed inductors.

Impedance variation of this magnitude is not acceptable in most applications. In addition to the obvious VSWR problem, filter bandwidth and insertion loss are adversely affected by input and output mismatch. Perhaps the unwanted impedance variation can be compensated by a tunable matching network that provides a variable impedance match as the filter is tuned. This compensation network should be as simple as possible and should not require variable inductors. In addition, its tuning varacters

should track those of the filter to which it is connected.

An L-Match is a simple two element impedance transformation network used for single frequency resistive impedance matching. Figure 3a shows an L-Match network, transforming 50 ohms to 75 ohms at a frequency of 60 MHz, and the relevant design equations. Can this network provide twice the impedance transformation (50 ohms to 150 ohms) at twice the design frequency without changing the inductor?

Repeating the L-Match design for a frequency of 120 MHz and an impedance transformation of 50 to 150 ohms gives the network shown in Figure 3b. The shunt capacitor is one half of its 60 MHz value and the inductor is unchanged.

By simultaneously tuning the shunt capacitor, the L-Match can properly terminate a 60 to 120 MHz tunable lowpass filter providing the filter is redesigned to present an impedance of 75 ohms at 60 MHz.

The initial impedance step-up required at the minimum filter frequency is a function of the filter tuning range and is found by simultaneous solution of the L-Match design equations to provide the proper impedance transformation at both ends of the filter tuning range. This solution is expressed by the equation listed below where R is the filter tuning ratio, and N is the initial impedance transformation at the low frequency end of the filter tuning range. N is equal to 1.5 for a one octave tunable filter and decreases to 1.25 for a two octave filter.

$$N = \frac{R^2 - 1}{R(R - 1)} \qquad R = \frac{\text{filter upper frequency}}{\text{filter lower frequency}}$$

Octave tuning requires a four to one capacitance ratio in the filter section as opposed to the two to one ratio needed in the matching network. Ideally both ratios should be the same to allow the use of a common tuning varactor.

The matching and filter section varactors can be combined into a single varactor if part of the varactor capacitance variation is absorbed or swamped with a fixed padding capacitor. For an octave tuned filter the padding capacitor makes up one third of the low frequency matching capacity with the other two thirds coming from the varactor.

Combining the matching network shown in Figure 3 with the filter from Figure 2a and 2c gives the tunable filters in Figure 4. The tuning capacitance varies fourfold from 69 pf at 60 MHz to 17.3 pf at 120 MHz. At 60 MHz 16.7 pf of the tuning capacitance tunes the matching network, while the remaining 52 pf is part of the filter network.

Blocking capacitors can be added to isolate the varactor control voltage which is supplied through a decoupling resistor or RF choke. The actual padding capacitor will be smaller than calculated when the stray capacitance at that node is considered.

Tunable Bandpass Filters

A voltage controlled bandpass filter can be designed by lowpass to bandpass transformation of a voltage controlled lowpass prototype. Unfortunately the lowpass to bandpass transformation which works well for wideband (BW > 10%) filters gives unrealizable component values if a narrowband filter design is attempted. Many advantages of a tunable bandpass filter are lost if the filter bandwidth is too large.

An alternative narrowband approach exists which gives more reasonable component values. It relies upon capacitive, inductive, or magnetic, coupling of parallel resonators and is suitable for filter bandwidths of 20

percent or less. Minimum filter bandwidth is limited primarily by resonato Q and acceptable filter insertion loss. Of the three possible coupling configurations the capacitively coupled version is the most common due to its economy and ease of manufacture.

Several references are available to guide the design of capacitively coupled resonators but one of the most straightforward approaches is given by Williams. Nodal Q's and coupling coefficients for a wide variety of filters including Butterworth, Tscnebyshev, and Bessel filters are listed in tabular form. Component values are found by frequency and impedance scaling of these values. The process is best illustrated by an example.

The design starts with the desired filter Q.

$$Q = \frac{fo}{BW}$$

fo = filter center frequency

BW = filter 3dB bandwidth

Nodal inductors and capacitors are found next.

$$L = \frac{Z}{2\pi fo Qn} \qquad C = \frac{1}{(2\pi fo)^2 L}$$

Z = filter impedance

qn = nodal Q (from tables)

The coupling capacitor C_{12} is found by

$$C_{12} = \frac{k12\ C}{Q}$$

k_{12} = coupling coefficient (from tables)

The total capacitance at each node must equal the nodal capacitance. In a two pole filter the shunt capacitor equals the nodal capacitance minus the value of the coupling capacitor. Working through the equations for a two pole Butterworth, 60 MHz filter gives the filter shown in Figure 5a. The filter bandwidth is 20 percent.

From this point the filter can be impedance and frequency scaled without affecting its percentage bandwidth. A fourfold capacitor value reduction will double the filter frequency and impedance just as before (Figure 5b). Combining this filter with the previously designed L-Match network gives a constant percentage bandwidth filter tunable from 60 to 120 MHz. This filter is shown in Figure 5c.

The inductors are rather small but still entirely feasible for small diameter air wound coils. Accurate repeatable coils can be wound using commonly available machine screw threads as winding forms. (For details see the article by Anderson listed at the end of this paper). Alternatively the inductors can be made larger, and the capacitors made smaller, by raising the 50 ohm filter impedance to something higher with a pair of broadband transformers.

Implementation

Substituting varactors for the variable capacitors in Figure 5c produces a voltage tuned filter. In principal only three varactors are required for a two pole bandpass filter; one coupling capacitor and two tuning capacitors. However, the coupling capacitor is much smaller than the tuning capacitors so two different types of varactor diodes must be used. Moreover, the varactor capacitance variation and tuning curves must match exactly. Finding two different varactors each having the correct capacice and identical tuning curves is very difficult.

A more reasonable approach is to choose a varactor for the coupling capacitor and obtain the larger tuning capacitance by placing a number of varactors in parallel. This way precise tracking between the coupling and tuning varactors is insured although the ratio between the tuning and the

coupling capacitors is limited to integer values. Pole to pole and unit to unit tracking is also improved since varactor variations tend to average out across the group.

For the filter in Figure 5c the ratio between the tuning and the coupling capacitance is almost seven to one. Nearly perfect tracking is possible using one varactor for the series coupling capacitor and seven varactors for each shunt capacitor. The BB-109 varactor which has a capacity of 8.8 pf at 15 vdc and 35 pf at 2 vdc is suitable.

The number of varactor diodes required can be reduced by manipulating the filter to reduce the shunt to series impedance ratio. Tapped inductors can be used to increase the size of the coupling capacitor, or decrease the size of the shunt capacitors. The tap can be located anywhere along the coil, however, a centertap providing a four to one impedance transformation is physically convenient. The capacitors scale directly with impedance so a four to one transformation increases (or decreases) the affected capacitors by a factor of four.

The series coupling capacitor can also be increased with a Pi to Tee conversion. First form a Pi network consisting of the series capacitor and a portion of the two adjacent shunt capacitances. Then convert this network into a Tee increasing the value of all three capacitors in the process. Design equations are given in Figure 6. Choosing equal values for C_1, C_2 and C_3 increases all the capacitors by a factor of three.

Intermodulation for Performance

The use of series opposed diodes is often suggested to reduce intermodulation distortion. This configuration makes it impossible for the applied RF to force either diode into conduction. In addition, the RF voltage applied to each diode is cut in half. Large amounts of distortion will be generated if a varactor is driven into conduction but in low power filters the dominant distortion mechanism appears to be RF modulation of the varactor tuning voltage. This effect is most pronounced at low varactor voltages where the slope of the varactor tuning curve is large and the tuning voltage is small.

One test with a single pole varactor tuned filter gave an input third order intercept of +10 dBm. Replacing the single varactor diode with a pair of series opposed diodes (total of four varactors) increased the third order intercept by six dB. The tuning voltage was two volts in both cases. Intermodulation distortion decreased rapidly as the tuning voltage was increased. Best intermodulation performance is obtained by keeping the filter impedance as low as possible, avoiding low varactor tuning voltages, and using series opposed diodes.

Tuning Range

Filter tuning range is essentially the square root of the usable varactor capacitance range with octave tuning requiring a four to one capacitance variation. Several factors tend to limit the available tuning range. At the high frequency end stray capacity can significantly limit the maximum filter frequency. At the low frequency end intermodulation performance is degraded and the filter insertion loss may increase.

A simple varactor equivalent circuit consists of a variable capacitor in series with a fixed resistor. When the varactor capacitance is small as it is at higher tuning voltages the resistor makes up a small portion of the overall device impedance and the varactor Q is high. Decreasing the tuning voltage decreases the varactor reactance without greatly affecting the series resistance. The result is decreased varactor Q and increased

filter loss at low tuning voltages. Whether the filter loss actually increases or not depends upon the bandwidth of the filter and the Q of the filter inductors.

Despite these effects octave range filters are easy to build and wide capacitance range varactors such as the Motorola MVAM-125 make filters tunable over at least two octaves possible although perhaps not easy. Needless to say wider tuning ranges require better varactor tracking and greater attention to stray capacitance and inductance.

Frequency Range

Filters below one megahertz are possible although the number of varactors required might be excessive. Increasing the filter impedance helps at the expense of increased inductor size and reduced intermodulation performance.

In the UHF region filters to at least 500 MHz are possible. At these frequencies the filter inductors become very small, the effects of component lead and package parasitics become apparent, and finding suitable varactors is difficult. As before the filter impedance can be increased to reduce the inductor problem but the improvement that can be achieved is limited by the effects of stray capacitance. Careful circuit layout is very important and reducing the tuning range to less than an octave helps.

The maximum practical frequency of these filters is an interesting question. Microstrip and other transmission line techniques come to mind but transmission line inductors have the undesirable property of turning into capacitors if the frequency is doubled. With careful design and construction useful filters with limited tuning ranges might be possible well above one gigahertz.

Summary

The design of voltage tuned lowpass and constant percentage bandwidth filters can be summarized as follows.

- Choose filter type, tuning range, number of poles and impedance.
- Determine initial impedance transformation N needed at the low frequency end of the filter tuning range.
- Design L-Match networks using N obtained above.
- Use tables to design the filter section. Use capacitively coupled resonators to implement narrowband bandpass filters. Filter impedance at the low end of its tuning range is N times 50 ohms in most cases.
- Select fixed padding capacitors to equalize tuning capacity ratios in the matching and filter sections then merge matching and filter varactors. Absorb stray capacitance into the padding capacitor.
- Manipulate filter impedance using tapped inductors or a capacitance Pi to Tee conversion to obtain an integer ratio between shunt and coupling capacitance using a minimum number of varactors.
- Use series opposed varactors and low filter impedances to minimize intermodulation distortion.

References

Anderson, Leonard H., "Self-Supporting Coils", Ham Radio Magazine, July 1977.

Williams, Arthur B., Electronic Filter Design Handbook. McGraw-Hill Book Company, New York, 1981.

Zverev, Anatol I., Handbook of Filter Synthesis, John Wiley and Sons, Inc. New York, 1967.

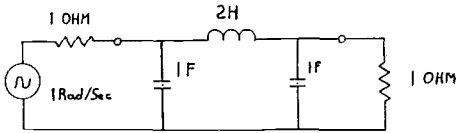
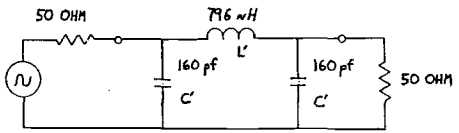
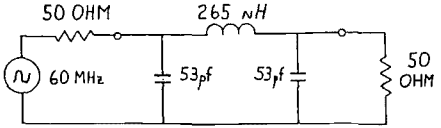


Figure 1a
Butterworth Lowpass Filter Prototype
3 pole, 1ohm, 1 Radian/Second

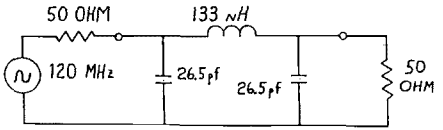


$C' = \frac{C}{2\pi f Z}$ $L' = \frac{L Z}{2\pi f}$ where L and C are prototype values

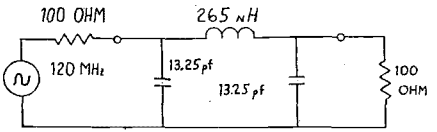
Figure 1b
Butterworth Lowpass Filter
3 pole, 50 ohm, 20 MHz



2a 60 MHz, 50 OHM

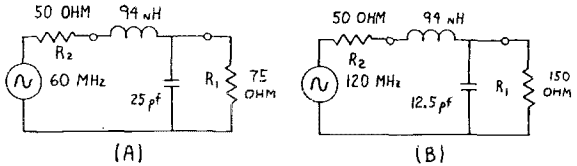


2b 120 MHz, 50 OHM



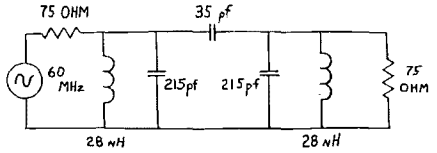
2c 120 MHz, 100 OHM

Figure 2
3 Pole Butterworth Lowpass Filters

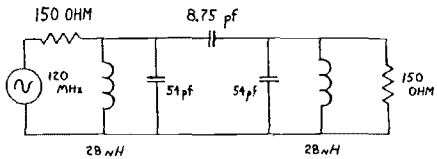


$$X_L = \sqrt{R_1 R_2 - R_2^2} \qquad X_C = \frac{R_1 R_2}{X_L}$$

Figure 3 L-Match Networks



(A) 60 MHz, 75 OHM



(B) 120 MHz, 150 OHM

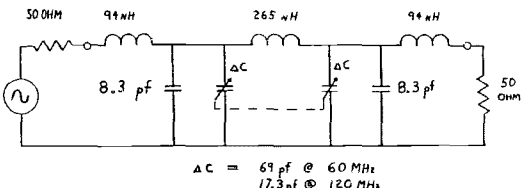
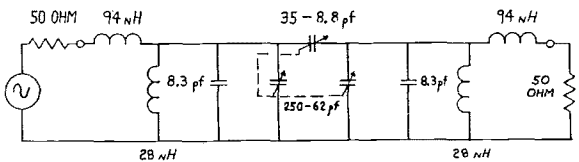
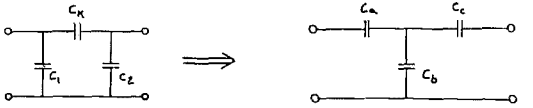


Figure 4 Tunable Lowpass Filter 60 to 120 MHz



(C) 60–120 MHz, 50 OHM

Figure 5 Bandpass Filters



$$\Sigma C = C_1C_2 + C_2C_3 + C_KC_1$$

$$C_a = \frac{\Sigma C}{C_1} \qquad C_b = \frac{\Sigma C}{C_K} \qquad C_c = \frac{\Sigma C}{C_2}$$

Figure 6 Capacitor PI to TEE Conversion

RF Design Evaluation Made Easier Through Automated Control

by
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With the advent of work stations for more efficient product development, attention now turns to the task of adequate design and product testing. The manufacturing environment offers an excellent automated testing solution which can readily be applied to the engineering development laboratory. This solution is based around the IEEE 488 general purpose interface bus (GPIB). The following discussion will take the reader through an introduction to GPIB, common definitions and specifications, and an outline of criteria for selecting a GPIB instrument. In addition, specific RF design examples will be given to emphasize the enhanced testing capability and efficiency. A series of programs are included in the appendix for reference in setting up similar test and evaluation procedures.

The manufacturing environment has experienced automation for many years. This began with the first assembly lines and continues to be a driving factor for economical production facilities. Industrial societies have learned that automation is an essential requirement for an efficient, as well as high quality operation.

In the past ten years that mind set has found a niche in the development engineering laboratories. We've graduated from mechanical pencils, to hand held calculators, to sophisticated work stations and CAD/CAM development. The impellent for this transition was much the same as for the manufacturing floor. The need was crucial to shorten the development time without risking the quality of the product or incurring undue liabilities by putting a product on the market without adequate testing. In addition, our country is experiencing a shortage of experienced design engineers on top of the rising cost of an engineering education and the rapid rise in starting salaries for new graduates. These factors all call for a new methodology for producing quality products, at a low cost, and even lower development cycle time.

It is easy to see why the application of automated testing has moved into the engineering development laboratory to become a permanent fixture. New design test and characterization can benefit from the same efficiency as manufacturing by utilizing equipment containing automated testing features. Design verification can be made at each level of the product before the finished item is complete, thus saving the need for costly corrections and redesigns. The savings in time and personnel is obvious. Yet, there are other subtle areas where integrated automated testing during product development can have an impact. There is a great potential for a higher quality of work and increased productivity by reducing the tedium and length of tasks; such as harmonic characterization in a particular design. Design documentation becomes easier and an additional confidence in the design is obtained through the ability to repeat the same tests for verification. Essentially, most user error attributed to test methodology can be eliminated.

Current automated design tools for the electronics world are usually inefficient in terms of data bases or are not compatible or applicable.

Therefore, the question now becomes "Where are these automated test features available?". The answer is simple, "They are already here - just look for them out in your production facility and bring them into the lab". The General Purpose Interface Bus available on many pieces of test equipment provides the ability for this automated testing. In the engineering lab, it offers one of the best methods for characterizing a new design A GPIB instrument allows the creation of an application specific data base with a minimum amount of pain. Visualize some of the advantages to performing the following characterizations through an automated means: phase noise, output level accuracy and flatness, frequency settling time and switching speed, spurious and harmonic response. All of these are available now and actual test setups and programs for some of these applications will be given in this discussion.

Let's pause a moment and take a look at GPIB and what it has generically to offer. The GPIB is a communications protocol specified by IEEE 488 "Standard Digital Interface for Programmable Instrumentation". You may have also heard of Hewlett-Packard's version called HPIB. The general purpose interface bus allows the remote transmission of an ASCII data string which simulates the front panel operation of an instrument. Each instrument is assigned an address over the bus and is then polled when activated. This allows for multiple addressing of several identical instruments which are used for the same purpose or provides the means to daisy chain different pieces of test equipment. In comparison, the RS-232 interface requires a specific hardware data port at a host computer or concentrator for each piece of interfacing equipment.

GPIB communicstion has been available since 1975 and highly accepted and supported since 1978. It provides a digital data exchange at rates of 1M byte per second in a byte serial, bit parallel format. The IEEE 488 specification provides a means for standardizing the mechanical interface, the electrical interface, and the bus communications protocol that is the signaling of data ready, data accepted, etc. As of this date no standard is provided for the codes and formats which are used to represent the instrument's front panel operation. A subsection of the IEEE P-981 Committee called TAPIS (Transportable Architecture for Programmable Instrument Systems) is trying to standardize on the codes that GPIB instruments understand. A published document on their recommendations will probably not be available for another year as they were scheduled for completion Mid 1986 and have not yet reached that milestone. For now, the format of codes is instrument dependent. In some cases, a specific manufacturer may use the same codes and formats for all of their products. In any event, it is the instrument dependent qualities of GPIB application which make the selection of test equipment critical. This interface is tantamount to the successful transition of the automated test from the manufacturing to the development environment.

Aside from the decision to employ automated testing through GPIB there is a bit of system design which must be completed in order to produce the test setup. The system will require the device under test, the GPIB test equipment, and a system/test controller. The test equipment involved must be capable of either receiving external communication, transmitting information, or both. In GPIB lingo, these qualities are referred to as listen and talk.

A device that listens is capable of receiving data over the common bus when and only when it is addressed. Examples of these devices are programmable signal sources, programmable power supplies, printers, and "dumb" display devices. A device that talks is capable of transmitting data over the common bus under the same addressing conditions. Examples of talkers are frequency counters and tape readers.

Some instruments include labeling on the back of a piece of test equipment that will give the equipment's specific level of GPIB intelligence. Be careful, not all instruments can both talk and listen. The HP 8656 A or B signal generator, for example, is a listen only device. Unfortunately, decoding the GPIB label may be difficult if it is not properly documented or if a copy of IEEE 488 is not readily accessible.

For a quick overview of what to look for, take the example of the Wavetek 2500 signal generator. It has complete source and acceptor capability (*SH1, AH1*), is a basic talker and listener (*T6, L4*), has extended modes of talk and listen disabled (TE0, LE0), has complete remote/local (RL1), device clear (DC1), and device trigger (DT1), and service request (SR1) capability. It has the parallel poll (PP0) and controller (C0) options disabled. E2 designates the type of electrical interface as one using tri-state drivers as opposed to open collector (E1) drivers.

In addition to the talk and/or listen capability of the test equipment, the system will require a GPIB controller. The controller will specify the talkers and listeners on the bus and regulate the data flow and access. Most controllers will also provide a means of programming test sequences to further increase throughput. Usually, this programming will be in BASIC or a BASIC related form for universality.

There are several sources of controllers in the current marketplace. The traditional form is an independent, dedicated instrument with keyboard entry and some sort of display feedback. Wavetek, Tektronix, and Hewlett-Packard all make this sort of GPIB controller. With the wide acceptance of IBM PC compatibles there are several companies producing plug-in boards for P.C.s to perform the IEEE 488 interfacing. In many cases, this can also be accomplished through an RS-232 to IEEE 488 converter. National Instruments and IOTech manufacture such equipment which allows the user to tap off of computer resources currently in house.

A good application of the PC type arrangement is a custom integrated workstation consisting of an IBM PC with a GPIB interface card communicating with an HP 8753 Network Analyzer with S parameter test set and the design under test. Using GPIB and Touchtone software the device under test can be fully characterized.

There is little specific advice for selecting a controller. The basic guidelines of cost, ease of use, longevity, and compatibility, as used in any capital expenditure, should be taken under consideration. Efficient usage of equipment provides a strong case for selecting a PC based product for integration as a controller. The drawback to be aware of for this application is the speed of execution. The PC products are notoriously slower than dedicated controllers which can be a distinct hinderance in the ATE environment.

As alluded to briefly before, it is in those areas, unregulated by the IEEE standards, which make the selection of automated test equipment critical. It is the area of codes and formats that exhibits the least amount of standardization. As each piece of test equipment has its own set of codes and formats, the user is essentially learning a new language developed specifically to talk to that equipment. The language should offer a consistent methodology for replicating the front panel operation of the instrument. The codes should be easy to remember through the use of mnemonics with the restrictions of being neither too cryptic nor too verbose. As an illustration, look at the specification of frequency, RF output level, and AM using the HP 8901A modulation analyzer and the Wavetek 2500 signal generator.

HP 8901	Wavetek 2500	Specification
M5	FRQ	frequency
R2	dBm	suffix for RF output level
M1	IAM	AM, the 2500 has internal AM (IAM) and external AM (XAM)

Though both offer a simplified mnemonic for the specified front panel input, there are no memory clues provided in the 8901 code.

More than a simplified code is needed to adequately convey the meaning of the front panel operations across the GPIB bus. The code should provide for a variety of numeric input formats such as engineering suffixes (MHz) and exponents (E6). Flexibility should be allowed in the syntax of the programming e.g. the use of space characters should not be restricted. In selecting a GPIB instrument, remember, the user will have to be learning a new programming language. To reduce the learning curve time, that language should be as close to normal conversant engineering terms as possible.

Some instruments have accomplished the task of providing a user friendly interface with a technique called minimum uniqueness formatting. This means that each command entry (front panel function) can be represented by a minimum number and sequence of alphanumeric inputs. As long as the user includes those minimum characters in the required order, any version of the command can be accepted. The minimum format may be consistent for all entries, such as a three character mnemonic, or it may vary. If the only command available starting with the letter F is frequency, then the minimum representation of a frequency input may be the single initial letter. Using the minimum uniqueness philosophy, F, FRQ, FREQ, FRQCY, FREQUENCY may all be employed to request a frequency command. In addition, an instrument with this type of coding will usually allow any combination of upper or lower case letters.

After formatting the command portion of the GPIB message, there is a requirement for formatting the numeric entry and termination of the message. Fortunately, there is a defacto standard for all of this data entry, pioneered by Tektronix. Tek codes and formats are specified under Tektronix Standard 962-1780-01 and cover the device dependent message coding for all Tektronix GPIB controllable products. As the IEEE standard is not yet available, any instrument advertising that they conform to Tek codes and formats will be the closest to following a standard as there is today.

Tektronix presents a great amount of detail on the formatting of a basic message unit. There are several building blocks which are combined as required for each message. The code representing the front panel command key is termed a header. With a header there may be an argument which can be either a numeric entry, such as a frequency setting, or a character entry, such as commanding "RF ON". Each message is completed with a terminator which may be an end of message designator such as carriage return / line feed or it may be a concatenation terminator indicating that there is another message on the same line. The diagram below illustrates a typical message string.

HEADER sp NUMERIC ARGUMENT sp SUFFIX sp TERMINATOR

The spaces in all areas except between the header and first argument are optional. The following examples are actual code input for the Wavetek 2500. They illustrate both the minimum uniqueness format and the methods of building a complete message string.

Frequency 500.00 MHz; LVL 300 mV; RF ON cr lf

IAM 50%; FRQ 123 B6; Level 500 B-9; STB 5 lf eoi

The semicolon is used as a message delimeter and the end of string terminations are actually control characters and are not actually printed.

Aside from the friendliness of the user interface, choosing a GPIB instrument should also include an evaluation of supplementary functions. These are commands which are available to the GPIB user but are not accessible from the front panel of the instrument. One of the biggest advantages is remote error reporting. A GPIB user may be able to receive RF error feedback from the instrument in more detail and in a more obvious manner than the local user. Indications such as FM over deviation, loop unlocked, and carrier unleveled can be communicated across the bus as soon as they occur and in "plain English" terminology. Error reporting may also include syntactical errors as related to the GPIB input e.g. Header Error, and system and communications errors. Additional enhancements such as service requests from the instrument to the bus controller and executing a group of commands simultaneously may also be available.

The concerns outlined above are basically software driven. There are other areas to be aware of when selecting a GPIB instrument which are more hardware related. Two rather simplistic ones involve setting the address of the instrument and the end of string identifiers. If these items are assigned via a hardware switch in the GPIB instrument further investigation as to the location and accessibility of the switch is needed. A software override of the address and termination may also be provided.

Some unobvious pitfalls may be present in the actual digital architecture of the GPIB instrument under consideration. If a single processor is controlling all instrument functions, the speed of execution may be relatively slow. This will effect both the GPIB responsiveness and the RF output. If the instrument uses two separate processors for control, specifically separate processors for the front panel operations and GPIB communications, there is a possibility of master/slave contention. Care should be taken to determine which side has execution priority so that the maximum throughput can be obtained.

In addition, a GPIB processor will need to have its clock running at

all times in order to detect its address from the bus. This clock will induce noise throughout the instrument. How the manufacturer handles the area of RF immunity to this clock noise is another critical point.

The actual GPIB interface to the BUS can be controlled through a single dedicated chip. This relieves the instrument software from the handshaking tasks. Several devices are currently on the market to handle this communication. Yet, some of those do not conform to the IEEE 488 standard nor can they handle the higher data transmission rates now prevalent in today's technologies. In those cases, data can actually be lost. Another pitfall is the existence of ghost interrupts through the BUS communication device. These are timing related problems where the controller is faster than the interface device used in the instrument being controlled. The interface device can miss critical communication signals due to its inability to handle the transmission rates.

In summation, there are critical areas to research in choosing a GPIB instrument which involve both software and hardware. The most evident area, though, is that of the user interface. The user is essentially employing three different languages when implementing an automated test setup: the language of the test instrument (individual codes and formats), the language of the controller, and the language of the control program. Choosing a system which will reduce the learning curve in any of these areas will be a great asset.

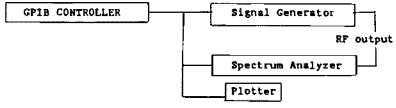
Now that you have completed a crash course on selecting and setting up a GPIB system, here comes the fun part. What can you actually do with this information?

For the GPIB novice, the appendix includes a walk through program demonstrating talk and listen features. This program is written for the HP 9825 controller and the Wavetek 2500 signal generator. It shows the combination of controller language and instrument specific language which a user would have to implement to achieve GPIB communication.

A typical example of an efficiency improvement through GPIB usage is the characterization of harmonics as related to the carrier in an RF design. This is a task which is exceedingly tedious to do under manual conditions. Typically, a system under test would be connected to a spectrum analyzer. The user would manually change the source frequency and "eye-ball" the occurrence of harmonics and spurs. Of course, it was easier if one knew where to look in frequency range and in level. By automating this sort of test, no previous knowledge of the circuitry is needed. A purely objective search can be made across the frequency band and a recording can be produced showing all power occurrences. The same test could be repeated at several temperature ranges to characterize the loss in the attenuators due to increases in temperature. Spikes or drops could be easily located emphasizing the phase relationships between various oscillators. All of this could be plotted and permanently stored in a period of 15 minutes. Factors such as allowing settling time for the signal generator can be included in the controlling program insuring the most accurate data possible.

The sketch below illustrates the test set up for harmonic characterization of the Fluke 6060A signal generator. Included in the appendix are plots of the results at varying temperatures.

The use of this type of program was exceedingly beneficial in determining whether or not the generator met its rated specifications.



Using the same setup, automated testing can be used to determine the frequency switching time of a new design. The following two plots show the responsiveness of the Wavetek 2500 during its initial design stages. The signal generator is rated at a switching speed of 200 ms, +/- 100 Hz of final value in CW and for changes greater than 10 kHz in FM mode, with a typical speed of 100 ms. To prove the initial design, GPIB testing was used to determine, plot, and record the switching speeds across critical bands. This exercise was extremely beneficial in pointing out both the high performance areas, as seen in the switch completed in approximately 50 msec, and the areas which required refinement. Such characterization can assist not only the design groups but can emphasize design superiority in a sales or marketing arena. A picture is worth a thousand words as the saying goes. Those pictures, proving technical superiority, are easily generated using GPIB test procedures in the engineering lab. The program used to generate the switching time evaluation is also included for your reference in the appendix.

The last example to be presented is no more complex in test procedures or setup as the previous illustrations, but does encompass a more critical RF design area, that of phase noise characterization. As the local oscillator phase noise will affect the overall performance of a receiving system, obtaining an accurate analysis of the receiver system is highly critical. In a manual mode, this measurement is time consuming and highly vulnerable to human error. In an H.P. application note (270-2) the recommendation is to use a narrow resolution bandwidth and perform eight sweeps, collecting data by hand at specified offset frequencies. All of these functions can be efficiently programmed and controlled through the use of the GPIB and a programmable spectrum analyzer. Using the programmable features of the analyzer will provide the opportunity to determine the phase noise sideband envelope over a wide frequency range. This is done by selectively avoiding discrete signal points.

The last series of charts in the appendix shows a thorough evaluation and comparison between Fluke, HP, and Marconi signal generators with respect to upper sideband phase noise.

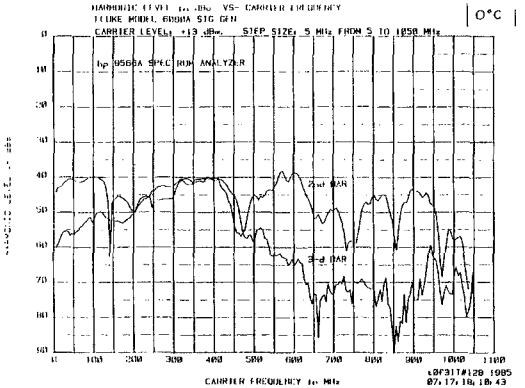
Again, the use of test equipment with GPIB can be seen as a very valuable design development tool. It can be employed both in technical market definition, such as the comparison of competitive equipment, and in design definition and evaluation. GPIB in the engineering lab increases both the credibility of the data and the efficiency in obtaining that data. Certainly, RF design testing can be made easier through automated testing procedures.

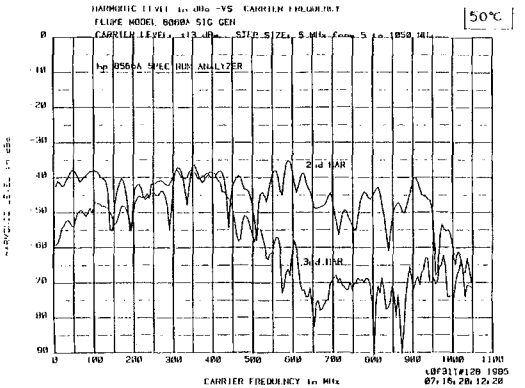
ACKNOWLEDGEMENT

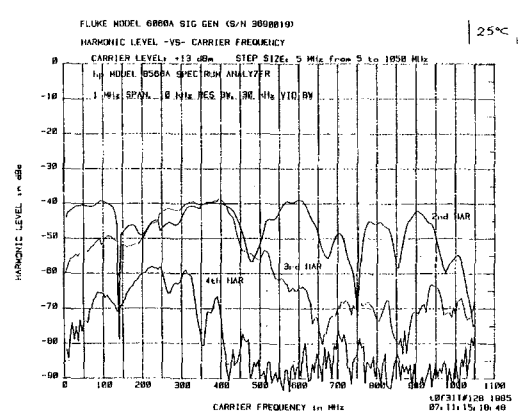
I would like to thank Bill Kennedy, Engineer, Wavetek Indiana, Inc. for his contribution of application programs and plots.

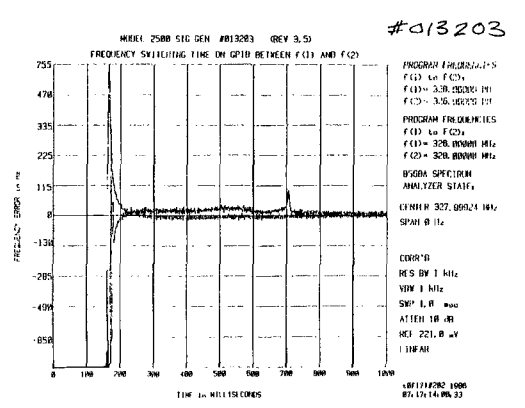
SMM

```
0: "LISTEN 4 TALI ROUTINE on 2508";
1: "tj4@"tk20C 204u@B";
2: trk 1;idl 8
3: dim M$[3],O$[3],R$[40]
4: "GPIB address";dev "sg",702
5: "Time delay ms";500)w
6: cl; ?
7: wait W
8: "Enable SRQ";wrt "sg","RQS ON"
9: wait W
10: gsb "RQS"
11: gsb "SELECT"
12:
13: "FRQ";+xd 5
14: ent "Enter FREQUENCY in MHz",F
15: wrt "sg","FRQ "&str(F)&" MHz"
16: wrt 0,"FRQ "&str(F)&" MHz"
17: wrt "sg","FRQ?"
18: gsb "Read"
19: gsb "SELECT"
20:
21: "LVL";+xd 2
22: ent "Enter OUTPUT LEVEL in dBm",L
23: wrt "sg","LVL "&str(L)&" dBm"
24: wrt 0,"LVL "&str(L)&" dBm"
25: wait W
26: wrt "sg","LVL?"
27: wait W
28: gsb "Read"
29: gsb "SELECT"
30:
31: "MOD";+xd 2
32: ent "Enter: IAM, IFm, XAM, or XFM",M$
33: if M$="IAM" or M$="iam" or M$="XAM" or M$="xam":gsb "AM"
34: if M$="IFM" or M$="ifm" or M$="XFM" or M$="xfm":gsb "FM"
35: dsp "SELECT KEY or Press CONTINUE";stp
36: gto "RTE"
37:
38: "AM";+xd 1
39: ent "Enter AMPLITUDE MODULATION in %",M
40: wrt "sg",M$," "&str(M)&" %"
41: wrt 0,M$," "&str(M)&" %"
42: wait W
43: if M$="IAM":wrt "sg","IAM?"
44: if M$="XAM":wrt "sg","XAM?"
45: wait W
46: gsb "Read"
47: ret
48:
49: "FM";+xd 2
50: ent "Enter FM DEVIATION in kHz",M
51: wrt "sg",M$," "&str(M)&" kHz"
52: wrt 0,M$," "&str(M)&" kHz"
53: wrt "sg",M$&"?"
54: wait W
55: gsb "Read"
56: ret
57:
58: "RTE";
59: ent "Enter 1000 or 400 for MOD RATE",A
60: wrt "sg","RTE "&str(A)
61: wrt 0,"RTE "&str(A)
62: wait W
63: wrt "sg","RTE?"
64: wait W
65: gsb "Read"
66: gsb "SELECT"
67:
68: "MOD OFF";
69: wrt "sg","IAM 0%;IFM 0 kHz;XAM 0%;XFM 0kHz"
70: wait W
71: wrt "sg","MOD OFF"
72: wrt 0,"MOD OFF"
73: wait W
74: wrt "sg","MOD?"
75: wait W
76: gsb "Read"
77: gsb "SELECT"
78:
79: "RF";
80: ent "Enter ""ON"" or ""OFF"" for RF state",O$
81: wrt "sg","RF "&O$
82: wrt 0,"RF "&O$
83: wait W
84: wrt "sg","RF?"
85: wait W
86: gsb "Read"
87: gsb "SELECT"
88:
89: "SET?";
90: wrt "sg","SET?"
91: wait W
92: gsb "RQS"
93: for I=1 to 10
94: red "sg",R$
95: wait W
96: dsp R$;wait 1e3
97: next I
98:
99: "ID?";
100: wait W
101: wrt "sg","ID?"
102: wrt 0,"ID?"
103: wait 1e3
104: gsb "RQS"
105: for I=1 to 2
106: red "sg",R$
107: wait W
108: dsp R$
109: wait 1e3
110: next I
111:
112: "HELP?";
113: wrt "sg","HELP?"
114: wrt 0,"HELP?"
115: wait 1e3
116: gsb "RQS"
117: for I=1 to 2
118: red "sg",R$
119: dsp R$;wait 1e3
120: next I
121:
122: dsp "END of ROUTINE";beep;stp ;gto +0
123:
124: "Read";
125: wait W
126: red "sg",R$
127: wait W
128: red "sg",R$
129: dsp "Press CONTINUE for READ string";stp
130: dsp R$;stp
131: ret
132:
133: "SELECT";
134: dsp "SELECT USER KEY or CONTINUE";stp ;ret
135:
136: "RQS";
137: rds(7))A;wait W
138: if bit(7,A)=0;gto +2
139: if bit(6,rds(702));wait W;gto -3
140: ret
141:
142: "KEY LIST";
143: "+0: FRQ";
144: "+1: LVL";
145: "+2: MOD";
146: "+3: RTE";
147: "+4: MOD OFF";
148: "+5: RF";
149: "+6: SET?";
150: "+7: ID?";
151: "+8: HELP?";
*25021
```

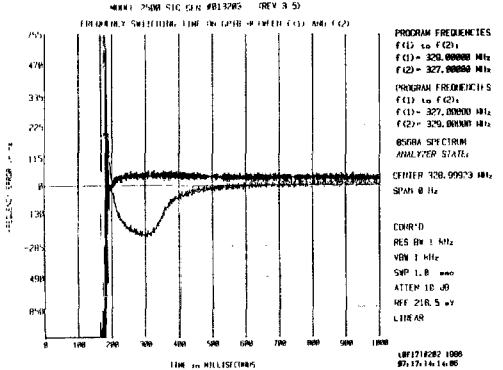

0°C
HARMONIC LEVEL -VS- CARRIER FREQUENCY
FLUKE MODEL 6000A SIG GEN
CARRIER LEVEL: +13 dBm STEP SIZE: 5 MHz FROM 5 TO 1050 MHz
hp 8568A SPEC RUN ANALYZER
2nd HAR
3rd HAR
HARMONIC LEVEL in dBm
CARRIER FREQUENCY in MHz
10F31T#128 1985
07:17:18:18:43


50°C
HARMONIC LEVEL -VS- CARRIER FREQUENCY
FLUKE MODEL 6000A SIG GEN
CARRIER LEVEL: +13 dBm STEP SIZE: 5 MHz from 5 to 1050 MHz
hp 8568A SPEC RUN ANALYZER
2nd HAR
3rd HAR
HARMONIC LEVEL in dBm
CARRIER FREQUENCY in MHz
10F31T#128 1985
07:16:20:12:20


25°C
FLUKE MODEL 6000A SIG GEN (S/N 3090019)
HARMONIC LEVEL -VS- CARRIER FREQUENCY
CARRIER LEVEL: +13 dBm STEP SIZE: 5 MHz from 5 to 1050 MHz
hp MODEL 8568A SPEC RUN ANALYZER
1 MHz SPAN 0 Hz RES BW 30 kHz VID BW
2nd HAR
3rd HAR
4th HAR
HARMONIC LEVEL in dBm
CARRIER FREQUENCY in MHz
10F31T#128 1985
07:11:15:10:40


#013203
MODEL 2588 SIG GEN #013203 (REV 3.5)
FREQUENCY SWITCHING TIME ON GPIB BETWEEN F(1) AND F(2)
PROGRAM FREQUENCIES
F(1) to F(2):
F(1)= 328.000000 MHz
F(2)= 328.000000 MHz
8568A SPECTRUM
ANALYZER STATE:
CENTER 327.999924 MHz
SPAN 0 Hz
CORR'D
RES BW 1 kHz
VBW 1 kHz
SWP 1.0 sec
ATTEN 10 dB
REF 221.8 mV
LINEAR
FREQUENCY ERROR in Hz
TIME in MILLISECONDS
10F17T#282 1986
07:17:14:09:33

#013203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f(2)= 327.00000 MHz
PROGRAM FREQUENCIES
f(1) to f(2):
f(1)= 327.00000 MHz
f(2)= 329.00000 MHz
8568A SPECTRUM
ANALYZER STATE:
CENTER 328.99973 MHz
SPAN 0 Hz
COMP'D
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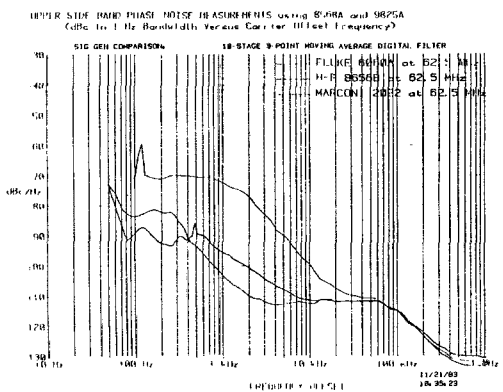
VBW 1 kHz
SWP 1.0 sec
ATTEN 10 dB
REF 218.5 mV
LINEAR
TIME in MILLISECONDS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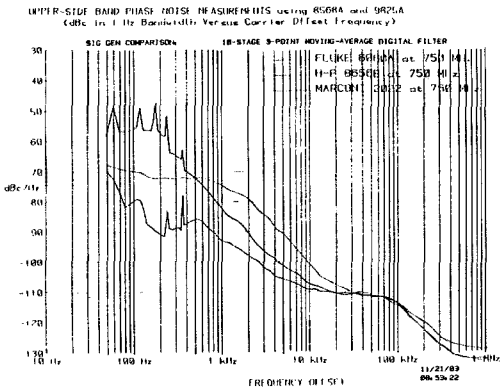
(dBc in 1 Hz Bandwidth Versus Carrier Offset Frequency)
SIG GEN COMPARISON
10-STAGE 9-POINT MOVING-AVERAGE DIGITAL FILTER
FLUKE 6010A at 62.5 MHz
H-P 8656B at 62.5 MHz
MARCONI 2042 at 62.5 MHz
dBc/Hz
11/21/89
08:55:23


UPPER-SIDE BAND PHASE NOISE MEASUREMENTS using 8568A and 9825A
(dBc in 1 Hz Bandwidth Versus Carrier Offset Frequency)
SIG GEN COMPARISON
10-STAGE 9-POINT MOVING-AVERAGE DIGITAL FILTER
FLUKE 6010A at 750 MHz
H-P 8656B at 750 MHz
MARCONI 2042 at 750 MHz
dBc/Hz
10 Hz
100 Hz
1 kHz
10 kHz
100 kHz
11/21/89
08:53:22
FREQUENCY OFFSET

OOK, FSK, and PSK Data Receivers Using an AM-FM Receiver IC

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Abstract

The Sprague ULN2241A and ULN3840A ICs are designed to be used in consumer AM-FM radios. They contain all the necessary functions for a complete AM tuner plus the FM IF and detector. With a few simple changes in the recommended circuitry, they can be used in a wide variety of low cost crystal controlled or synthesized OOK (carrier is amplitude modulated or turned on and off by the data), FSK (carrier is shifted in frequency by the data), and PSK (carrier is shifted in phase by the data) data receivers. The range of data rates is almost unlimited because the IF frequency is not limited to 455 kHz and the inclusion of an internal mixer and regulated supply means that in many cases, the complete unit can be built with a few coils and an unregulated supply.

ULN2241A and ULN3840A

Block diagrams of the ULN2241 and ULN3840 are shown in Figures 1 and 2 respectively. The two ICs are essentially identical in performance except that the latter has more features and therefore more pins. The one exception is that the ULN2241 provides an AGC output from pin 10 in the FM mode which goes from 5V to 0 as the input signal increases. The ULN3840, on the other hand has a DC output from pin 15 which increases with the input signal level and goes from 0 to about 4 volts in both the AM and FM modes. Other features unique to the ULN3840 are an AFC output, a mute signal, and a mute input pin.

Typical radio receiver circuits using these two ICs are shown in Figures 3 and 4. Note that the complete AM tuner is contained in the IC and only the tuned circuits need to be added. The AM local oscillator is a negative resistance type and is internally connected to a low-noise balanced mixer. A very important feature of the ICs is that the AM and FM IF amplifier are common and use the same transistors. Each stage of the IF amplifier is down 3 dB at about 30 MHz, and there are four stages. This differs from most combination radio IC's which have different IF sections for AM and FM and the AM section is usually designed not to have much gain above 455 kHz. Since they are common in the ULN2241 and ULN3840, the IF out pin is common for both modes and the detector coils must be connected to feed the FM and AM detectors. In this application, the AM detector coil is a short circuit in the FM mode, and the 22 uH coil feeds the FM quadrature detector coil. Because a quadrature detector is a phase detector with one input connected internally to the IF output and the other connected to the quadrature coil, it can also be used, as we shall see later, as part of a phase

detector in both FSK and PSK demodulation.

The frequency range of operation of the mixer is from audio up to about 100 MHz and although the mixer is designed to work only in the AM mode, it can be turned on in the FM mode by connecting a bias resistor from the reference voltage to the mixer bias pin (12 on the ULN2241 and 15 on the ULN3840). The mixer works quite well at 100 MHz if a buffered signal is fed to the oscillator input port, and it will handle input signals up to about 30 mV without significant crossmodulation, but in the AM mode the internal oscillator gives up at about 30 MHz. A stable internal regulated voltage is available from pin 9 on the 2241 or 13 on the 3840. If this voltage is used for other circuits in the receiver which require a regulated voltage like an oscillator, then the unit can be built to operate from an unregulated supply. (The current drawn from the regulator should not be more than about 2 mA.) The input impedances to the mixer and IF amplifier are quite high at the lower frequencies, and so it is possible to accommodate a wide variety of RF or IF filters.

The mute output pin of the ULN3840 can be used to drive the internal mute when in the FM mode so that noise is not present at the output when no carrier is being received. It can also be set up to mute if there is a tuning error and the mute signal could also be fed to the data processing circuits to indicate a loss of carrier or a signal too small for reliable reception.

OOK Data Receivers

Personally, I do not like the term OOK because the carrier may not be completely off because of leakage. AM seems to be a more appropriate term with the ON/OFF ratio being specified.

AM modulation is not used very often in data transmission, because of claimed susceptibility to errors, but this seems to be grounded in the belief that AM radio has more static than FM. In fact, AM requires a S/N (power ratio) of only about 18.5 dB for a BER of 10E-9 (1). AM is also very easy to generate by simply gating the RF signal on and off, and it occupies much less bandwidth than FSK. A 20 dB S/N is not difficult to guarantee in cable systems and bandwidth might be an important factor in these cases. (2) The only restriction here is that the receiver IC has an internal AGC system, so it is better to operate the system with the carrier normally on and the data signals turning it off. The number of data signals in succession which turn the carrier off must be limited depending on the time constant selected for the AGC or the IC gain will increase until it reaches its maximum gain condition.

Figure 5 shows a 14.5 MHz AM data receiver using a crystal controlled external oscillator. The AM local oscillator coil is replaced by a 100 Ohm resistor to prevent it from oscillating due to the internal negative resistance. The IF

frequency in this case is 4.5 MHz and was selected as a compromise between image rejection and available coil Q to produce the desired IF selectivity. Note that the internal detector has not been used here. This is because the data rate for this receiver is up to 38 KBPS and the internal detector is designed for audio use. At lower data rates, the internal detector can be connected to an external comparator. Other possibilities might be a diode detector and comparator.

The AGC time constants are set by the capacitors on pins 16 and 12 with the one on pin 16 being the most important. If the carrier is always on and long strings of data are to be sent, the capacitor on pin 16 can be made larger. If fast attack for the AGC is desired, it can be made smaller.

If higher data rates are desired, a wider bandwidth filter can be used. A 10.7 MHz ceramic FM IF filter will allow data rates up to about 140 KBPS. If the data rates are low, a 455 kHz IF can be used but this may require dual conversion to achieve the desired spurious response rejection.

It should be pointed out that the occupied bandwidth of AM data signals is only two times the data rate. The occupied bandwidth of FSK signals is approximately 2(data rate)+ 2(frequency shift) so that this data receivers which can handle 140 KBPS in the AM mode would handle only about 65 KBPS in an FSK mode with a frequency shift of 75 kHz.

FSK Data Receivers

Grounding pin 16 of the ULN2241 or 1 of the ULN3840 puts it into the FM mode. As was mentioned above, the mixer is off in this mode, but as was mentioned earlier, it can be turned on by connecting a resistor from the reference voltage to the mixer bias pin. In the ULN2241, this resistor can instead be connected to the AGC voltage on pin 10 so that the mixer gain is reduced as the signal level increases. Figure 6 shows a 49 MHz FSK receiver using an external crystal oscillator and comparator to produce the output pulses. Unlike in the AM case, there is no limit on how long the data can stay in the 0 or 1 state. This particular data receiver uses a 10.7 MHz FM receiver IF filter and will operate up to about 50 KBPS. Current 10.7 MHz FM receiver IF filters such as the Murata SFE 10.7 ML or Toko CFSD have excellent group delay response and cause very little pulse distortion.

The FM detector is a standard quadrature detector and when it is correctly tuned at the center frequency, the output from pin 5 is the same DC voltage as the reference voltage on pin 9. In the ULN3840, the AFC output pin can also be used if a load resistor is connected from pin 7 to pin 13. The reference voltage can then be used as the other input to the comparator.

An alternative to this arrangement is, of course, the Motorola MC 3356 which has been specifically designed as an FSK data receiver.

PSK Data Receivers

PSK modulation is capable of low error rates in the presence of noise (1) and occupies a bandwidth only equal to twice the data rate (6), but the circuitry is complex and there are restrictions on the data format because of the phase ambiguity problem. One solution for polled systems was mentioned in another paper (4) and other schemes are presently used for telephone data receivers. (Polled systems are those in which a number of receivers are polled in sequence.) The most common solution for RF data receivers is to use a phase-locked-loop with a very narrow bandwidth for demodulation. In any case, the ULN2241 and ULN3840 have many of the necessary components for constructing the loop (3). Figure 7 shows a PSK demodulator which uses the phase detector in the ULN2241 for the loop and an external MC1496 phase detector to detect the 180 degree phase changes. The VCO locks up at 90 degrees from the signal at the IF output on pin 8 of the ULN2241, and the IF output is shifted 90 degrees by T10 and applied to the MC1496. Thus the ULN2241 contains the Q detector and the MC1496 the I detector. The output of the I detector is fed through a low-pass filter to a comparator to produce the output data.

The Q or loop phase detector consists of the quadrature detector components in the IC, and the audio output pin, pin 5, is the phase detector output. The phase detector constant for the ULN2241 and ULN3840 is 3.8 volts/radian. The internal impedance at the audio output pin is about 900 ohms so R1 is added together with R2 and C to form a passive loop filter. If the ULN3840 is used instead, the AFC output could be used, and the load resistor from pin 7 to 13 could be R1 of the loop filter. The AFC output is a current source with a detector constant of about 700 uA/radian. The oscillator constant, Ko, for this circuit is 577e3 radians/sec/volt, so the loop frequency of this design is 1 kHz.(5) This is a relatively narrow band loop, but it still will have a problem with data pulses over about 200 microseconds long;(5) When the carrier changes phase 180 degrees, the loop tries to follow it, and if the carrier stays at 180 degrees long enough , the VCO will lock on to the 180 degree carrier. If the VCO changes only 90 degrees, the role of the two phase detectors is reversed and the data will be lost. Thus, the length of the data pulses must be restricted or some means must be found to accommodate longer ones. A common solution is to build a very narrow-band loop and use a crystal-controlled VCO to keep it very close to the center frequency so that lock-up can be achieved in a reasonable length of time.

Conclusion

It has been shown that low-cost RF data receivers can be built with integrated circuits commonly used for consumer AM/FM radios, and their operating frequencies are not limited to the broadcast frequencies. Almost any range of data rates and type of modulation can be accommodated, and in many

cases, very few external components are required. In particular, the Sprague ULN2241A and ULN3840A are exceptionally good for this application because of the wide frequency response of their internal mixer and IF stages and features like AGC drive, signal strength indication and mute input and output.

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Figure 1 ULN2241A

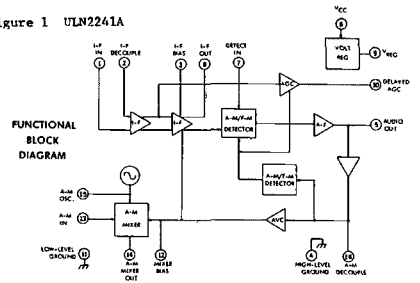
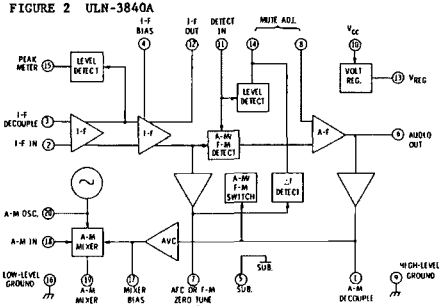


FIGURE 2 ULN-3840A



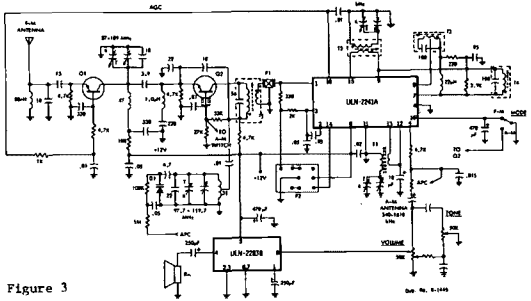


Figure 3

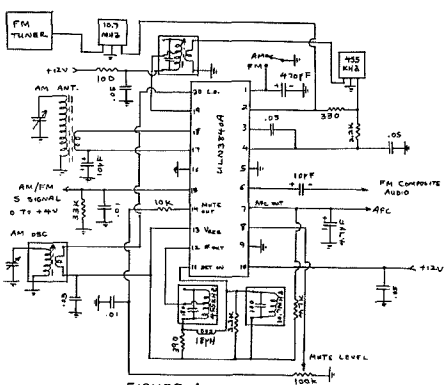


FIGURE 4

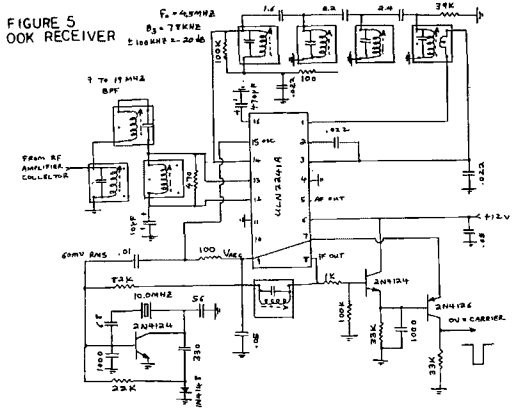


FIGURE 5
OOK RECEIVER

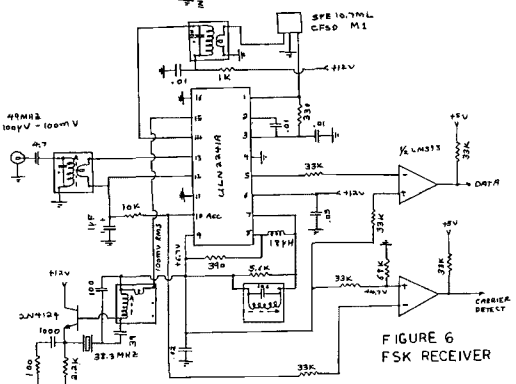


FIGURE 6
FSK RECEIVER

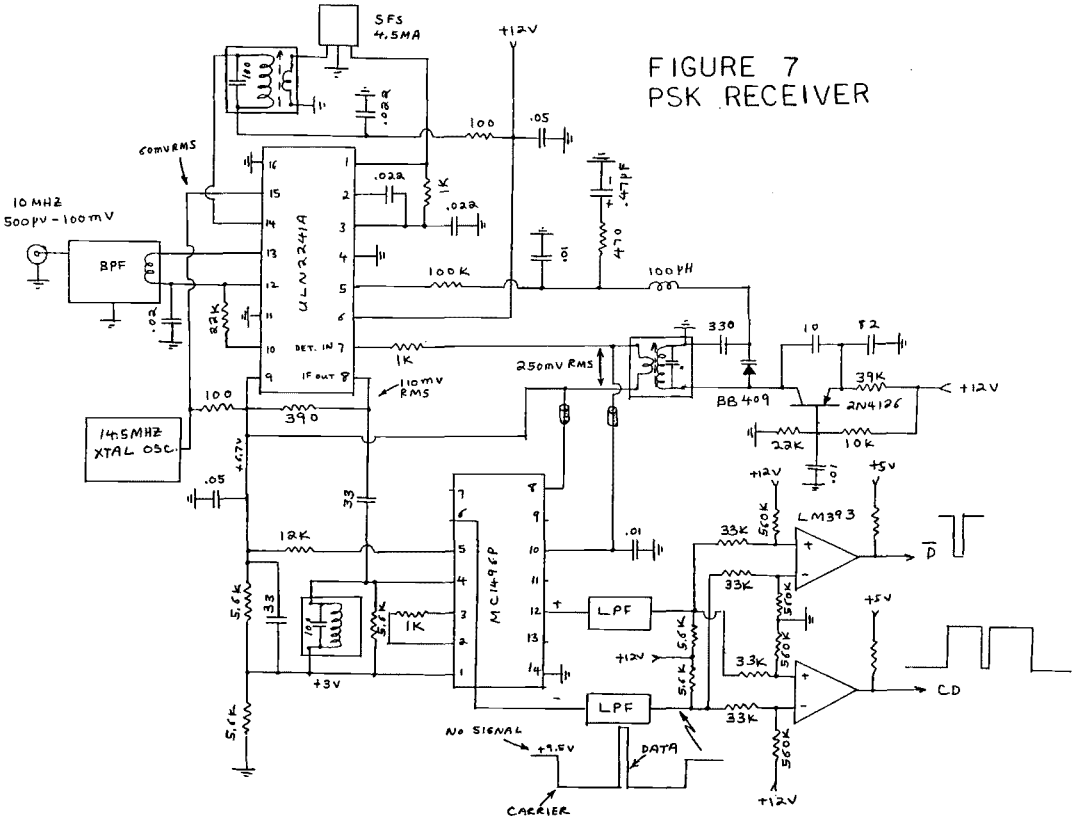


FIGURE 7
PSK RECEIVER

A THICK FILM HYBRID TRANSMITTER FOR CELLULAR TELEPHONE

by

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Introduction

Rapidly growing markets of cellular telephones are demanding smaller lighter and cheaper radiotelephones. To fulfill these demands manufacturer have to search new production techniques also for the radio units of the cellular telephones. This paper describes the design and performance of a thick film hybrid transmitter. Thick film technique was selected, because it is cheaper and more suitable for mass-production than thin film technique. The frequency range of the transmitter is from 890 MHz to 915 MHz.

The design of the power amplifier is based on measured S-parameters and large signal impedances of the transistors and equivalent circuits of passive components. The analysis and optimization of the matching circuits was done using computer, because the same work done manually would be an overwhelming task.

Measurement of S-parameters was done using an automatic network analyser. Large signal impedances were measured with conventional pull-load method and equivalent circuits of passive components were measured using HP 4191A impedance analyser and the least squares fitting method.

Properties of class A and B power amplifiers

For power amplifiers , the output current is either in the cutoff region or saturation region during a portion of the input signal cycle. This leads to the classification of power amplifiers into three modes of operation: class A, B and C. When the output current flows during the whole input signal cycle, the amplifier is called class A amplifier. If the output current flows only during the half of the input signal cycle, the mode of operation is B and if the output current flows less than half of the input signal cycle the amplifier is called class C amplifier.

The class of operation of the transistor amplifier has significant effect on available gain and efficiency. Figure 1 shows the variation of efficiency and maximum output power as a function of operation mode and conduction angle.

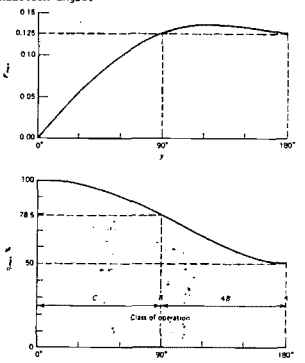

Figure 1. Efficiency and power output of power amplifier /1/.

The gain of the transistor decreases if the bias point of the transistor is transfered from class A towards class B, while efficiency increases. Both of these parameters determine also the total efficiency of whole amplifier. The first stage of the power amplifier operates usually in class A, because this class gives the highest gain and power level is relatively low so the efficiency in this case is not of major importance. The last stages operate on high power level and efficiency has to be as high as possible without sacrificing the gain of the transistor. For this reason in the UHF frequency range class B is usually chosen as good compromise between gain and efficiency.

Amplifier design

The target specifications for hybrid amplifier were 23 dB gain with 2 W output power and 12 V supply voltage in 890-915 MHz frequency range. This leads to three amplifier stages when the average gain of each stage is 7-8 dB. The operation classes of the stages were A, B and B for optimum total efficiency.

Class A amplifier can be considered a linear amplifier and the theory of linear two ports can be applied directly to the design of matching circuits of the transistor. The small signal S-parameters are not useful for class B amplifier design , because it operates in nonlinear region. In this case the design of the matching circuits is based on large-signal impedances which can be measured using conventional pull load method.

Manufacturers usually give the typical values of S-parameters for packaged transistors. However, in hybrid circuits transistors are bonded on a substrate in chip form. This structure is different from packaged transistor and S-parameters mentioned in data sheet are not valid anymore.

S-parameters for the first stage transistor were measured using automatic network analyser and three point calibration method, which uses short circuit, 50 ohm load and open circuit as reference impedances. The test jig is shown in figure 2 and reference impedances in figure 3.

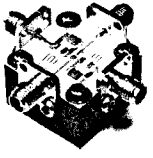

Figure 2. S-parameter measurement jig.

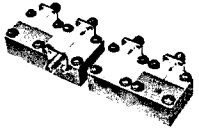

Figure 3. Reference impedances for three point calibration.

The nonidealities of the network analyser are eliminated by computer, which calculates the correction factors for measured S-parameters and writes out the corrected values on paper or to mass-storage media like floppy disk. These parameters can be used directly to the design of the matching circuits without any kind of peeling process, because reference planes were selected to be on the connection point of the transistor bonding wires.

As previously mentioned, a power transistor can be described in terms of the large-signal source and load impedances required to produce a given output power and gain. A typical measuring system for large-signal impedances and power measurements is illustrated in figure 4.

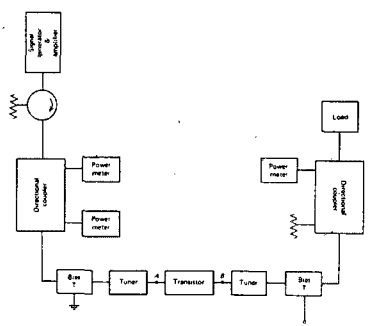

Figure 4. Measuring system for large-signal impedances /3/.

Tuners used in this measurement system were coaxcial stub tuners. The input tuner was adjusted until reflected power was zero and output tuner was adjusted for given output power level. After the transistor was properly tuned for given power level , the transistor was disconnected from the test setup and the impedances at the reference planes A and B looking toward the generator and toward the load were measured with a network analyser. The conjugates of these impedances represent the transistor's large-signal input and output impedances, respectively. These impedances are functions of output power level, frequency and bias conditions. For this reason the transistor has to be measured in those conditions where it is intended to be used.

Matching circuits consist of microstriplines and ceramic chip capacitors. In spite of the small size of the chip capacitor its equivalent circuit contains small series inductor, which means that the capacitance is a function of frequency. For accurate computer analysis the equivalent circuit of the capacitor has to be measured.

The capacitance was measured with HP 4191A impedance analyser as a function of frequency . The equivalent circuit of the capacitor, which consists of inductor and capacitor in series connection, was fitted to the measurement results, using least squares fitting method. The total capacitance can be written in form

$$\frac{1}{C_{tot}} = \frac{1}{C} - \omega^2 L \qquad (1)$$

where C and L are the values of the equivalent circuit.

This equation is of quadratic type and coefficients C and L can be solved using quadratig regression analysis.

The basic structures of the matching circuits were designed using immittance chart. The starting values were optimized with computer using APLAC program /2/. This program is intended for the linear analysis of the microwave circuits, but also matching circuits for nonlinear transistor stages can oe designed when the input and the output ports of the transistors are treated as passive impedances (large-signal impedances). Today there is more powerful programs commercially available than APLAC. Most widely known programs are probably Touchstone and Super-Compact.

Construction

The circuit was printed on 0.635 mm thick alumina substrate using gold and resistor pastes. Metallized holes were made printing gold on both sides of the substrate. Chip transistors were bonded to the substrate with conductive epoxy and gold wires using ultrasonic bonding. After this the substrate was fixed to the heatsink with conductive epoxy and the whole circuit was connected to the test jig. The construction of the transmitter is shown in figure 5 and the test jig is illustrated in figure 6.

Measured performance

The manufactured amplifier was measured in 890 - 915 MHz frequency range with 10 mW input power and 12 V supply voltage. The measured gain of the amplifier is shown in figure 7. The amplifier achieves 22 dB gain and 1.5 W output power.

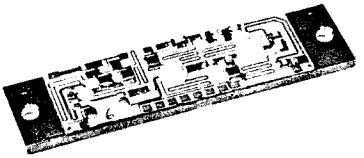

Figure 5. The manufactured hybrid transmitter.

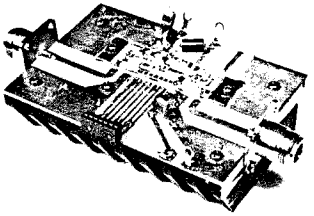

Figure 6. The test jig of the transmitter.

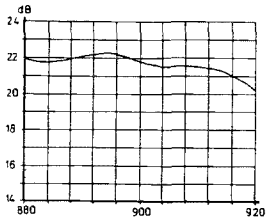

Figure 7. The gain of the amplifier.

Conclusion

The aim of this paper is to investigate possibilities to realize UHF power amplifier with thick film techniques. This technique was verified to achieve acceptable performance in this frequency range if low losses and sharp outlines of the microstrip are not required.

Acknowledgement

The author wishes to express his gratitude to professor Veikko Porra of Helsinki University of Technology. Discussions with professor Porra have been very useful during this work.

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DESIGN: A Program for the Automated Synthesis of Broadband Matching Networks between Complex Terminations

by

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I. ABSTRACT: DESIGN - A Program for the Automated Synthesis of Broadband Matching Networks between Complex Terminations

A computer program has been written that performs the truly automated synthesis of precision, broadband, gain-sloped, lumped-element or distributed-parameter matching networks between complex sources and complex loads. The algorithm is based upon the real-frequency technique, which requires, as essential data, only a table of values for the source and load impedances, along with a set of desired values for the transducer gain function of the equalizer at a number of frequency points.

The program proceeds virtually automatically to the realization of the matching network once the data file has been read and a degree for the equalizer has been selected. This is in contrast to previous efforts, where the user had to provide special initial solutions, particular error-function weights, and other detailed information in order to obtain convergence of the design algorithm.

The capabilities of the algorithm have been verified in many different matching-network design examples. Some of these examples have been taken from the literature, and, in each such case, the program has been able to meet or

exceed the efficiency and performance of the previously published designs.

The program runs on IBM PC/XT/AT® and compatibles as well as on HP-series desktop computers.

II. INTRODUCTION

A. The Methods and Capabilities of DESIGN

DESIGN performs the truly automated synthesis of precision, broadband, gain-sloped, lumped-element or distributed-parameter matching networks - also referred to as equalizers - between complex sources and complex loads.

1. The Advantages of DESIGN's "Real-Frequency" Technique

The essential part of the synthesis method used in DESIGN is based upon the work of Carlin and Komiak [1]. Their method, also known as the real-frequency technique, has been shown to produce matching networks that are "simpler in structure and superior in frequency response to equal-ripple designs" [2] based upon the classical approaches of Fano [3] and Youla [4] as developed by Chen [5] and Mellor [6]. Furthermore, the real-frequency technique requires only a simple numerical description of the source and load as necessary data for the synthesis. The design process can proceed automatically once the source and load has been so described. On the other hand, the classical approaches require, as a preliminary task, the construction of equivalent circuit models for the source and load, and then require substantial designer interaction to perform such tasks as parasitic absorption and impedance scaling via the Norton/Kuroda transformations. To the best of our knowledge, DESIGN is the only commercially available program that employs Carlin and Komiak's superior real-frequency technique for matching network synthesis.

2. DESIGN: What It Does

DESIGN synthesizes lossless matching networks to provide a specified magnitude response (Sm21) across a frequency band between a complex source impedance and a complex load impedance. The program user must first construct a data file containing (1) the source and load data, and (2) the desired values for Sm21 at a number of frequencies points which define the passband. The user interactively inputs the name of the data file and the desired degree of the network once the program starts executing. DESIGN then proceeds with

only a small amount of user interaction after this point, although certain default options may be reset, if desired, during the synthesis process.

The design procedure is based on a lumped, shunt-capacitor, series-inductor, lowpass topology, with an optional shunt-inductor at the load end of the network providing a bandpass response, if so desired. The program indicates which topology is most appropriate for a given set of source and load data, and the program user has the option to follow this suggestion or not. The allowable circuit structures are capable of handling virtually any set of matching network design requirements.

3. DESIGN: Single Matching Problems

The real frequency technique was developed in somewhat different ways for the "single-matching" case, i.e. a real source and a complex load, and for the "double-matching" case, i.e. a source and load which are both complex. The method for single-matching has been described in [7]. Basically, the method involves: (1) constructing a piecewise linear function of frequency, R(f), as an initial approximation to the real-part of the matching network impedance at the output port; (2) optimizing R(f) so that the network, if it could be realized exactly from R(f), would provide the prescribed gain shape across the passband; (3) constructing a rational approximation to R(f); and (4) realizing and optimizing the final circuit. Our enhancements to the original Carlin-Komiak algorithm include the automation of the design process and the optimization of the final circuit.

4. DESIGN: Double Matching Problems

At least two different methods have been developed previously to match complex sources to complex loads [8], [9], [10]. In each case a difficult optimization problem must be solved to yield the final circuit. To obtain convergence, the user must first generate a good initial guess to the solution.

DESIGN's method for solving the double-matching problem is a direct extension of the approach to single-matching. The presence of complex sources and complex loads is accommodated by performing a relatively easy optimization on a preliminary design of the network. This initial design is produced automatically by the program.

The technique begins with the conversion of the double-matching problem to one which initially involves only single-matching. This is done by resonating the source impedance with either a series-inductor or a shunt-capacitor so that the source impedance becomes purely real at one frequency. The synthesis then proceeds on the presumption of a purely real source, constant with frequency across the passband, and the given complex load. Hence this part of the design process is identical to the single-matching case. After this preliminary network is designed, the actual complex source is reintroduced,

and the network is optimized to meet the original design goals. The optimization proceeds quickly and efficiently to a solution since (1) we start from a comparatively good initial guess obtained in our preliminary design; and (2) we use an optimizer specially developed by us to handle this kind of circuit problem.

B. The Efficacy of DESIGN's Single- and Double-Matching Algorithms

DESIGN has been able to duplicate, if not exceed, the quality and efficiency of the networks designed by any of the other single- or double-matching synthesis algorithms. It should also be noted that while DESIGN goes through a sequence of intricate steps to realize the desired matching network, the user need not be familiar with the details of the techniques, because the program proceeds automatically, with very little input from the user. The program does indicate what it is doing at any given moment, and various parts of the program may be interrupted and re-executed, as desired, with different values for the defaults.

III. DESIGN SAMPLE SESSION: DOUBLE-MATCHING

A. The Data File Format for Double-Matching

The rules for constructing the file are as follows.

The first line of the data provides the following information:

1. The nature of the matching problem - C indicates complex-source to complex-load;
2. How the source is described - Z for impedance values, Y for admittance values, or S followed by a corresponding reference resistance for reflection coefficient values;
3. How the load is described - Z for impedance values, Y for admittance values, or S followed by a corresponding reference resistance for reflection coefficient values; and
4. How the desired gain for S21 is specified - A for absolute magnitude, and D for decibels.

Each subsequent line gives, for each frequency,

1. The frequency in Hertz, followed by
2. The values for the source (real and imaginary parts for impedance and admittance, magnitude and phase in degrees for reflection coefficient), followed by

3. The values for the load (real and imaginary parts for impedance and admittance, magnitude and phase in degrees for reflection coefficient), followed by

4. The desired value for S21 (absolute magnitude or dB, as noted above).

Any time an alphabetic character is called for in the first line of the data file, any other symbol may be appended to that character to aid, for example, in the readability of the file. All alphabetic data may be entered in either upper or lower case.

Data entry in the file is entirely free-format; blank lines are allowed anywhere; comment lines are denoted by the single apostrophe (') being the first non-blank character on the line. Furthermore, comments may be appended to the end of any data line. DESIGN will inform the user of most data file errors.

B. Matching a Complex Source to a Complex Load - An Example

Consider a typical microwave transistor amplifier, where the topology is a cascade of transistors and matching networks. We shall consider the design of an interstage matching network that (1) couples the output of one Plessey GAT6 GaAs FET to the input of an identical device, and that (2) provides maximum unilateral transducer gain through the cascade of the equalizer and one of the devices. In other words, we seek an equalizer to provide a prescribed transducer gain function when terminated at the source end by the S22 of the GaAs FET and terminated at the load end by the S11 of the device.

1. The Data File

The data file for this problem could be written as follows, according to the rules of the previous section.

```
'The name of this data file on disk is CEXAMPLO.MCH
'S22 as a source, S11 as a load between a pair of GAT6 GaAs FETs
'First line of data could be written simply as: C  S 50  S 50  D
```

Complex-source	Sparams-for-source 50		Sparams-for-load 50		dB-S21
8e9	.735	-42	.775	-107	-2.71
9e9	.740	-47	.750	-118	-1.84
10e9	.750	-52	.730	-128	-1.16
11e9	.755	-58	.710	-136	-0.515
12e9	.765	-62	.695	-145	0.0

The gain slope of the equalizer was chosen to achieve an overall flat gain shape between the matching network and the terminating transistor, and to obtain the maximum available unilateral gain.

2. Performing the Synthesis

In response to screen queries, we type in the data file name, and then specify a degree of 5 with a lowpass topology. As shown on the next 3 pages, the resistance-excursion optimization proceeds (with all options set to their default values), and we stop it after 12 iterations. DESIGN performs the curve-fitting and final synthesis steps to yield preliminary lumped and distributed circuits, which are seen to furnish a good response at the high end of the band, but whose response degrades at lower frequencies. This is expected as part of our design algorithm. The final optimization is then applied, again in response to screen queries, and the lumped and distributed circuits yield a final response error of 0.46 dB and 0.78 dB, respectively.

IV. CONCLUSION

DESIGN represents what we believe to be the best program available to date for matching network synthesis. The program has been constructed to proceed rapidly and automatically to a circuit realization from a basic set of user-supplied data. The User's Guide for DESIGN, obtainable from us, demonstrates 18 examples of matching network synthesis. In those cases where the examples have been taken from the open literature, the program has been able to meet or exceed the efficiency and performance of the previously published designs.

```
MATCHING NETWORK DESIGN BEGINS:  The Resistance Excursion Optimization

        ... hold down SPACE BAR to interrupt optimization ...

Iteration     Function Evaluations     RMS % Error of |S21|^2 Across Passband
    4                 2                          2.578
    5                 2                          2.445
    6                 2                          2.426
    7                 3                          2.385
    8                 2                          2.238
    9                 2                          2.224
   10                 2                          2.104
   11                 2                          2.028
   12                 2                          1.937
Error function has changed by less than 0.50 percent.
Do you wish to continue optimization?  (Y/N): n

**Convergence Achieved, final summary follows.

   13              2                          1.934

Do you want to RETRY the resistance excursion optimization with different
internal program defaults or do you want to CONTINUE with the design process?

Retry or Continue -- (R/C): c

RESULTS: MATCHING NETWORK ELEMENT VALUES FROM THE COMPLEX SOURCE
                    TO THE COMPLEX-LOAD.

  The Lumped Element Design              The Distributed Element Design

Series Inductor: 1.054E-009 H     TRL: 120.0 ohms,  33.51 deg at 1.000E+010 Hz
Shunt Capacitor: 4.482E-013 F     OST:  25.0 ohms,  35.14 deg at 1.000E+010 Hz
Series Inductor: 3.737E-010 H     TRL: 120.0 ohms,  11.29 deg at 1.000E+010 Hz
Shunt Capacitor: 8.443E-013 F     OST:  25.0 ohms,  32.98 deg at 1.000E+010 Hz
Series Inductor: 4.195E-010 H     TRL: 120.0 ohms,  12.69 deg at 1.000E+010 Hz

Press <cr> to clear the screen and to proceed ...

   A circuit analysis follows ...

Freq. (Hz)    S21 in dB:  Desired   Lumped Design   Distributed Design
----                      -------   -------------   ------------------
8.000E+009                  -2.71         -6.96            -4.75
9.000E+009                  -1.84         -1.93            -0.37
1.000E+010                  -1.16         -0.03            -0.69
1.100E+010                  -0.52         -0.58            -0.69
1.200E+010                   0.00         -0.25            -0.60

Do you want to retry the curve-fitting with new values
for the curve-fit factor or the degree?  (Y/N): n
```

```
      Function Evaluation No.:  188

 Maximum Response Error in dB <=  0.46

Design refinement completed - hit <cr> to continue ...
```

```
RESULTS: MATCHING NETWORK ELEMENT VALUES FROM THE COMPLEX SOURCE
                    TO THE COMPLEX-LOAD.

  The Lumped Element Design

Series Inductor: 1.645E-009 H
Shunt Capacitor: 5.143E-013 F
Series Inductor: 5.426E-010 H
Shunt Capacitor: 8.550E-013 F
Series Inductor: 3.870E-010 H
```

Press <cr> to clear the screen and to proceed ...

NOTE: Maximum response error in Lumped Design is 8.46 dB.

```
   A circuit analysis follows ...

Freq. (Hz)    S21 in dB:  Desired    Lumped Design
----                      -------    -------------
8.000E+009                -2.71      -2.76
9.000E+009                -1.84      -1.38
1.000E+010                -1.16      -1.62
1.100E+010                -0.52      -0.49
1.200E+010                 0.00      -0.45

Optimize the (D)istributed design or (Q)uit - (D/Q): d
Optimization proceeds - hold down SPACE BAR to stop ...

      Function Evaluation No.:  233

 Maximum Response Error in dB <=  0.78

Design refinement completed - hit <cr> to continue ...
```

```
RESULTS: MATCHING NETWORK ELEMENT VALUES FROM THE COMPLEX SOURCE
                    TO THE COMPLEX-LOAD.

                The Distributed Element Design

TRL: 120.0 ohms,   47.59 deg at 1.000E+010 Hz
OST:  25.0 ohms,   36.98 deg at 1.000E+010 Hz
TRL: 120.0 ohms,    9.73 deg at 1.000E+010 Hz
OST:  25.0 ohms,   33.11 deg at 1.000E+010 Hz
TRL: 120.0 ohms,   11.70 deg at 1.000E+010 Hz
```

NOTE: Maximum response error in Distributed Design is 8.78 dB.

Press <cr> to clear the screen and to proceed ...

```
   A circuit analysis follows ...

Freq. (Hz)    S21 in dB:  Desired    Distributed Design
----                      -------    ------------------
8.000E+009                -2.71      -2.74
9.000E+009                -1.84      -1.06
1.000E+010                -1.16      -1.88
1.100E+010                -0.52      -1.24
1.200E+010                 0.00      -0.75

Do you wish to restart the entire design process from the beginning (with
the same load data) or do you wish to quit?

Restart or Quit -- (R/Q): q
```

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DEVELOPING NON-LINEAR OSCILLATOR MODELS USING LINEAR DESIGN TOOLS

Summary

The design of oscillators typically starts from the Class A operating condition and then changes into the large signal range for the semiconductor. The designer has two choices: either to design for highest output power, (highest efficiency) or for lowest noise. Highest output power and lowest noise are not necessarily the same. This paper is a brief summary of requirements towards designing high power low noise oscillators at high frequencies using a dielectric resonator oscillator as an example.

Introduction

A variety of transistor feedback arrangements are possible which lead to building an oscillator. Figure 1 a-c show successful RF topologies. The tuned element is an LC circuit, depending upon the devices, with a grounded emitter, grounded base, or grounded collector circuit is a better choice. The tuned circuit is responsible for determining the resonant frequency and at the same time provides 180° phase shift. The overall performance of the oscillator depends on the Q of the resonator and of the high frequency performance of the semiconductor. By making slight changes in the circuit, a field effect transistor can be used at UHF frequencies and higher, instead of the bipolar transistor. At microwave frequencies, MESFETs are frequently used. In looking at Figure 1-C the capacitor from emitter to ground can be replaced by a series resonant device and therefore obtaining the possibility of using a second tuned circuit. This configuration has been used for designing low phase noise oscillators (1) and if this emitter circuit takes over the burden of the high Q devices, then the other LC circuit is only used as a phase shifter.

In analyzing the semiconductor one obtains the equivalent circuits, Figure 2 and 3, which describe the intrinsic model of the bipolar transistor and the MESFET. For reason of convenience, the model used for the MESFET has has all the elements to describe a HEMPT (high electron mobility transistor). In the past, the dominant nonlinearities have been described in the so-called SPICE model. SPICE is a program that uses non-linear approximation. The computation time is excessive. SPICE programs, including microwave extensions, suffer from the lack of accurate microwave models and do not have any facilities for optimizations. Execution speed of SPICE programs are 1,000 times slower than their linear counterparts. A new method called the Modified Harmonic Balance method has been developed with the key authors being Fred Rosenbaum and Rowan Gilmore (2). This allows the use of SPICE-like models together with linear programs with as little as 1% overhead and taking full advantage of linear optimizers. As a result, transparent linear programs can be designed. This literature (3, 4) provides information on modelling of MESFETs.

Figures 4 and 5 show the large signal equivalent circuits of

the bipolar and the MESFET. One of the best papers on bipolar nonlinearities is the book, Modeling the Bipolar Transistor, by Ian Getreu, published by Tektronix, Inc., Beaverton, Oregon, in 1976, Order #062-2841-00.

In order to maintain information on the large signal handling capabilities during Class C operation, a nonlinear analysis like the one leading to the oscillator amplitude stabilization was calculated. This is shown in the Appendix. While the interested reader can follow the Appendix, for those with less patience, we will assume the following simplifications. The emitter diffusion capacitants

$$C_{ed} = K \cdot I_e/V_t$$

with I_e being the diode current, in our case the emitter current and V_t is the temperature voltage or 26 mV. The emitter diffusion resistor rd = Vt/i_d. These two nonlinearities are related to the emitter current. The depletion layer capacitants are proportional to $\frac{1}{\sqrt{V}}$. Any large voltage or current modulates those elements. It can be shown that the depletion layer capacitants follow the equation C = f(V) =

$$\int_{t=0}^{\infty} f(c)dt = 2 \cdot C$$

The transconductance G_m can be expressed as

$$G_m = \sum_{V=1}^{n} g_V =$$

$$= g_0 + g_1 + g_2 + + + g_n,$$

whereby the first component g_0 is the DC transconductance, g_1 is the transconductance for the basic frequency, and the following are the harmonics.

Translation Into Nonlinearities

Recent publications have mostly dealt with modelling the GAS FET where the translation into large signal parameters is easier based on the fact that the nonlinearities in FETs are somewhat better to describe. Device measurements on the large signal indicate that the most contribution for the nonlinearitles are G_m and Rds, while the other capacitors have smaller contributions. For this paper, I will concentrate on bipolar effects.

As a general rule, bipolar transistors have lower phase noise contribution at high frequencies based on the fact that corner frequency, f_c, which describes the flicker noise contribution is low. For small currents and for power transistors, the following table can be assumed for f_c:

1 mA	=	300 Hz
10 mA	=	1,000 Hz
30 mA	=	10,000 Hz

This noise contribution f_c can be reduced by incorporating a resistor feedback piece in the emitter, but this is done at the expense of efficiency and cut-off frequency following the approximation A = $AO/(1 + R_e \cdot G_m)$. At frequencies above several thousand MHz, the gain band width product of the bipolar

transistors is no longer sufficient to maintain oscillation. Therefore, one has to switch over to MESFETs. The N-channel field effect transistors are useful in oscillators from less than a few MHz to approximately 1,000 MHz. Then bipolar microwave transistors should take over, and above 4-6 GHz MESFETs are the choice.

A convenient way of obtaining large signal parameters for the bipolar transistor is to look at the nonlinear model Figure 4 and to computer optimize the equivalent model Figure 2, by adjusting the nonlinearities as previously indicated by approximately doubling the depletion layer capacities and reducing G_m and adjusting R_{de}.

Fourier analysis can show that the transconductance Gm and the input conductance Re(Y11) can be calculated from the following. The emitter resistance R_e, which has been described by

$$R_e = 26mV/I_e,$$

will be rewritten in the form $R_e = \frac{KT}{qI_e}$ whereby R_e is said to be the small signal emitter resistance which increases with signal level, then the ratios

$$\frac{R_e^*}{R_e} = \frac{\left(\frac{Eq}{kT}\right) J_0\left(\frac{Eq}{kT}\right)}{2 J_1\left(\frac{Eq}{kT}\right)} = \frac{V J_0(V)}{2 J_1(V)}, \quad \frac{C_e^*}{C_e} = \frac{g_m^*}{g_m} = \frac{2 \cdot J_1(V)}{V J_0(V)}$$

whereby E is the peak value of the base emitter signal voltage assume to be given by $E \cdot \cos(\omega t)$. These ratios, expressed in $I_0(v)$ and $I_1(v)$, which are hyberbolic Bessel functions of the first kind of order zero and one are shown in the Appendix. It can be further shown mathematically that the transconductance and the input capacitance get reduced in value as a function of the base emitter drive voltage, while the input resistance increases. The final emitter current is also going to change based to a bias shift as a function of the applied signal voltage following the equation

$$V_{Bias} = \frac{kT}{q} \cdot \ln\left[J_0(V)\right]$$

Finally the peak emitter current using the same hyperbolic function can be expressed as

$$i_C\,(peak) = \frac{I_e\,(mean)\; e^V}{I_0(V)} .$$

Example: Setting the base to emitter drive voltage $\frac{qE}{KT}$ to 2, the value of the transconductance reaches the 3dB point and the input resistance also increases from the relative value 1 to 1.4. This base emitter drive voltage generates an approximate bias shift of $\frac{q\,E}{KT}$ which then results into a ratio of the collector current components relative to twice the mean current of approximately 1.5 for the peak current, .7 for the fundamental frequency component,

.3 for the second harmonic, and less than .1 for the third harmonic.

Our large signal model now can be easily obtained by adjusting the values of the small signal equivalent circuit. As previosuly indicated, the voltage dependent capacitors should be essentially doubled.

Practical Application

The recent trend to develop oscillators with dielectric stabilizers shall be picked up here and our example shall be developed around it. Figure 6 shows the equivalent circuit of a dielectric resonator oscillator. The entire circuit is described in a circuit file for CADEC 4 using the parallel resonator approach for the dielectric resonator. The LCR values have been determined from th definition of physics. The transmission line terminated with 50 ohms is set at quarter wavelengths for best coupling and the transmission line into the emitter of the transistor is set at approximately quarter wavelengths as the parallel resonant condition of the dielectric resonator transforms into approximately 2 ohm resistive output resistance into the emitter of the transistor. The circuit can therefore be redrawn as shown in Figure 7. To meet the requirements for oscillation the combination of internal and external feedback has to provide the necessary phase shift and this oscillator circuit can be made unstable to meet the approximate criteria by optimizing the inductance betwen base and ground while allowing for the resistive feedback in the emitter at large DC currents. This feedback will reduce the gain band width product of the oscillator. Figure 8 shows the measured resonant character of the dielectric of the DRO of the function using an HP8510 network alanyzer. This permits measurement of the Q of the resonator. Figures 9 and 10 show the close-in purity of the oscillator, and Figure 11 shows the single side band phase noise. I will deal with the noise calculation in a future paper. The maximum output power is achieved by matching the output impedance calculated from $P_{out} = \frac{(.9 \times VCE)^2}{2P_{out}}$.

The maximum available output power can be determined from the Fourier coefficient of the fundamental current and the voltage swing across the transistor. The output matching stub guarantees 50 ohms matching. By selecting the feedback properly, superior noise performance can be obtained if matching for best noise figure and best output power is done by adjusting the emitter transmission line lengths slightly offset to the dielectric resonator coupling. CADEC 4 allows one to do such analysis and the details on optimum noise matching will be shown in the following paper. Table 1 shows the circuit listing for the CADEC circuit file. Note the statement NAB, which stands for Noise Analysis Begin; and the #300 refers to the noise temperature of 300° Kelvin. Table 2 shows the listing of the results. Please note that S22 magnitude at 4GHz is approximately 100.

Figure 12 shows a plot of the noise figure and the gain due to the Q multiplier effect, the noise figure gets the unusual curve based on matching for maximum output power rather than best noise figure. Figure 13 shows the noise and gain circles for the circuit configuration chosen.

Conclusion

To predict the output power at microwave frequencies and analyze the phase noise of the oscillator, specifically for MESFETs, more modern techniques like load pulling or Harmonic Balance methods have been developed. It was shown in this paper that by using a somewhat cruder approach for first approximation using bipolar transistors, fairly good understanding of the mechanism is possible. More experimental results and noise theory will be presented in a forthcoming paper.

ULR:jd
0180C (A)
8/14/86

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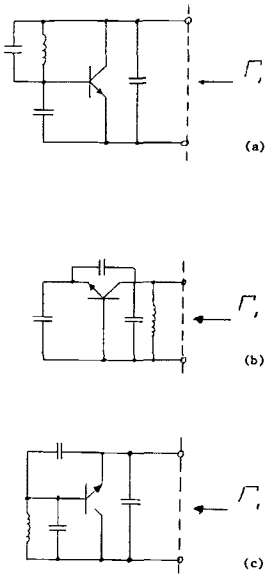


FIGURE 1

A range of possible oscillator circuits.

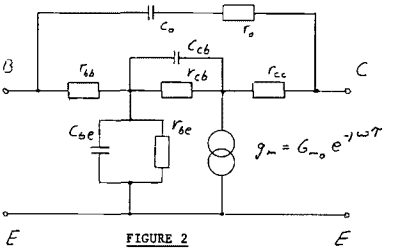


FIGURE 2

Equivalent circuit for a bipolar transiator.

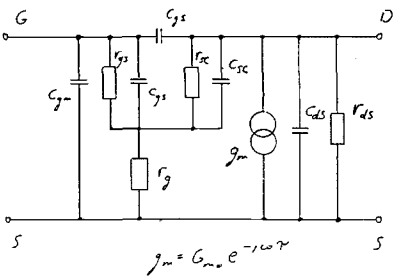


FIGURE 3

Equivalent circuit for a MESFET, including extensions to HEMPT.

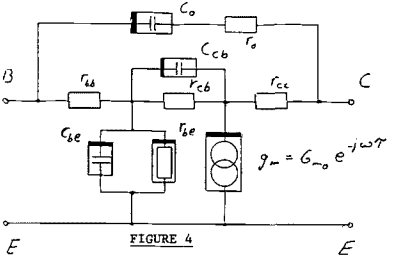


FIGURE 4

Large signal components in the equivalent circuit of a bipolar transistor.

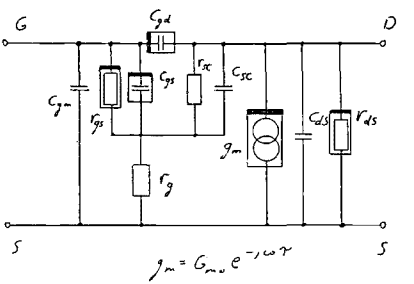


FIGURE 5

Large signal components in a field effect transistor.

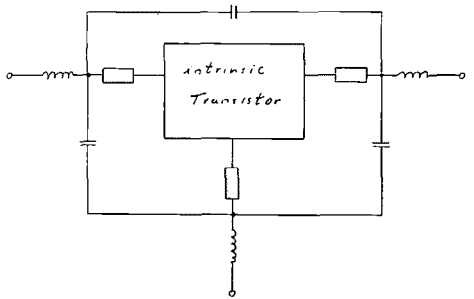


FIGURE 6

Influence of the packaging to the "intrinsic" transistor.

FIGURE 7

Equivalent circuit of oscillator.

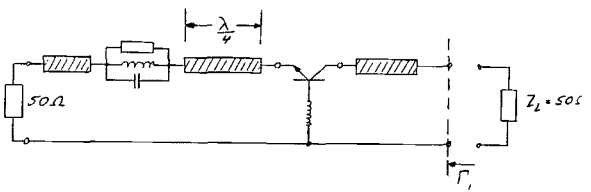


FIGURE 8

Measured response of a dielectric resonator at 4GHz.

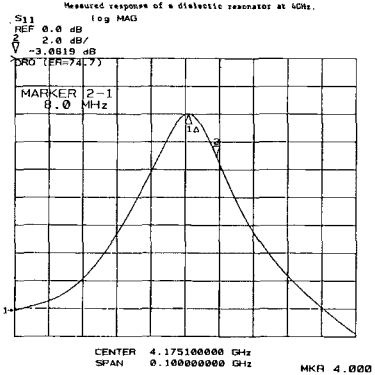
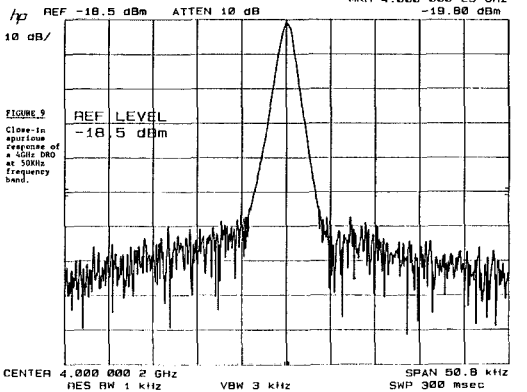


FIGURE 9

Close-in spurious response of a 4GHz DRO at 50KHz frequency band.



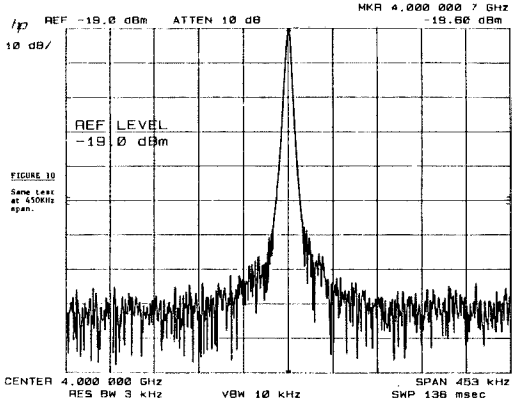


FIGURE 10
Same test at 450KHz span.

FIGURE 11
Single side band phase noise of the oscillator under phase locked condition to improve close-in noise.

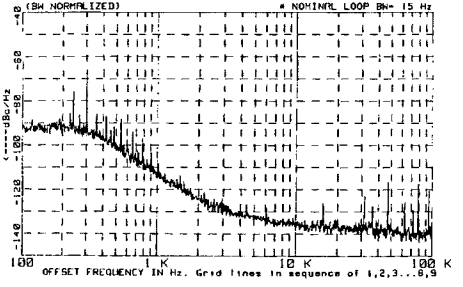


FIGURE 12
Noise and gain as a function of frequency

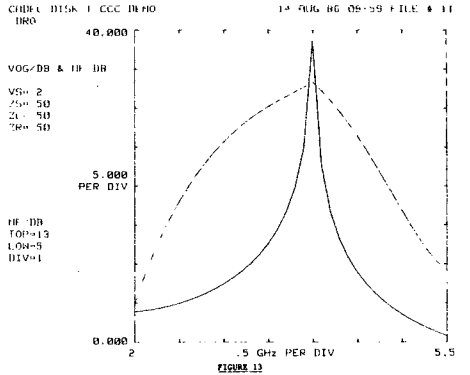


FIGURE 13
Noise and gain circles.

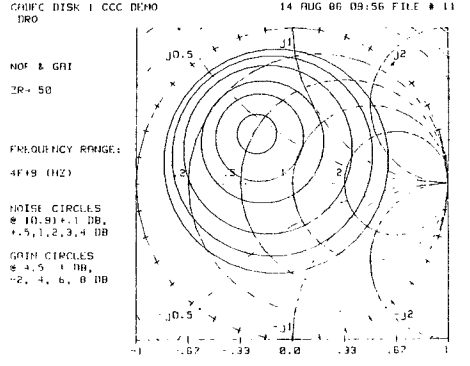


TABLE 1

```
CADEC DISK # 1 CCC DEMO                    13 AUG 86 21:27 FILE # 11
    FRI DRO
  1: SRC              2V  50ohm
  3: TER              50ohm
  4: LFR              2GHz  6GHz  100MHz
     REM  OPT    S22/M =100/1
     REM  SFR              4GHz
  7: NAB              290K
  8: RS               50ohm
     .CON  0  0  1
  9: CAB              .1mm  50ohm
     .CON  1  0  2
 11: LIS              795.774pH  500  4GHz  4GHz
     .CON  2  0  3
 15: CS               19.894pF
     .CON  2  0  3
 16: CAB              17.5mm  50ohm
     .CON  3  0  4
 18: LS               500pH
     .CON  4  0  5
     REM  TRB              20  10GHz  30mA
     OLD R_BIP
     .X16
     .CON  5  6  7
 19: LS               344.01038211lpH(1a/10n)
     .CON  E  0  0
     TWO  1  7
     .OUT VOG/DB   K/M    S22/M   NF/DB
```

TABLE 2

```
Loading OLD R_BIP:,707,0
50HZ_BIP

CADEC DISK # 1 CCC DEMO                    13 AUG 86 21:29 FILE # 11

 DFO
 VS= 2  ZS= 50  ZL= 50  ZR= 50

FREQUENCY/HZ      VOG/DB          K/M          S22/M          NF/DB

   2.0000E9       3.8834      -1.7910        1.3326         5.9668
   2.1000E9       3.9953      -2.0137        1.4080         6.6199
   2.2000E9       4.1620      -2.1896        1.4901         7.1993
   2.3000E9       4.3795      -2.3280        1.5801         7.7163
   2.4000E9       4.6465      -2.4360        1.6795         8.1795
   2.5000E9       4.9639      -2.5186        1.7901         8.5957
   2.6000E9       5.3342      -2.5792        1.9145         8.9703
   2.7000E9       5.7616      -2.6207        2.0557         9.3078
   2.8000E9       6.2517      -2.6448        2.2180         9.6119
   2.9000E9       6.8123      -2.6530        2.4071         9.8858
   3.0000E9       7.4539      -2.6466        2.6310         10.1321
   3.1000E9       8.1902      -2.6265        2.9009         10.3536
   3.2000E9       9.0404      -2.5935        3.2338         10.5526
   3.3000E9       10.0312     -2.5495        3.6561         10.7314
   3.4000E9       11.2015     -2.4922        4.2113         10.8926
   3.5000E9       12.6114     -2.4253        4.9762         11.0387
   3.6000E9       14.3600     -2.3487        6.1014         11.1727
   3.7000E9       16.6285     -2.2629        7.9264         11.2980
   3.8000E9       19.8063     -2.1689        11.4104        11.4184
   3.9000E9       25.0126     -2.0673        20.7047        11.5391
   4.0000E9       38.6398     -1.9590        96.8514        11.6661
   4.1000E9       22.5771     -1.8358        15.4591        11.4400
   4.2000E9       16.6318     -1.6967        7.7296         11.1860
   4.3000E9       13.1829     -1.5457        5.1390         10.9048
   4.4000E9       10.7703     -1.3860        3.8399         10.5977
   4.5000E9       8.9298      -1.2205        3.0571         10.2664
   4.6000E9       7.4540      -1.0518        2.5321         9.9131
   4.7000E9       6.2318      -.8819749      2.1541         9.5410
   4.8000E9       5.1989      -.7129069      1.9660         9.1546
   4.9000E9       4.3061      -.5461834      1.8431         8.7557
   5.0000E9       3.5298      -.3831572      1.4610         8.3644
   5.1000E9       2.8458      -.2249582      1.3101         7.9791
   5.2000E9       2.2411      -.0725551      1.1827         7.6172
   5.3000E9       1.7006       .0733075      1.0733         7.2949
   5.4000E9       1.2156       .2120132      .9782942       7.0313
   5.5000E9        .7783439    .3430991      .8949142       6.8471
   5.6000E9        .3924293    .4662352      .8211659       6.7629
   5.7000E9        .0225103    .5812119      .7555744       6.7975
   5.8000E9       -.3059532    .6879297      .6970482       6.9660
   5.9000E9       -.6058647    .7863035      .5447851       7.2804
   6.0000E9       -.8836193    .8766621      .5992061       7.7519
```

APPENDIX

We mentioned briefly that the oscillator amplitude stabilizes due to some nonlinear performance of the transistor. There are various mechanisms involved, and depending on the circuit, several of them are simultaneously responsible for the performance of an oscillator. Under most circumstances, the transistor is operated in an area where the dc bias voltages are substantially larger than the ac voltages. Therefore, the theory describing the transistor performance under these conditions is called "small-signal theory". In a transistor oscillator, however, we are dealing with a feedback circuit that applies positive feedback. The energy that is being generated by the initial switch-on of the circuit is being fed back to the input of the circuit, amplified, and returned to the input again until oscillation starts. The oscillation would theoretically increase in value unless some limiting or stabilization occurs. In transistor circuits, we have two basic phenomena responsible for limiting the amplitude of oscillation.

1. Limiting because of gain saturation and reduction of open-loop gain.
2. Automatic bias generated by the rectifying mechanism of either the diode in the bipolar transitor or in the junction field-effect transistor. In MOSFETs an external diode is sometimes used for this biasing.
3. A third one would be external AGC, but it will not be considered here

The oscillators we discuss here are self-limiting oscillators.

The self-limiting process, which by generating a dc offset bias moves the operating point into a region of less gain, is generally noisy. For very low noise oscillators, this operation is not recommended. After dealing with the quarter-wavelength oscillator in the preceding section, we will deal here only with the negative resistance oscillator, in which, through a mechanism, a negative resistance is generated due to feedback and is used to start oscillation with the passive device. Here we look at what is happening inside the transistor that is responsible for amplitude stabilization, and we will thus be in a position to make a prediction regarding the available energy and the harmonic contents.

Figure A-1 shows the quarter-wavelength oscillator redrawn in such a way that the source electrode is now at gorund potential while the gate and drain electrode are electrically hot. The reason for doing this is because we will look at the gate-to-source transfer characteristic and use its nonlinearities as a tool to describe what is happening. The same analysis can be applied to a transistor circuit, provided that the resistors used for dc bias are small enough not to cause any dc offset. The field-effect transistor characteristic follows a square law and, therefore, can be expressed as

$$i_2 = I_{DSS}\left(1 - \frac{V_1}{V_p}\right)^2 \qquad \text{(A-68)}$$

For any other device, we have to take the necessary transfer characteristic into consideration, and this could theoretically be done by changing the square law into nth order. The voltage v_1 will be in the form

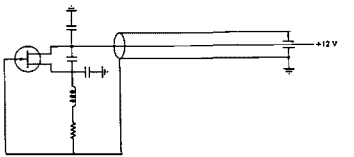


Figure A-1 Quarter-wavelength oscillator with grounded source electrode.

$$v_1 = V_b + V_1 \cos\omega t \tag{A-69}$$

This is the voltage that is being generated due to the selectivity of the tuned circuit at which there is a resonant frequency. Inserting this into the above equation and using

$$V_y = V_p - V_b \tag{A-70}$$

we obtain

$$i_2 = \frac{I_{DSS}}{V^2}\left(V_x^2 - 2V_x V_1 \cos\omega t + V_1^2 \cos^2\omega t\right) \tag{A-71}$$

Once we know the peak value of i_2, we can expland this into a Fourier series. In this case a Fourier series expansion for i_2 has only three terms; that is,

$$i_2(t) = I_o + I_1 \cos\omega t + I_2 \cos 2\omega t \tag{A-72}$$

$$I_o = \frac{I_{DSS}}{V^2} V_x^2 + \frac{V_1^2}{2} \tag{A-73}$$

$$I_1 = -2\frac{I_{DSS}}{V_p^2} V_x V_1 \tag{A-74}$$

$$I_2 = \frac{I_{DSS}}{V^2} \frac{V_1^2}{2} \tag{A-75}$$

Because of the square-law characteristic, I_1 is a linear function of V_1 and we can define a large-signal average transconductance G_m,

$$G_m = \frac{I_1}{V_1} = -2\frac{I_{DSS}}{V_p^2} V_x \tag{A-76}$$

In the case of the square-law characteristic, we find the interesting property that the small-signal transconductance g_m at any particular point is equal to the large-signal average transconductance G_m at the same point. The second harmonic distortion is the output current is given by

$$\frac{I_2}{I_1} = \frac{V_1}{4V_x} = \frac{V_1}{4V_p} \frac{g_{mo}}{g_m} \tag{A-77}$$

The transconductance G_m can be defined in such a way that it indicates the gain for a particular frequency relative to the fundamental, which means that there is a certain G_m for the fundamental frequency and one for the second harmonic, and in the general case, a G_{mn} for the nth-order harmonic. In the more general form, we rewrite our equation

$$i_d = C_n(-V_b + V_1 \cos x)^n \tag{A-78}$$

As this current will exist only during the period from $-\alpha$ to $+\alpha$, the equation

$$-\alpha < x < +\alpha$$

exists only for

$$i_2 = 0$$

$$x = \pm\alpha$$

$$\cos\alpha = \frac{V_b}{V_1}$$

We can rewrite our equation for the drain current or collector current of a transistor:

$$i_d = C_n V_1^n (\cos x - \cos\omega)^n \tag{A-79}$$

The dc value of the current

$$I_d = \frac{1}{\pi}\int_0^{\pi} i_d \, dx \tag{A-80}$$

or

$$I_d = \frac{C_n V_1}{\pi}\int_\alpha^{\pi}(\cos x - \cos\alpha)^n \, dx \tag{A-81}$$

The amplitude of the fundamental frequency

$$I_1 = \frac{2}{\pi}\int_0^{\pi} i_d \cos x \, dx \tag{A-82}$$

or

$$I_1 = \frac{2C_n V_1^n}{\pi}\int_\alpha^{\pi}(\cos x - \cos\alpha)^n \cos x \, dx \tag{A-83}$$

For n = 1, the collector current

$$I_d = C_1 V_1 A_1 \tag{A-84}$$

and the amplitude of the fundamental frequency

$$I_1 = C_1 V_1 B_1 \tag{A-85}$$

For n = 2, the collector current is therefore

$$I_d = C_2 V_1^2 A_2 \tag{A-86}$$

and the amplitude of the fundamental frequency

$$I_1 = C_2 V_1^2 B_2 \tag{A-87}$$

With the definition of the conduction angle,

$$\alpha = \text{arc}\,\frac{V_b}{V_1} \tag{A-88}$$

These values are listed in Table A-3.

TABLE A-3 NORMALIZED FOURIER COEFFICIENTS

$\frac{V_b}{V_1}$	A_1	B_1	$\frac{B_1}{A_1}$	A_2	B_2	$\frac{B_2}{A_2}$
0	0.318	0.500	1.57	0.250	0.425	1.7
0.1	0.269	0.436	1.62	0.191	0.331	1.73
0.2	0.225	0.373	1.66	0.141	0.251	1.78
0.3	0.185	0.312	1.69	0.101	0.181	1.79
0.4	0.144	0.251	1.74	0.0674	0.126	1.87
0.5	0.109	0.195	1.79	0.0422	0.0802	1.90
0.6	0.077	0.141	1.83	0.0244	0.0458	~1.95
0.7	0.050	0.093	1.86	0.0118	0.0236	~2
0.8	0.027	0.052	1.92	0.0043	0.0082	~2
0.9	0.010	0.020	2	0.00074	0.00148	2
1.0	0	0	2	0	0	2

These are the normalized Fourier coefficients as a function of n and the conduction angle. Theoretically, this has to be expanded to the order n of 3 or 4, depending on the particular device, and can be found from tables or by a digital computer.

For simplifications, let us go back to the case of our square-law device, where our transconductance

$$G_m = \frac{I_1}{V_1} = -2\frac{I_{DSS}}{V_P^2} V_2 \tag{A-89}$$

This can be rewritten in the form

$$G_m = \frac{2I_{DSS}}{V_P^2}\left(V_b - V_b + V_1 \cos\omega t\right) \tag{A-90}$$

V_p is the pinch-off voltage of the field-effect transistor, V_b is the bias voltage that is measured between source and ground, and V_1 is the peak value of the voltage of the fundamental frequency. Figure A-2 shows the effect where the sine wave is driving the transfer characteristic, and the resulting output currents are narrow pulses. Based on the duration, the mutual conductance g_m becomes a fraction of the dc transconductance G_m, and therefore the gain is reduced. For small conduction angles $I_n | I_d$, the mutual conductance can take very small values, and therefore the gain gets very small; that is the cause for stabilizing the amplitude in the oscillator. We note that the gain is being reduced as the amplitude causing the small conduction angle is increased.

Fourier analysis indicates that, for a small harmonic distortion, the RF voltage at the source or gate (depending on where it is grounded) has to be less than 80 mV. Now we can design the oscillator performance.

Let us assume that the saturation voltage of the active device is 2 V, battery voltage applied to the transistor is 12 V, and the transistor starts at a dc current of 10 mA with a source resistor of 200Ω. This results in a voltage drop of 1 V at the source and 2 V in the device; therefore, 9 V is available. It can be assumed that the maximum voltage at the drain will be $9 \times \sqrt{2}$. The capacitor voltage divider from drain to voltage now depends on the gain. If we assume an $I_n | I_d$ of 0.15 for about 50° conduction angle, 2α, and the dc conductance of the transistor at

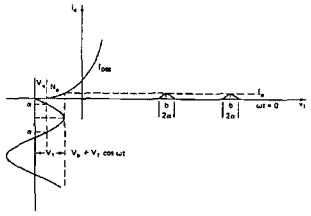


FIGURE A-2 Current tips as a function of narrow conduction angles in a square-wave transfer characteristic.

the starting dc operating point is 20 mA|V, the resulting transconductance is 3 mA|V.

Next we need the output impedance the quarter-wave resonator provides,

$$R_L = Q\frac{1}{\omega C}(250\ \text{MHz})$$

or

$$R_L = 600\frac{1}{2\pi \times 47 \times 10^{-12} \times 250 \times 10^6} = 8127\Omega$$

As we want 9 V rms at the output, we have to use the equation

$$\frac{V_{out}}{V_{in}} = A(\text{voltage gain}) = g_m R_L = 3 \times 10^{-3} \times 8.127 \times 10^3$$

$$A = 24.38$$

or

$$V_{in} = \frac{9V}{A} = 328mV$$

This would mean that the capacitance ratio of the feedback capacitors C_1 and C_2 would be 1:24.38. In practice we will find that this is incorrect, and we need a 1:4 or 1:5 ratio. The reason for this is that the equations we have used so far are not

accurate enough to represent the acutal dc shifts and harmonic occurrences. As mentioned in Sections 4-1 and A-1-5 a certain amount of experimentation is required to obtain the proper value. To determine the actual ratio, it is recommended that one obtain from the transistor manufacturer the device with the lowest gain and build an oscillator testing it over the necessary temperature range. As the gain of the transistor changes as a funciton of temperature (gain increases as temperature decreases for field-effect transistors and acts in reverse for bipolar transistors), a voltage divider has to be chosen that is, on the one hand, high enough to prevent the device from going into saturation which will cause noise, and on the other hand, small enough to allow oscillation under worst-case conditions. Suitable values were determined for the CP643 transistor and shown in the circuit for the field-effect quarter-wavelength transistor.

--See Chapter A-1-6, "Oscillator Amplitude Stabilization," from Digital PLL Frequence Synthesizers, pp. 400-405. Copyright, Dr. Ulrich L. Rohde.

Logarithmic Amplifiers

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Radio first started with just a simple detector. Some early users complained that this lacked sensitivity. The next step was to add a linear amplifier. Then the problem was strong signals, which occasionally required an alert hand on the gain control to avoid severely overloading the receiver. The immediate solution was an automatic finger on the gain reduction control, but AGC systems had problems with choices for time constants, occasionally causing inappropriate responses.

With the advent of radar at the start of WW II the job of the IF amplifier became more demanding. The origin of the problem can be seen in the radar range equation below.

$$S = \frac{PG^2 d \lambda^2}{(4\pi)^3 R^4}$$

S = received power
P = transmitted power
G = antenna gain (ratio, not dB)
d = target radar cross section (area)
λ = wavelength
R = range

The troublsome term is the $1/R^4$ factor. Since the received signal varies as $1/R^4$, a 2:1 change in range leads to a 12 dB change in signal. A radar with a maximum range of 32 miles will normally be expected to resolve the same target at less than 1 mile. A 32:1 range variation gives a 96 dB signal variation. Linear amplifiers with such dynamic range are not currently practical.

One solution to this problem is a swept gain IF amplifier strip. Predictive information is available on the returning radio echo. The time of arrival is directly proportional to the range. If we make the gain of the amplifier time variant so that the gain is proportional to T^4 (T = time elapsed since the transmission of the outgoing pulse) then the IF strip output amplitude should be constant for a particular target at all ranges.

The swept gain method allows wide dynamic range while maintaining the fine amplitude resolution of a linear amplifier. The problem is that swept gain deals poorly with "surprises". A large target can easily paralyse the amplifier. If the recovery time is 1 us, then any object less than 250 feet behind the large reflector will be hidden. The swept gain IF will also fall to pick up small targets, even when they are close in. Surface skimming anti-ship missles are an example of this class of low radio reflection objects.

Limiting amplifiers, which level the output of the IF to a fixxed amplitude, are useful in radars where frequency or phase information is of interest. Doppler and MTI sytems are examples. A limiting IF requires a separate detector system to retain received signal amplitude information if needed.

In the demanding environments of radar, sonar and ECM rapid pulse repetition and amplitude variation cannot be dealt with by the normal AGC loops used in AM and SSB radio systems, because these depend on the continuous nature of the carrier. New techniques used to avoid interception and jamming involve wider use of the electromagnetic spectrum, frequency agility, and pulse compression or dispersion. Such systems require broadband IF amplification that responds instantaneously.

The common technique to achieve the instantaneous compression of dynamic range is to use a logarithmic amplifier. This gives an output voltage that is proportional to the logarithm of the input. Compare this to the case of linear amplifiers where output voltage is proportional to input voltage and to limiting amplifiers where amplitude information is removed by leveling the output.

The important characteristic of a log amp system is its huge instantaneous dynamic range and resulting fast response time. This has advantages over AGC systems where a fixed time constant is optimised to meet predicted variations in amplitude. Sophisticated AGC variations are bulky and expensive. The typical result is a loss of amplitude information if the time constant is too large.

When is a logarithmic amplifier IF system the best choice? The electronics industry sees requirements for instantaneous amplitude compression of input signals in many specialized receiver systems. In a typical log amplifier strip an input dynamic range of 80 dB can be compressed to about 20 dB by the logging action. The output can then be easily processed by succeeding circuitry.

When is a log amp inappropriate? When input amplitude is an important component of the desired information. In applications like radar signature analysis, terrain mapping radar, and terrain following radar linear amplifiers are often used. Logarithmic amplifiers sacrifice amplitude precision for dynamic range, so a linear amplifier will provide superior resolution in these systems.

TYPES OF LOG RECEIVER SYSTEMS

Receivers that accept pulsed signals, such as those used in radar and ECM, tend to use two techniques to step down the signal to a manageable frequency. The heterodyne mixer is widely used in search radar. The crystal video (or microwave detector) is seen on broadband warning and direction finders. Figure 1 shows schematically the essential output signal differences of the logarithmic signal processing employed with these techniques.

(1) LOG VIDEO SYSTEMS

Log video amplifiers are used in systems requiring simplicity, compactness and low price. These systems lack the sensitivity and dynamic range achieved by successive

detection and true log amplifiers. Log video amplifiers perform the logging function directly on the video signal from a microwave detector. It is worth noting that although it is possible to get a log video amplifier system with a dynamic range of 80 dB, the overall system dynamic range is reduced to half by the square law of the detector. Log video sytems are employed in direction finders, alarm systems and other less sensitive measurement equipment.

(2) TRUE LOG SYSTEMS

The second system works from a mixer and is for applications where both sensitivity and minimal frequency distortion in the IF are required. True log amplifiers have a undetected, undistorted IF output of amplitude approximating the logarithm of the input amplitude. Stages can be cascaded to give up to 80 dB of dynamic range. A dual-gain technique is used to obtain the log transfer function. Figure 2 shows such a stage, consisting of a limiting amplifier of gain G in parallel with a unity gain amplifier. This is in fact a hybrid between a linear and a limiting amplifier in form as well as function.

The single stage soft limiting dual-gain characteristic is shown in Figure 3. For small input signals the gain is around 10 dB. The gain drops to unity when the input signal reaches the saturation point of the limiting amplifier part of the stage. The delays can be matched in the unity gain and limiting amplifier portions of the stage to minimize frequency distortion and phase error. The theoretical transfer function of a six stage true log system is shown in figure 4, plotted with both axes linear. It is a series of straight lines with breakpoints where each limiting amplifier saturates. The practical characteristic is curved, giving reduced ripple and less log error. Low ripple is dependent on component matching. An eight stage strip with an 80 dB dynamic range is possible.

(3) SUCCESSIVE DETECTION LOG SYSTEMS

Successive Detection is the most commonly used log IF amplification system. To meet the required dynamic range, identical limiting amplifiers with logarithmic detectors are cascaded. The parallel sum of their detected outputs produce a composite logarithmic straight line transfer function.

The basic stage in a successive detection strip is shown in Fig. 5. A limiting amplifier of 10 dB gain is followed by a low level detector. The single stage response is shown in Fig. 6. An important feature is that the video and RF outputs limit at a precise input level. A three stage strip built with circuits of this type is shown in Fig. 7. The first stage will give a video output identical to a single device. The second is constant so when a logarithmic scale is used for the RF input the second stage video output will be identical to that of the first stage just displaced to the

left by the stage gain, as shown in Fig. 8. This shows the individual transfer characteristics of the three cascaded stages separated by the gain of each limiting amplifier. A 10 dB increase in signal will drive number three detector to its maximum output and similar increases will sequentially saturate D2 and then D1.

The final step is to sum the video outputs. The schematic and corresponding response are shown in Fig. 9. For each increase in input level corresponding to a single stage gain, a contribution equal to the maximum video output from a single stage is added to the summed video output. To obtain a straight log law, stages must be well matched, particularly the detector characteristic and the flatness of the limiting level.

Successive detection log strips give amplification, great sensitivity (-80 dBm), and large dynamic range. They are widely used in marine radars, I.F.F. systems, primary surveillance radars, missile radars, navigation aids, instrumentation, etc.. Their only disadvantage is that the signal phase and frequency information is degraded.

The dynamic range of a log strip can be extended by increasing the number of stages. The limit is reached when the last stage in the cascade reaches full video output solely on the noise produced by the first stage. The number of stages can be increased if the bandwidth of the strip is reduced. It is common practice to insert a bandpass filter in the centre of the log strip for this purpose. Care must be taken that the filter insertion loss is 0 dB or the log response of strip will have a "kink" in the middle of the response curve. Another technique for increasing the dynamic range is to attenuate the input signal and apply it to another short strip operating in parallel to the main strip. The video output from this "lift" strip is added to that from the main strip. Normally the log response limits when the input signal exceeds that necessary to produce full video output from the first stage. The lift strip is fed with an attenuated signal and will continue to give an output change. The limit to this technique is reached when the input voltage is sufficient to cause damage or overload in the first stage of the main strip.

The Plessey SL2521 is a monolithic IC approach to the successive detection log amplifier. The features that make it unique are an improved bandwidth over previous IC amps, 1.3 GHz, and the ability to simultaneously give both a log linear successive detection video output and a phase linear limited IF output. This previously required two separate IF strips, a successive detection log strip for video information and a limiting strip for phase information. When cascaded into a six stage strip the result is 60 dB dynamic range, 600 MHz video detection bandwidth, and 450 MHz IF bandwidth with low phase error.

The monolythic approach offers advantages over and above its combined excellence in both phase and amplitude accuracy.

Compared to a hybrid device the monolythic system has higher reliability, since there are no bonds or solder joints to fail. The final result is not only more reliable than the labor intensive solution, it is physically smaller and lighter. Last but not least the monolythic solution is cheaper.

Three six stage log amplifiers were constructed and evaluated by the Royal Signals and Radar Establishment in England. The basics of the R.S.R.E. results are summarized in the following five figures.

Fig. 10 shows the detected video response of the strip as the input amplitude is varied from -80 dBM to +10 dBM. Response is shown for four different frequencies. Note that the response is log linear between -55 dBM and -5 dBM at frequencies from 60 to 600 MHz. The detected video level drops as the frequency increases, but the slope of the detected output remains relatively constant.

Fig. 11 is the error of the video response. Fig 10 shows small deviations from a perfect linear response. Fig 11 shows this deviation at two frequencies. Note that this is a very difficult measurement to make, requiring attenuators with an absolute accuracy of .25 dB across a range of 80 dB. Hewlett Packard offers a laboratory service that is capable of providing special attenuators individually calibrated to these tolerances. the calibration is valid only at one frequency, so each frequency measured requires a set of super precision attenuators. The video output thus obtained indicates accuracy of .5 dB max error between -55 dBM and -5 dBM at both frequencies tested.

Fig. 12 graphs the output amplitude of the IF port with varying input levels at three frequencies in the range. One of the virtues of the SL2521 is its ability to provide both accurate video output and a quality limited IF respose. The IF output gives solid limiting from -45 dBM to +5 dBM. Both the limiting level and the limiting knee are essentially constant with changes in frequency.

Fig. 13 illustrates the change in phase with change in input amplitude of one of the strips. One of the most unique properties of the SL2521 is that it gives both a log linear video output and a phase linear IF output. At 70 and 450 MHz the phase delay through the six stage strip changes less than 2 degrees across the full dynamic range. The worst case frequency gives a maximum change of 8 degrees across the amplitude range.

Fig. 14 gives the differential phase tracking error between amplifiers across 70 dB of dynamic range. For many uses the absolute amount of the phase shift through the amplifier and the variation of the phase shift with input amplitude are not important. What is important is that the

difference between two channnels remain constant. Phased array radars are an example of such a system.The differential phase change across the available dynamic range is less than 1 degree at 60 and 120 MHz and less than 2.5 degrees at 450 MHz for the six stage SL2521 log strip..

Special thanks to Peter Chadwick and Doug Kleven for assistance in the preparation of this manuscript.

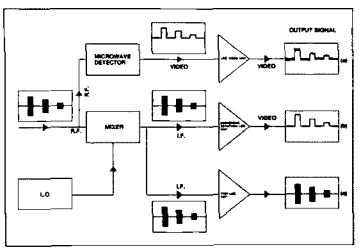


Fig. 1 Block diagram of broadband pulse amplification showing log video, successive detection, and true log techniques.

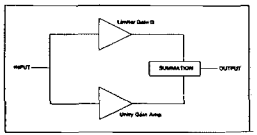


Fig. 2 True log amp block diagram showing limiter and unity gain amps in parallel

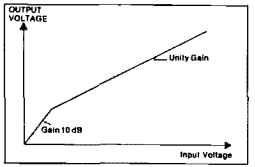
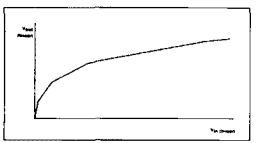


Fig. 3 Transfer function of true log stage showing dual gain characteristic

Fig. 4 Transfer function of six stage true log strip showing approximation of logarithmic response



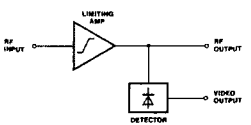


Fig. 5 Basic successive detection stage

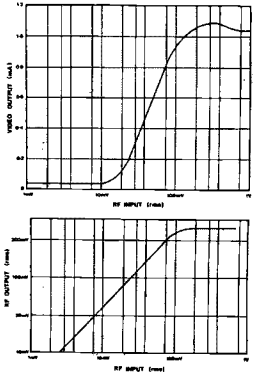


Fig. 6 Successive detection stage transfer function

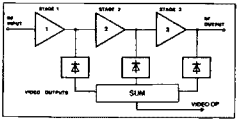


Fig. 7 Three stage log strip

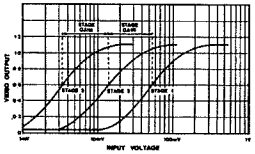


Fig. 8 Video outputs from three stage strip

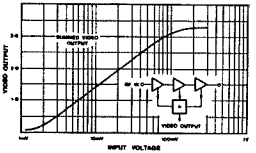


Fig. 9 Summed video output from three stage strip

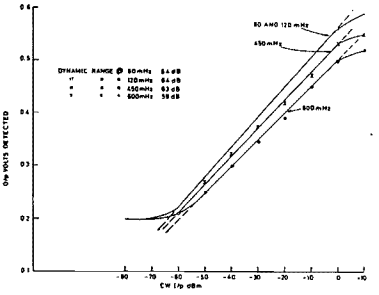


Fig. 10 Video output vs. IF input for six stage SL2521 strip

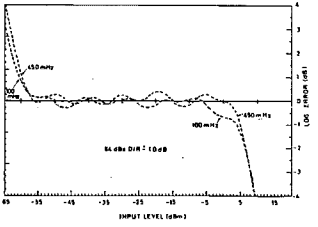


Fig. 11 Log error vs. input level

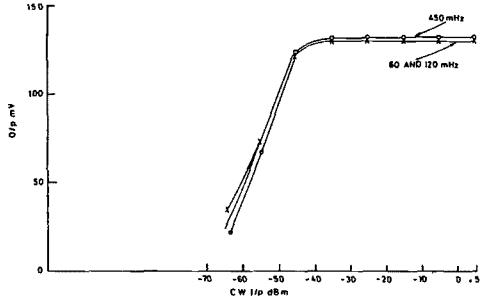


Fig. 12 IF limiting characteristic

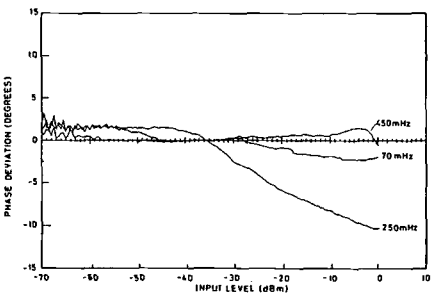


Fig. 13 Phase change vs. input level

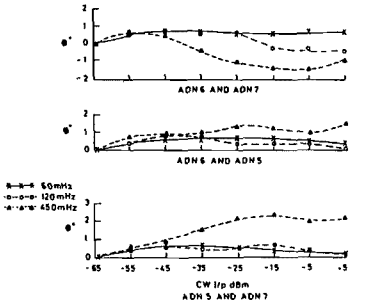


Fig. 14 Phase tracking of amplifier pairs with changing input level

LINEAR FM MODULATOR

by
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ABSTRACT:

A system has been developed that will generate a linear FM modulated pulse signal. The system uses a 100 MHz clock and a 200 MHz CW input to generate a 20 ns pulse of 200 MHz energy. This pulse is used to excite a surface acoustic wave (SAW) expander. The resulting signal is a continuous linear sweep of frequencies of 75 MHz bandwidth, centered about 200 MHz. The duration of this sweep, or chirp, of frequencies is selected by using different SAW expanders. The chirp is then amplified and gated in time to sharpen the corners of the generated spectrum. The system has been designed, assembled, and successfully tested.

INTRODUCTION

Linear FM is a modulation scheme that is commonly used in radar systems.[1] This modulation consists of a sweep of frequencies, sometimes called a chirp, that occur within a given time period and with a specific repetition rate (Figure 1). This paper discusses a system that has been developed to generate this modulation.

THEORY

A Linear FM waveform may be generated by exciting a dispersive delay line with an impulse function. The dispersive delay line transfer function is flat in amplitude and has linear group delay within its bandwidth (Figure 2). The impulse response of the dispersive delay line is the inverse fourier transform of its transfer function. This is a signal of time duration t with the instantaneous frequency varying linearly over the bandwidth of the delay line. This waveform is called the expanded pulse (Figure 1).[2]

This transformation may be visualized by thinking of the delay line as a frequency sensitive delay element that passes lower frequencies with the least amount of delay and higher frequencies with the greatest delay (Figure 3). If you simultaneously input all the frequencies within the delay line's bandwidth they come out in progression from low to high resulting in the expanded pulse.

In our case the dispersive delay line is implemented with a Surface Acoustic Wave (SAW) expander. Three different expanders are used to generate different expanded pulse widths. The

expanders have a transfer function which exhibits linear group delay over a bandwidth of 75 MHz centered at 200 MHz.

To approximate the impulse function the SAW expanders are excited with a 10 ns pulse of 200 MHz. The spectrum of this pulse approximates an impulse function within the 75 MHz bandwidth (Figure 4).

In the SAW expanders the 10 ns input signal is spread over many microseconds resulting in a large loss in amplitude. The loss may be calculated by:

$$(1)\quad \text{Expansion Loss (db)} = 10 \log \frac{\text{Expanded pulse width}}{\text{Input pulse width}}$$

This loss is in addition to the CW insertion loss of the device. The expansion and insertion losses for the three SAW expanders are summarized in Table 1.

SAW EXPANDER	INSERTION LOSS	EXPANSION LOSS	TOTAL LOSS
0.64 us	35 db	18.1 db	53.1 db
5.12 us	35 db	27.1 db	62.1 db
20.48 us	42 db	33.1 db	75.1 db

TABLE 1. SAW EXPANDER LOSSES

SYSTEM CONFIGURATION

The linear FM signal is generated by simultaneously inputing a spectrum of frequencies to a SAW expander. Three SAW expanders are used to generate expanded pulse widths of 0.64 us, 5.12 us, and 20.48 us. These pulses are then amplified and gated to eliminate any undesired signals outside the pulse. A CW mode is also available for test purposes.

The modulator consists of four sections; a digital control section, a Pre-SAW module, the SAW expanders, and the Post-SAW module. These sections are configured as shown in Figure 5.

The construction style for the RF sections is microstip PWBs on GIO material. The Pre and Post-SAW sections were mounted in separate aluminum housings to provide shielding and isolation for the circuitry. The digital control section is located on a card cage PWB as part of the parent system. The switches and SAW expanders are connectorized modules and are connected to the other sections with semi-rigid cable and SMA connectors.

DIGITAL CONTROL SECTION

In response to a modulator trigger signal the digital control section generates two signals; a 10 ns ECL pulse which is sent to the Pre-SAW module and a variable width TTL gate which is sent to the Post-SAW module. The width of the TTL gate signal is equal to the output pulse width of the selected SAW expander, within the resolution of its clock (400 ns).

PRE-SAW MODULE

A schematic diagram of the Pre-SAW module is shown in Figure 6. The input signal for the expander is generated by gating a 200 MHz CW signal for 10 ns. This waveform is shown in Figure 4.

The 200 MHz CW input is amplified by A1 to +7 dbm at the input to the mixer, M1. A 10 ns ECL pulse is input from the digital control board to the mixer IF port through A2. The DC offset voltage on the IF port is trimmed by the 500 ohm pot; this increases the LO to RF isolation of the mixer to approximately 60 db at room temperature. The waveforms shown in Figures 4 are present at the RF port of M1. This signal is amplified to +20 dbm before it is output to the SAW expanders. A test input is provided which turns the mixer on at all times to allow a CW output. It is important that all amplifiers which process the pulsed signal be broadband so that a minimum of distortion is generated.

SAW EXPANDER ASSEMBLY

A schematic diagram of the SAW expander assembly is shown in Figure 7. S1 and S2 determine which of the three SAW expanders or a bypass path is selected. The attenuators on the expander outputs are used to adjust the signal level so that it is identical irregardless of which path is selected.

POST-SAW MODULE

A schematic diagram of the Post-SAW module is shown in Figure 8. The Post-SAW module consists of three amplification stages, a gated mixer and a limiter. The signal level at the input to this module is approximately -67 dbm, therefore a large amount of gain is needed to restore it to a useable level; this is accomplished with A1, A2 and A3. The mixer is gated on by a TTL signal coincident with the leading edge of the expanded pulse. This prevents the large gain in front of the mixer from producing unnecessary noise when the pulse is not present; it also sharpens the edges of the expanded pulse. As in the Pre-SAW module DC bias is provided for the mixer to improve its isolation. The gated expanded pulse at the mixer output is limited by about 6 db in L1. This removes any amplitude ripple in the expanded pulse. The output level is 0 dbm.

SUMMARY AND SUGGESTIONS FOR FURTHER WORK

This system has been prototyped and thoroughly tested. All of the design goals were met. The modulator is presently integrated into a prototype radar system.

There are three areas which I feel could be changed to improve the performance.

1. To achieve the maximum signal to noise level at the modulator output it is necessary to drive the SAW expanders with as large a signal as possible. This creates a requirement for a high power switch at the expander inputs. This part can be costly and hard to obtain. A low power switch may be used by assigning a separate power amp to each expander and switching the low power input to the amp as shown in Figure 9.

2. The signal to noise level is degraded on the .64 us and 5.12 us expanders by the attenuators on their outputs. The attenuators are used to provide equal levels at the Post-SAW input. This equalization may also be accomplished by amplifying the output of the 20.48 us and 5.12 us expanders to the level of the .64 us expander before the switch. This is shown in Figure 10.

3. The expanded pulse is gated by a signal that is generated from a 400ns clock. For the .64 us (640ns) expanded pulse this results in a rather coarse gate. Originally a fourth expander with a longer pulse width was used in the system. This required the 400 ns clock to generate a gate signal long enough for it. With the present three expanders a higher frequency clock could be used to generate a gate of finer resolution. This will eliminate some potential signal processing problems elsewhere in the radar.

[1]Skolnik, M., "Radar Handbook", McGraw-Hill, 1970, p. 20-4.

[2]Andersen Laboratories, "Dispersive Delay Lines", 1983

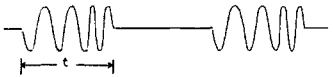

Figure 1. Linear FM Pulse Modulation

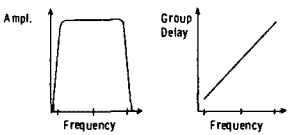

Figure 2. Transfer Function of Dispersive Delay Line

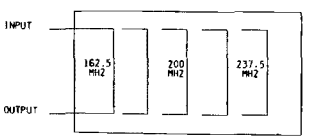

FIGURE 3. DISPERSIVE DELAY LINE

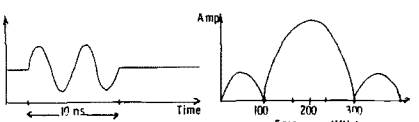

Figure 4. 200 MHz Impulse

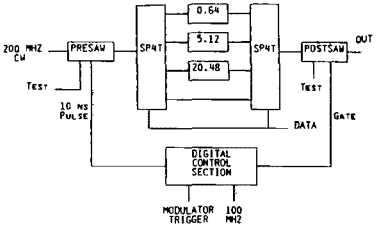

FIGURE 5. SYSTEM CONFIGURATION

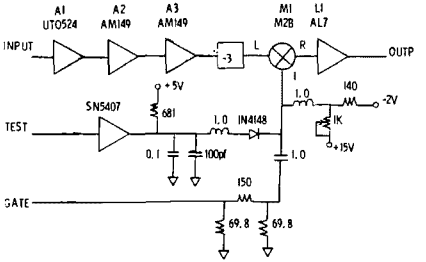

FIGURE 8. Post SAW Module

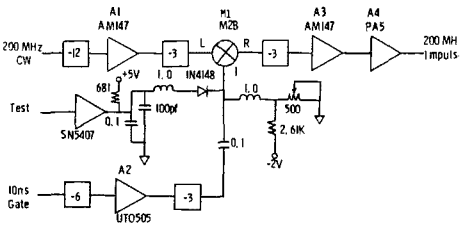

Figure 6. PreSAW Module

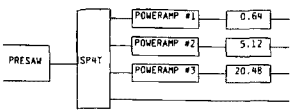

FIGURE 9. LOW POWER SWITCH MODIFICATION

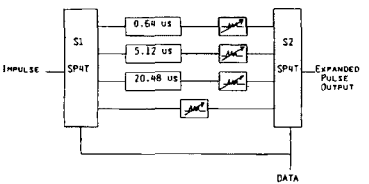

FIGURE 7. SAW EXPANDER ASSEMBLY

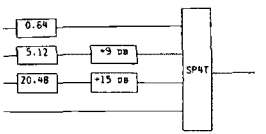

FIGURE 10. SWITCHED OUTPUT AMPS MODIFICATION

EW APPLICATIONS OF HIGH RESOLUTION COMPRESSIVE RECEIVERS

BY

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ABSTRACT

With the crowding of the electromagnetic spectrum and the evolution of spread spectrum and other complex signatures, the ELINT/ESM demands of the 1990's will pose new challenges to EW receiver manufacturers. Resolution down to the hundreds of Hertz and real-time processing will be essential.

This paper will make the system designer aware of a few of these analog technologies for signal processing in radar systems. When low cost, low complexity, and flexibility are key considerations in configuring a system, analog technology should be the system designer's first choice to meet these requirements.

INTRODUCTION: THE EW SCENARIO

Analog compressive (microscan) receivers can be used to provide fast, real-time spectrum analysis of the IF operating band. The range of their performance is characterized in Figure 1. The microscan receiver can provide quick processing times, wide bandwidths or very good resolution depending on the environment and users' needs. Applications can vary from electronic intelligence gathering, radar warning receivers, anti-radiation seekers to moving target indicators (MTI).

The compressive receivers' function is to perform threat analysis on a complex signal environment. This environment is crowded with different modulating techniques, magnitudes of signals and frequencies. The compressive receiver can be configured to gather and translate an unknown, crowded frequency/time spectra, perform a true instantaneous Fourier transform and output valuable information which can be used for threat accuracy measurements.

Threat accuracy can be defined as the probability of intercept (POI) ratio, processing and scan time and system resolution. Each one of these topics will be discussed within the body of the paper.

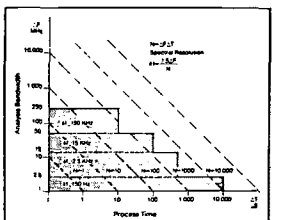


Figure 1. Range of Performance.

THEORY OF THE COMPRESSIVE RECEIVER

A compressive receiver can be configured in two basic forms which are illustrated in Figure 2. Each one has its own applications when used within the EW environment.

The C-M-C compressive receiver, Figure 2B, has its own applications within the EW environment, but due to its poorer dynamic range and increased cost over the M-C-M system, it will only be briefly mentioned.

The C-M-C configuration suffers from poorer dynamic range due to its signal-to-noise ratio. Typically the dispersive devices' insertion loss is -30dB to -40dB. Any incoming RF signal must be recovered before convolution occurs, and then be recovered again at the output of the second dispersive device. With the M-C-M configuration this recovery of signal-to-noise is minimized.

In the M-C-M configuration, Figure 2A, the incoming RF signal has only to be recovered after going through one dispersive device and not two. The sweeping local oscillator (SLO) has negligible effect on the incoming signal due to its noise level. The noise level of the SLO is strictly limited to the thermal noise of itself.

The M-C-M compressive receiver will be discussed in depth and specifically mention the multiply long-convolve short M-C-M transform method. Either M-C-M or C-M-C configuration can guarantee 100% probability of intercept when a tandem system is implemented.

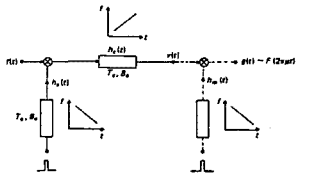


FIGURE 2A: Multiply-Convolve-Multiply Fourier Transform System

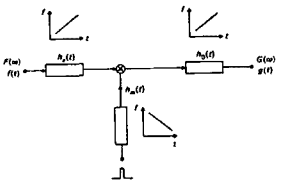


FIGURE 2B: Convolve-Multiply-Convolve Fourier Transform System

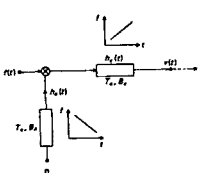


FIGURE 2C: Multiply-Convolve Fourier Transform System

If only one system is to be used and a maximum FOI is required, the M-C-M multiply short microscan receiver should be implemented. This configuration is designed with a shorter dead time interval to provide maximum coverage of the analysis bandwidth. This system has an added advantage in that amplitude and phase information is preserved for possible down line signal processing if the user requires. Spectral phase can be preserved allowing inverse transforming back to the original input domain. If spectral phase data is not required by the user, in threat analysis, the user could simply eliminate the final multiply stage which is used to preserve phase data, Figure 2C. Derivation of the above systems mentioned generated waveforms can be reviewed in Morgan, Surface-Wave Devices for Signal Processing, pp 271-275 [1].

A point that should be mentioned is that the M-C-M multiply long system's Fourier output spectra does not exactly correspond to the input spectra. This is due to an effect known as a "Sliding Fourier Effect" [2] transform.

OPERATION OF THE COMPRESSIVE RECEIVER

Let us assume the scenario in which Figure 3, a functional block diagram of a compressive receiver, detects a variety of threat spectra which must be quickly detected, analyzed, discriminated and acted upon. This threat spectra could be transmitted from a hostile frequency jammer, hopper or ECM communications. These intercepted signals are mixed with the known generated chirp or the sweeping local oscillator.

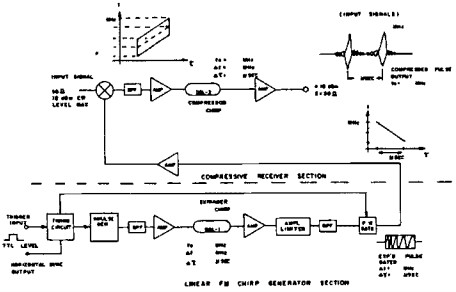


FIGURE 3: Compressive IF Receiver
Functional Block Diagram

This signal is amplified and fed into the compressor of the microscan receiver. The compressor is designed with the required bandwidth, dispersion and opposite sign slope of the SLO and can be weighted. Convolution occurs, and the output is the magnitude of the Fourier transform of the complex input spectra.

The weighting can be a separate "Black Box" within the receiver if the user prefers. Typically a Hamming or Taylor weighting function is used. Weighting is performed within the receiver to reduce time sidelobes at the output. This gives the system the capability to resolve similar frequencies with substantially different power levels and modulating techniques. Weighting of the output pulse does incur some system resolution loss, but the device bandwidth can be increased to compensate for this. A coherent or non-coherent system can be designed if the user requires.

BUILDING BLOCKS OF THE COMPRESSIVE RECEIVER

Analog pulse compression can be accomplished using specific technologies of Surface Acoustic Wave (SAW) Reflective Array Compressors (RAC) or Impedance Control Devices (IMCON). Each device has its advantages and applications within the receiver.

IMCON TECHNOLOGY

The IMCON, which was developed at Andersen Laboratories, Inc., in 1968, is used as a key signal processing component for commercial, military and aerospace system applications.

The IMCON is based on the concepts of a single grating dispersive device which makes use of Perini's[3] observations that impedance mismatches which occur at joints in waveguides can produce reflections. By controlling the location of these impedance mismatches or surface discontinuities, a grating device could be generated where reflections could be advantageously used.

As illustrated in Figure 4, the IMCON is configured using a rectangular thin steel strip as the media for wave propagation. At one end of this steel strip two piezoelectric horizontal shear mode transducers are edge bonded to the steel. These piezoelectric transducers are cut and lapped along the proper axis to allow for highest coupling of electric energy. The function of the piezoelectric transducers is to convert an electric signal to an acoustic signal and then to retransfer this acoustic energy back to electric energy at the output of the device. A herringbone-like pattern or grating is designed and photolithographically etched on to the steel at a 45 degree angle to the acoustic path from the transducers. The grating pattern is designed so that the acoustic energy at various frequencies reflects at differing distances from the transducers, giving a precisely controlled time delay as a function of frequency to the output.

An acoustic damping material is applied to the edges and one end of the steel strip. This acoustic damping material helps to eliminate any type of time spurious signals which may degrade the performance of the device.

A key advantage of the IMCON over other technologies is the availability to routinely amplitude correct and phase correct for any type of ambiguities which may occur due to manufacturing imperfections.

Depending on a customer's requirements, amplitude and phase errors can be controlled to a tolerance typical of ± 0.2dB of amplitude error, and $\pm 1^{0}$ of phase error. Sidelobe structure in the area of -40dB is the norm for IMCON performance and -50dB sidelobes have been demonstrated. Dispersions from 8 μsec to 5a5 μsec can be implemented on one steel strip, and if required the IMCONs can be cascaded together to achieve 10,090 μsec of dispersion in one package.

The IMCON is a linear device whose delay vs. frequency characteristic curve can be defined by Figure 5. The phase response of the IMCON is defined as a quadratic response. It is considered a reciprocal device in that once it is tuned either transducer can be configured as either input or output.

IMCONs can be designed, according to the users needs, as either up-chirp (positive slope devices) or down-chirp (negative slope devices). An up-chirp

device is designed with the low frequency grating lines appearing closest to the transducers and traversing up the media of proportion. As the frequency increases the grating line spacing will physically get closeo together through the band of interest. This is opposite for down-chirp devices. The up-chirp IMCON can operate from 4 MHz to 24 MHz with 50% bandwidths. Down-chirp devices do have some bandwidth limitations due to undesired accustic modes[4], but can be implesented as long as the bandwidth is under 10%. IMCONs can be designed depending on a customer's praference as linear FM or non-linear FM. The NLFM IMCON has a slope which will vary across its operating bans.

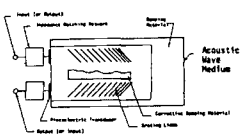


FIGURE 4: SAW RAC/IMCON Structure

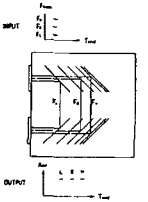


FIGURE 5: SAW RAC/IMCON UP-CHIRP FREQUENCY DISPERSION

SAW RAC TECHNOLOGY

Within the last 10 years the SAW device has become the "most common main throughout analog device for pulse compression techniques"[5]. Center frequencies as high as 1 GHz are being developed and soon will be able to be commercially fabricated. Dispersions of 100 us, bandwidths of 500 MHz, and sidelobes of -40dB can be realized within the laboratory under tightly controlled manufacturing tolerances. The advantage of the SAW RAC over most other analog devices and the digital counterpart is its size, weight, cost and reliability.

The surface acoustic wave reflective array compressor (SAW RAC) is the SAW technology counterpart to the IMCON. The SAW RAC is conceptually similar in structure to the IMCON in that grating lines are etched into a substrate such as litnium niobate, or other, depending on the user's applicable environment. The SAW RAC offers practical methods of achieving linear and non-linear FM dispersive delay characteristics. Using ion beam etching, grating lines can be etched into a substrate in varying depths to achieve the user's required amplitude/frequency weighting characteristics. Grating lines can be positioned if required to achieve the above mentioned non-linear delay function.

The SAW RAC is most suited for moderate dispersions (<100 usec), bandwidth capabilities from 20 MHz to 100 MHz and sidelobe performance of -35dB, typical, in the linear FM application.

The SAW RAC operates at center frequencies from 10 MHz to 1000 MHz and can be easily manufactured as up-chirp or down-chirp devices.

SAW RAC AND IMCON USE IN COMPRESSIVE RECEIVERS

The compressive receiver is a fast, active real time Fourier analysis receiver that has applications in ELINT/ESM surveillance. The IMCON or SAW RAC when configured in the compressive receiver will generate the linear sweep of the desired dispersion and analysis bandwidth. The linear sweep can be generated by impulsing the specific dispersive devices as in the case of a coherent system or the user may choose to do their own triggering of the chirp as in the non-coherent system.

The output of the dispersive device is a high energy expanded pulse with the designed dispersive content and analysis bandwidth.

PERFORMANCE OF A COMPRESSIVE RECEIVER

Now that the basic building blocks are understood we can begin to define some terminology within the receiver. This terminology will be helpful when the user is ready to draw up a technical specification of a compressive receiver.

SPECTRAL RESOLUTION COMPUTATIONS

Spectral resolution (δf), is defined as the smallest frequency deviation or difference that can be detected and accurately measured. Resolution down to the hundreds of Hertz can be achieved when large time bandwidth products are implemented.

Resolution is defined as: $\delta f = \frac{P_b}{\Delta\tau}$

where
- δf = System Resolution
- $\Delta\tau$ = System Dispersion
- P_b = Pulse Broadening Factor as a result of a weighting function being used to suppress temporal sidelobes. For example, when $P_b = 1.0$ this is a typical pulse broadening factor for no weighting; when $P_b = 1.5$ this is a typical pulse broadening factor for a Taylor weighting of 47-50dB.

PROCESSING TIME COMPUTATIONS

Processing time is defined as the amount of time the compressive receiver needs to analyze an incoming frequency spectrum once it has been captured within the analysis band and display the Fourier transform at the output as a function of time.

Processing time is defined as, $P_t = K(\Delta\tau) + t$

where
- P_t = Signal Processing Time
- K = Multiplication factor for the number of cascaded compressive receivers
- $\Delta\tau$ = System Dispersion
- t = Delay Time attributed to non-dispersive devices, i.e., mixers, bandpass filters, etc.

PULSE WIDTH COMPUTATIONS

Pulse width measurements can be defined as:

$$\text{-4dB pulse width} = \frac{P_b}{\Delta\tau}$$

where
- P_b = Pulse Broadening Factor as a result of a weighting function being used to suppress temporal sidelobes
- Δf = Analysis Bandwidth

POI COMPUTATIONS

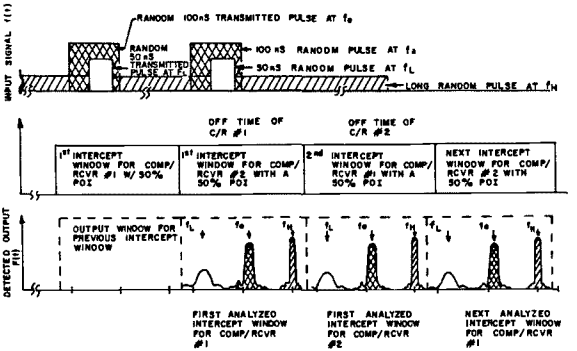
Probability of intercept is defined as the chance that a signal, if present within a given frequency/time spectra, will be detected.

POI for a compressive receiver can be defined as a minimum of 50%. This is characterized by:

$$\frac{\Delta\tau}{\text{Pulse Repetition Time}}$$

where $\Delta\tau$ = system dispersion.

Any signal which is captured within the ramp of the chirp will be displayed as a Fourier transform. If two compressive receivers were to be run so that their "chirps" were to share some overlap time, Figure 6, a 100% POI would be guaranteed!


INPUT SIGNAL f(t)
RANDOM 100nS TRANSMITTED PULSE AT f_0
RANDOM 50 nS TRANSMITTED PULSE AT f_a
100 nS RANDOM PULSE AT f_a
50nS RANDOM PULSE AT f_L
LONG RANDOM PULSE AT f_N
OFF TIME OF C/R #1
OFF TIME OF C/R #2
1ST INTERCEPT WINDOW FOR COMP/ RCVR #1 W/ 50% POI
1ST INTERCEPT WINDOW FOR COMP/ RCVR #2 WITH A 50% POI
2nd INTERCEPT WINDOW FOR COMP/ RCVR #1 WITH A 50% POI
NEXT INTERCEPT WINDOW FOR COMP/ RCVR #2 WITH 50% POI
DETECTED OUTPUT F(t)
OUTPUT WINDOW FOR PREVIOUS INTERCEPT WINDOW
f_L
f_0
f_H
FIRST ANALYZED INTERCEPT WINDOW FOR COMP/RCVR #1
FIRST ANALYZED INTERCEPT WINDOW FOR COMP/RCVR #2
NEXT ANALYZED INTERCEPT WINDOW FOR COMP/RCVR #1

100% GUARANTEED POI
COMP/RCVR SYSTEM
BLOCK DIAGRAM
FIGURE 6

CONCLUSION

The use of such devices as SAW and IMCON technology give the compressive receiver the flexibility, low cost and low complexity that is required when designing signal processing radar systems. These technologies give a user the necessary requirements of excellent resolution, wide band surveillance and true fast Fourier analysis of all types of incoming signatures which are present within the EW/ECM environment. When the IF spectrum is to be analyzed, IMCON and SAW analog technology should be the system designer's choice.

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2. Ibid. pg 275.
3. Sittig and Coquin, "Filters and Dispersive Delay Lines Using Repetitively Misaatched Ultrasonic Transaission Lines", IEEE Trans. on Sonics and Ultrasonics, Vol. SU-15, No. 2, April 1968.
4. Martin, T. A., Microwave Network Approach to the IMCON Dispersive Delay Line", The University of Connecticut, Ph.D., 1974.
5. Brookner. Eli, "Trends in Radar Signal Processing", Microwave Journal, October 1982.

DIGITAL - RF INTERFACING

The Story of a Marriage

by

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submitted to

RF DESIGN RF EXPO EAST

NOV. 1986

DIGITAL - RF INTERFACING
The Story of a Marriage

My story begins in a far-off place, many years ago, at the time of the flood. All creatures of the earth boarded the Ark in pairs, two by two. Noah, the engineer in charge of construction, selected at the last moment his final pair, a couple of engineers. One was an RF engineer, the other of the digital persuasion.

Since then, the two disciplines have prospered in their separate ways, managing until recently to avoid much contact with each other. Within the last few years, however, the cultural restraints of the past have been thrust aside, and we are now in an era of fruitful cooperation.

The disciplines of RF and Digital have joined forces. The place where they have met is called the interface. Fraught with problems and tensions of protocol, this boundary is important and deserves our attention .

Three factors make the digital-RF interface increasingly important:

First, the systems of today call for sophisticated, almost symphonic control of a large number of separate elements, be they antennas, phase shifters, attenuators or separate signal paths, etc., etc. The individual contributions of these elements are combined and manipulated by computer programs to create powerful systems.

Second, the necessary digitally controlled components are available today to control the phase, attenuation and routing of RF signals; (RF and IF are considered equals in this discussion).

Third, computer programs and control systems are available to give, receive and digest information to and from RF equipment.

Where is the RF-Digital interface? Precisely where does RF became digital? This is rather like asking where the source of the Nile is. The most obvious case is that of a digitally controlled RF component, in the form of an attenuator, phase shifter, multi-pole electronic switch or switch matrix, to name a few. Inside each such package, the designer has to do what is required so that the unit will perform its function when addressed digitally by the user. The component designer thus provides the first interface, but he does it in private, as it were. As long as he remains consistent with an accepted method of address, he can do what he wants inside his box, and in that sense he has few problems with this first interface, most of which is hidden mercifully from view.

If we assume that our RF designer is producing an RF receiver, then he will soon have the confidence to group various components, each digitally controlled, into a complete, self-contained design. Now he has to face a different, and more scary, interface, because in the outside world strangers will want to talk to his machine, and he will not be able to cover up little idiosyncrasies as he could in the privacy of his own domain.

In that sense the first true interface is the public one, where the digitally controlled component, sealed in its own container and provided with connections and data sheet, meets its alien user. As units became more complex, and as major assemblies are separated physically from each other by greater distances, the interface changes in nature, and requires quite different approaches. Most of these latter interface considerations can be said to be purely digital in nature, and no longer of the RF sort, but in this age of increasing complexity it behoves the RF engineer to become more aware of the overall digital scene, and certainly the digital engineer can learn from the RF engineer, particularly in terms of processing high frequency bit-streams.

One aspect of the interface is that of architecture, the 'big picture', in which the flow of information is studied in terms of systems such as the IEEE-488 bus and its associates, for example the economical and hard-working RS-422C and variants. References thereto are appended to this paper.

The other aspect concerns the nitty-gritty detail of interfacing, at the level where wire meets wire and voltage meets current. This aspect, in the experience of this speaker, is the most problematic, and gives the greatest opportunity for creative chaos. My company supplies digitally controlled components to the industry, and I believe it is appropriate to discuss some of the practical problems that have risen with the interface. Some of them may sound silly and obvious, but all have caused problems at one time or another for those peering across the Digital-RF frontier. The list is unending, but I have selected a few of the more obvious.

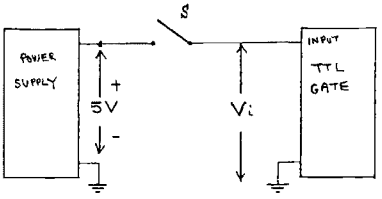
Any discussion of interface detail must begin with Transistor-Transistor Logic, or TTL, which has truly become the day-to-day language, the lingua franca, of RF-Digital interfacing. Most RF engineers have heard of TTL, and know that it uses two voltage levels to represent the two states of the binary system; a low voltage of about zero represents a '0', while a high voltage of plus 5 or so represents a '1'. Right?.....WRONG!

The above statement epitomizes the type of misunderstanding that can make life difficult. Figure 1 illustrates my own first attempt, many years ago, to test a TTL device. When switch S was open, voltage Vi applied across the input of the gate was zero. When the switch was closed, Vi became +5V. Should have worked! All digitally literate persons in the audience will smirk at such innocence, but I found later that a lot of people had been down this particular alley, to their later chagrin.

Figure 2 uses a typical TTL interface to demonstrate what was wrong. At the left is a TTL gate output of the open-collector type, which uses R1 to provide the collector of transistor Q1 with positive voltage. Sometimes a transistor is used to perform the function of R1, and the output is referred to quaintly as a 'totem pole'. R1 is also connected to the emitter of gate input transistor Q2.

When the base of Q1 is biased 'on', base and collector currents ib and ic flow, the latter being predominantly from the emitter of Q2, since R1 is of high resistance. Inter-stage voltage Vi changes from +5V to about +0.3V, with the flow of emitter current Ie from Q2 thru Q1 to ground. The effect on Q2 is to lower the collector voltage, cutting off transistor Q3 and changing the state of gate 2. It is interesting to see how TTL evolved as an improved version of the earlier Diode-Transistor-Logic, or DTL. The circular inset of Figure 2 shows how the diodes of DTL became the transistor of TTL. Note that the input voltage Vi indeed changed from +5V to +0.3V, just as the test circuit of Figure 1 was meant to simulate; the difference is that something else happened too. Transistor Q1 of gate 1 acted as a sink, permitting emitter current from input transistor Q2 to flow, thus initiating the state-change process in gate 2. Table 1 summarises the action.

A full discussion of the exact operating criteria for proper TTL operation is beyond the scope of this paper, (the interested are encouraged to read the attached References), but already we can see the important truth that TTL operation is first and foremost concerned with impedance change, in this case from the emitter of Q2 to ground. Anything that causes that impedance, or simply resistance, to change efficiently from a low to a high value will operate the TTL gate properly. A screwdriver held from emitter to ground will do just fine. The +5V level at the input is not essential, but enhances noise immunity in practical systems, by ensuring that transistor Q2 is held 'off' even when noise spikes of a few volts are present.



S	Vi
OPEN	0
CLOSED	+5

FIG 1
HOW NOT TO CONTROL A TTL GATE

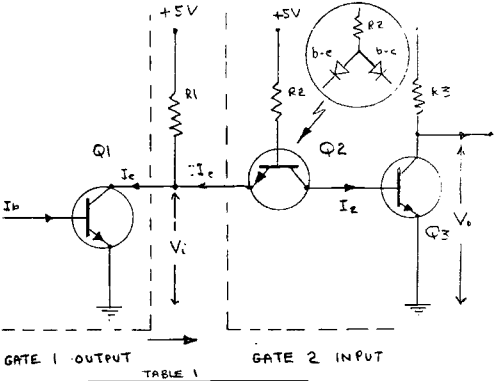


TABLE 1

I_b mA	V_i V	I_e mA	I_c mA	V_o V
0	3.5	0	2	.3
2	.3	2	0	.5

FIG 2
BASIC TTL INTERFACE

Figure 3 shows a practical TTL test circuit at the right, compared with the original non-working circuit of Figure 1 at the left. The value of the resistor R is arbitrary within limits; 3K ohms is reasonable. When switch S2 is open, the gate input is high impedance and held high to +5V. When S2 is closed, the input voltage is close to zero and a low impedance permits the emitter current of the input gate to flow unimpeded.

The above does not mean that the TTL recommended levels corresponding to '1' and '0' are unimporant; it is just that a gate input will of its own accord assume the appropriate voltages if the proper high or low impedance connections are made to it. You never 'apply' the correct voltages to it. If, for example, the sink path impedance connected to the gate input is too high, then the emitter current to ground will cause too high a voltage drop, and the emitter bias will not permit proper gate operation. In that case the input voltage will exceed the specified maximum.

While these considerations are important when testing a TTL unit, they are equally important in normal circuit design. For example, the output of a TTL gate that will 'feed' the input of another has a finite sink current capability. If more current has to be sunk than can be handled by the gate output, then the emitter voltage of the input gate will become too high and exceed permitted limits.

Figure 4 illustrates this point. Assume that, for some reason, a total of twenty gate inputs are connected in parallel and have to be driven from a TTL source. The emitters of the input transistors, Q1 thru Q20, each carry a normal sink current of about 1.6 mA. (This is standard for TTL, although it is sensible always to check the handbook for the sink requirements of a particular gate). The total sink current is then 32mA.

If the twenty input gates of the figure are hidden, being enclosed within a digital attenuator or like device, then a problem can arise when the user of the device goes to provide a TTL control driver. All he has been told is that the attenuator is TTL compatible, and he may assume that a normal low-current gate will do the job, providing a maximum sink current capability of 16mA. The interface will not work, and a lot of effort may be expended finding out why.

The answer here is to tell the user more detail about the required interface, and this is done by adding the note 'TTL compatible, 20 standard loads'. It will be realized that this is a very unusual case, but it is not at all unusual to have two gates in parallel, and to find that the driver

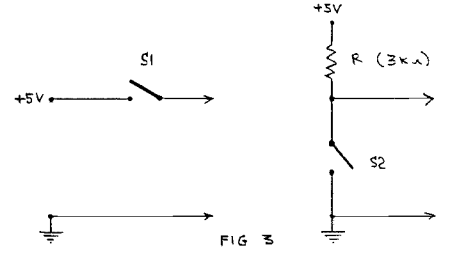


FIG 3

TEST CIRCUITS

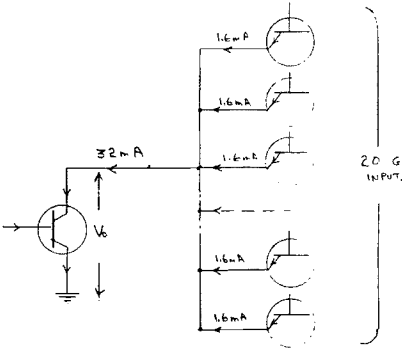


FIG 4

OVERLOAD

gate was feeding other gates in addition to those of the attenuator in question. If told how many standard loads have to be sunk, the user can provide a high-current driver gate or take other precautions.

A further caveat. You may recall my associating the low-voltage state with digital '0', and the high-voltage state with a '1'. Beware! Your digital engineer can get very tricky with things like "negative logic, active low", and you can find , too late and to your expensive embarrassment, that he meant 'TTL 1 = low '. The safest thing for the RF engineer to do is refer to the states as 'TTL High', and 'TTL Low' or even 'TTL Low Voltage', etc. In the case of a digital attenuator, for example, the specification should then read:

'TTL high = 0dB, TTL low = xdB'

Rather than:

'TTL 1 = 0dB, TTL 0 = xdB'

Such a message rings loud and clear across the interface. Never proceed with a design until this matter is fully clarified. You may get laughed at for being pedantic, but he who laughs last laughs within budget and delivers on time.

It was pointed out earlier that a TTL device can be tested by making a simple metallic, e.g. screwdriver, connection from TTL input to ground. Figure 5 shows how not to do that, and raises an important point about handling devices safely without impairing reliability.

Whether it is a screwdriver or an alligator clip held in the hand, the wrong method, i.e. touch the input and then ground it, can result in destruction of the unit, because of the static charge that can build up on hands and other things that may touch the input. In the right method, the grounded metal is applied to the input. Small difference, big effect! Such a circumstance may not be likely to arise in a completed design, but many a chip has gone to its reward at Incoming Inspection, at the hands of a dedicated inspector who wanted to make sure the thing was working properly, and who did not have specialized test equipment to test all the different devices that cross his bench.

Fortunately, TTL devices are remarkably rugged and under most circumstances do not require special handling as some CMOS and diode assemblies do, with grounded wrists and conductive floor mats. Simple good manners and common sense will usually suffice.

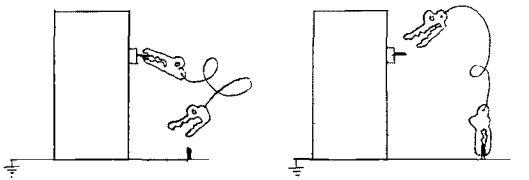


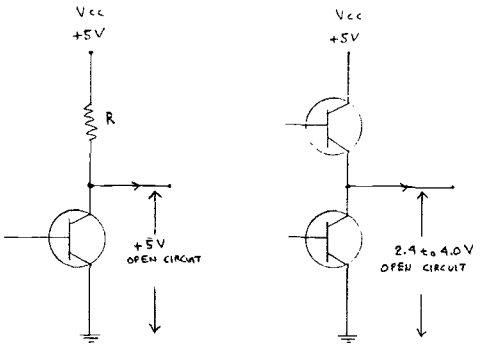
FIG 5
GROUNDING

Earlier we encountered Open-Collector and Totem-Pole TTL output circuits, each of which has its place in classical digital practice. One facet of their use can be exploited by the RF engineer. Figure 6 shows the two types side-by-side, with each in the high output state. In the case of the open-collector output, the circuit is defined fully by the values of Vcc and R, both of which can be known with precision; if some analog function is to be operated by the output, it can be properly designed. In the case of the totem-pole circuit, the exact value of the open-circuit voltage is dependent on a number of variables, and cannot be known as precisely. The primary reason for the totem-pole's use is in achieving speed of operation, as the output is driven high.

The one area where the digital engineer can learn from his RF colleague is that of high speed operation. TTL gates are available with operating times in the region of a few nanoseconds. In addition, the gates of TTL include very high gain amplifiers that limit severely to form the square waves we all enjoy; but they are still very high gain devices with enormous bandwidths. In terms of RF amplifiers, we are dealing with units having gains of 40 to 60 dB, and bandwidths of DC to several hundred Megahertz. Whereas the RF engineer would shield such boxes and have them on a proper ground plane with short interconnecting leads, the digital world tends still to think in terms of plastic devices mounted on boards having no effective ground plane, and with long, thin wire interconnections. Shame on them! They deserve the oscillations, crosstalk and ringing they get.

Similarly, when high-speed digital bit streams have to be transported more than an inch or so, there is an ancient body of transmission line theory and practice available to the digital engineer from the earliest days of radio, so that he can improve his systems without reinventing the wheel. Such knowledge deals directly with the problems of delay, circuit ringing, reflections, etc., that plagued the engineers who laid the first trans-Atlantic cable eons ago.

What I have tried to do is highlight some of the problems of the Digital-RF interface in practical terms; there is a long way to go, but it looks as if the artificial interface of mutual ignorance is being broken down, to the benifit of both camps. We now have reached another interface - that between this talk and the next. Thank you for listening.



Ref. 1 'Designing With TTL Integrated Circuits' T.I Series, McGraw-Hill.

Ref. 2 'The TTL Design Handbook' Texas Instruments.

Ref. 3 'IEEE Standard Digital Interface for Programmable Instrumentation', ANSI/IEEE Std. 488, (New York IEEE Inc. 1978)

Ref. 4 'Line Circuits for IEEE and EIA Inustry Standards, Texas Instruments, Inc., Dallas, TX 1982), Document SC6-588.

Ref. 5 'Reprints from Microwaves and RF on TTL Interfacing Articles', by R.Sproul, Lorch Electronics Corp., 105 Cedar Lane, Englewood, NJ 07631.

RF BIPOLAR PARAMETER EXTRACTION FOR MODELING CLASS C AMPLIFIER RESPONSE

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Today's RF circuit designer has many circuit response simulation models at his disposal to speed breadboarding, and to provide some unique analysis capabilities. Some of these models employ rigorous transistor models based to a large extent upon the integral Charge-Control bipolar transistor model published by H. K. Gummel and H. C. Poon in 1970.[1] The G-P model basically improves upon the dc model of Ebers and Moll[2] in that it incorporates a unified approach to charge storage within the device thus enhancing its ability to predict ac performance.

Our major concern here is with the accuracy of the model parameters, as evidenced by the precision of the circuit simulation. Since parameter extraction from dc and ac measurements involves curve fitting and extrapolation from tangents, one must take care to arrive at solutions that are physically rational as well as satisfying the requirements for a good fit. We begin with those derived from dc measurements of the device.

Parameter Extraction From DC Measurements

The most informative dc measurement to be performed is what is known as the "Gummel Plot" (fig 1.) This is simply a log vs. linear plot of collector and base currents (I_C and I_B) vs. the intrinsic base-emitter forward bias voltage ($V_{B'E'}$) with V_{BC}=0. From this plot one can determine:

the transport saturation current (I_S),

ideal maximum forward beta (B_F),

the foward current emission coefficient (N_F),

the base-emitter forward bias emission coefficient (N_E),

the base-emitter forward bias leakage saturation current (I_{SE} or C_2), the forward knee current (I_{KF}).

Transport Saturation Current (I_S) is obtained by extrapolating the plot of the natural log of collector current to the y axis (V_{BE}=0). The value obtained for I_S is proportional to the area of the emitter base junction, and therefore is device type dependent.

Ideal maximum forward beta (B_F) can be determined from the maximum separation between the two curves (I_C/I_B), and varies substantially from wafer lot to wafer lot. A typical low noise transistor may have B_F from 100 to 200, while a 12.5 volt, class C power transistor will typically have a B_F of 40 to 80.

The forward emission coefficient (N_F) is extracted from the slope of the I_B locus in the mid region of the plot and models the deviation from ideal slope. N_F typically has a value of near unity.

The base-emitter low level forward bias emission coefficient (N_E or n_{EL}) is typically 2 for a shallow junction transistor, and is calculated from the slope of the I_B line near the Y axis.

$$\text{Slope} = q/(NE)KT$$

The base-emitter leakage saturation current (I_{SE} or C_2) models leakage current of the forward biased base-emitter junction. It is obtained from the Y axis intercept of the extrapolated curve for IB.

$$\text{(Y intercept)} = C_2 I_S$$

Forward knee current (I_{KF}) characterizes the onset of high injection effects and is near where the slope of the I_C curve changes to half its original value.

Similarly, a group of parameters is extracted from the Gummel Plot of the reverse transistor (i.e., exchanging collector for emitter) (fig. 2),

yielding:

maximum reverse beta (B_R),

reverse current emission coefficient (N_R),

base-collector leakage emission coefficient (N_C),

base-collector saturation current (I_{SC} or C_4),

and reverse knee current (I_{KR}).

Extracted from DC Beta plots (I_C vs V_{CE} for stepped I_B) are measurements from which the forward Early Voltage (V_{AF}), and collector resistance (R_C) can be extracted.

V_{AF} can be graphically determined (fig. 3) by extending a tangent of the I_C plot to intercept the x axis (a negative number). The foward Early Voltage is an indication of the doping level of the active base in the vicinity of the collector. As the voltage across the collector-base junction is increased, the effective base charge is reduced as the collector depletion area spreads into the base, and so forward beta increases (the Early Effect[3]). For lower frequency devices with deeper bases (f_t < 2 Ghz), V_{AF} is typically over 100 volts, but for very high frequency NPNs, and especially PNPs , the Early Voltage may be considerably less than 50 volts.

R_C can be extracted as $R_{C(sat)}$ and/or $R_{C(active)}$ by calculating the slope of the line tangent to the I_C curve in the saturation region, or through the knees of the active region, respectively (fig. 4).

The reverse Early Voltage (V_{AR}) is similarly extracted from the reverse beta plot (fig. 5). Because the reverse transistor's "collector" is the heavily doped emitter region of the forward transistor, the depletion area spreads more readily into the more lightly doped base, and V_{AR} is normally less than V_{AF}.

Parameter Extraction From Capacitance Vs. Voltage Mesurements

Capacitance parameters are obtained by employing curve fitting techniques, assuming that capacitance vs voltage follows the model:

$$C_j(V) = C_j0 / (1-V/f)^m + C_{(para)}$$

$C_{(para)}$, the parasitic capacitance of the package, bond pads, and die metallization must be measured and/or calculated. With the appropriate algorithm, $C_{(para)}$ can also be curve fitted. A reasonable approximation of $C_{(para)}$ would be 50% of specified capacitance at rated voltage for a typical 12 volt UHF transistor, to less than 20% for a 50 volt microwave pulsed power transistor.

Barrier potential f is typically 0.5 to 0.7 volt, and the gradient factor m is expected to be .33 to .50, representing the graded junction and abrupt junction respectively. Specific conditions such as collector grading can lead to effective values of m beyond the normal range. More accurate models are needed.

Simulation programs such as SPICE [8] use f and m only to calculate capacitance vs voltage, so even though the absolute numbers arrived at through curve fitting may not be in agreement with physical data, the circuit simulation results may be. The art is to set limits for parameters derived from device layout and process knowledge, and force the optimization of the curve fit (fig. 6, 7).

Parameter Extraction From AC Measurements

Forward transit time (t_F) is the sum of the emitter to collector time delays for carrier propagation through a transistor, and can be determined from the measurement of hfe over a range of frequencies and collector currents. The common emitter forward current gain is most easily derived for RF and microwave devices by first measuring the scattering parameters on a network analyzer, and then converting to the hybrid parameters. There are now a number of network analyzer systems available offering semi-automatic, and automatic, parameter extraction and calibration. Many systems offer on-line conversion from 's' parameters to other parameters including 'h' parameters. Determination of transit time from hfe then becomes a relatively simple task of plotting the inverse product of the forward current gain (hfe) and radian frequency

frequency intercept is given by [6]:

$$RE(h_{ie})=r_{bcon}+r_{b'}+r_{bb'}+r_{e'}+w_tL_e$$

The effect of the parasitic capacitances, C_{bc} and C_{be}, and the extrinsic collector junction capacitance, C_{0}, is to reduce the real component of h_{ie} by an amount depending on the magnitude of h_{ie}. Including this capacitance, and, as h_{in} approaches the real axis, at high frequency the real part of the input impedance can be approximated by [7]:

$$RE(h_{in})=RE(h_{ie})/(1+B^2*RE(h_{ie})^2)$$

where

$$B=2\pi f(C_{bc}+C_{be}+C_0)$$

Accurate determination of Rb by this method depends on a knowledge of the emitter inductance, and the parasitic package and transistor capacitances. For transistors with high ft, small values of base resistance are easily swamped by the dominant emitter inductance term.

Difficulties in measuring the 'h' parameters at high frequencies are best avoided by the more practical method of measuring the 'S' parameters. The base resistance is a function of the current, and this dependence is modeled in the circuit simulator by allocating a low and high current value for the base resistance, RB and RBM, and a current at which RB falls half way to the minimum value, IRB. Input impedance circles are required over a range of bias currents to determine these values (Fig. 12).

For class 'B' and 'C' amplifier simulations, RB can be represented by the high current value without much loss of accuracy.

Application of SPICE in Class 'C' Amplifier Design

Parameters determined by the above methods can be used to simulate the operation of class 'C' amplifier circuits and gain an appreciation of the various terminal current and voltage waveforms. SPICE has been used to simulate a rf transistor operating as a class 'C' amplifier at 870MHz with 12.5 Volt collector bias, with the results compared to the performance of an actual circuit.

The 12 cell interdigitated geometry used in this comparison was packaged in a UHF flange package, with double emitter wire bonds to minimize package inductance. The SPICE parameters were extracted on a single cell die to improve accuracy. These parameters were then scaled for the larger die and the package parasitics included. Measurements were made, at an output power of 5 Watts, of the input and output impedances at the fundamental, second and third harmonics. Impedance transforming networks on input and output were modeled to accurately represent the load seen by the transistor (Fig. 13). Since the performance, especially efficiency, is strongly dependent on the collector harmonic loading, operating conditions of the test amplifier were replicated as closely as possible. In a synthesis role the packaged transistor impedances would normally be calculated from the terminal current and voltage waveforms. SPICE was able to predict the gain within 0.5dB and the efficiency within 6% of the performance of the actual circuit.

Collector voltage for the initial 100 nsec after the start of the analysis is shown in fig. 14. Because the operation of the circuit is highly non-linear and certain of the circuit time constants are relatively long, a number of cycles need to be analyzed before the response reaches a quasi-static solution. The collector voltage waveform indicates a damped oscillation exists, eventually decaying after approximately 150 nsec. The oscillation is a resonance of the collector bias choke with the collector capacitance, and illustrates the need for long analysis periods.

Five cycles have been expanded in the subsequent plots to show the collector and base voltage and current waveforms (fig. 15, 16, 17). The collector and base current waveforms are forced to be sinusoidal by the active matching networks. SPICE also provides the facility for determining the circuit performance as a function of frequency, but only for small signal conditions, and therefore is unusable when the device is initially biased off.

Although SPICE does not provide circuit optimization capabilities, when allied with network synthesis and analysis programs (i.e. SUPERCOMPACT [9] or TOUCHSTONE [10]) circuit performace can be evaluated and the design checked to ensure maximum ratings are not exceeded. The effects of changes in the device parameters can also be assessed and the influence of parasitic components can be analyzed. This

is demonstrated by the influence on gain and collector efficiency of variation in emitter inductance shown in fig. 18.

Conclusions

While linear models for RF circuit response have been in use for some time, models based upon intrinsic transistor parameters have only recently found utility in predicting RF power amplifier response Extraction of these parameters from I-V, C-V and AC measurements is still, however, something of an art Utilizing these models to characterize the AC response of a class C amplifier gives insight into device design and process optimization, as well as circuit performance considerations.

To demonstrate this approach to computer aided design, a 12.5 Volt, 870 MHz, 5 Watt amplifier has been modeled, and the results discussed, especially model parameter extraction.

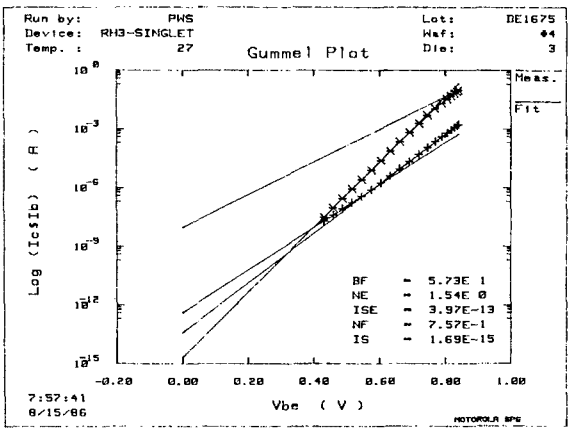

Fig. 1. Gummel Plot

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3. J. M. Early, "Effects of Space-Charge Layer Widening in Junction Transistors," Proc. IRE, Vol 40, pp. 1401-1406, November 1952.
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8. L. W. Nagel and D. O. Pederson, "Simulation Program With Integrated Circuit Emphasis (SPICE)" 16th Midwest Symposium on Circuit Theory, Waterloo, Ontario, April 12, 1973. All simulations run on SPICE2, available from the Electronics Laboratory of the University of Calif., Berkely.
9. SUPERCOMPACT, a software product of **Compact Software,** Palo Alto, Ca. (703-698-0215)
10. TOUCHSTONE, a software product of **EEsof**, Westlake Village, Ca. (818-991-7530)

ACKNOWLEDGMENTS

Special thanks to **Ivan Pesic** of **Silvaco Data Systems** for parameter extraction software support, **Tony Alvarez** of **Motorola** for helpful discussions, and to **Tom Baker** of **Motorola** for proof reading the text.

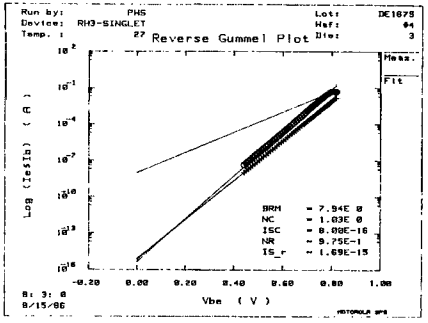

Fig. 2. Reverse Gummel Plot.

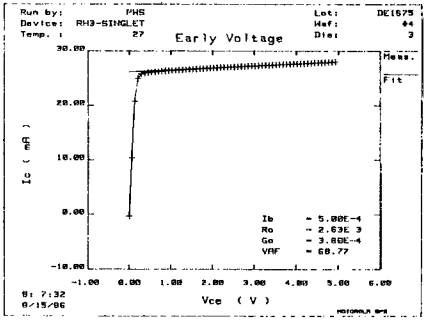

Fig. 3. Forward Early Voltage

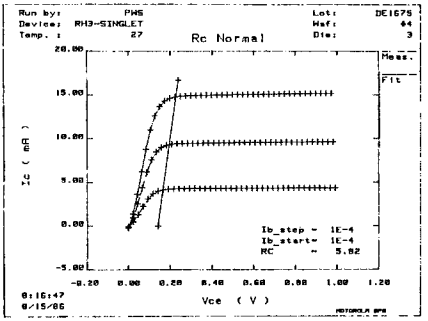

Fig. 4. Collector Resistance (RCactive).

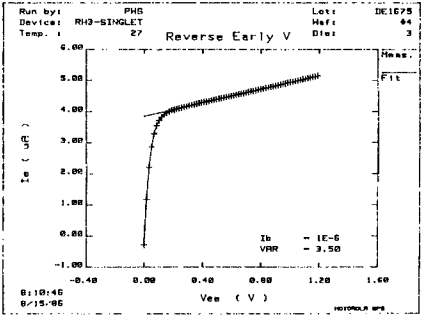

Fig. 5. Reverse Early Voltage.

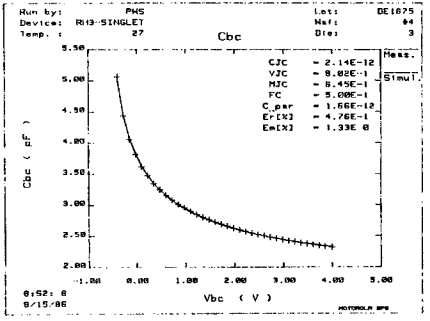

Fig. 6. Collector-Base Junction Capacitance

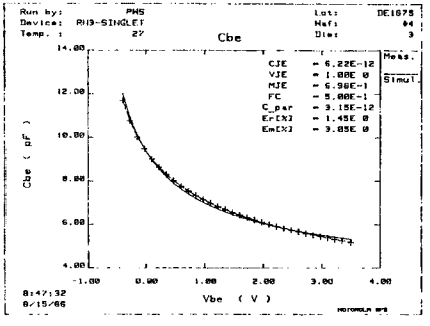

Fig. 7. Emitter-Base Junction Capacitance.

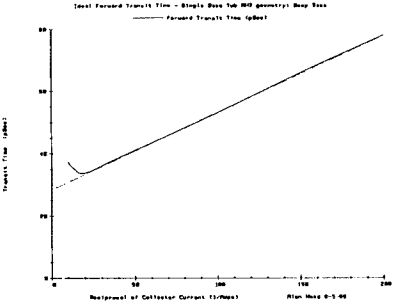
Ideal Forward Transit Time - Single Base Tub RH9 geometry: Deep Base
Forward Transit Time (pSec)
Transit Time (pSec)
Reciprocal of Collector Current (1/Amps)

Fig. 8. Forward Transit Time Extraction.

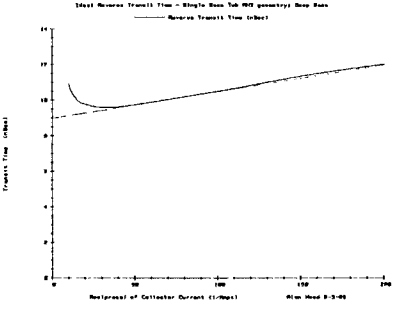
Ideal Reverse Transit Time - Single Base Tub RH9 geometry: Deep Base
Reverse Transit Time (nSec)
Transit Time (nSec)
Reciprocal of Collector Current (1/Amps)

Fig. 9. Reverse Transit Time Extraction.

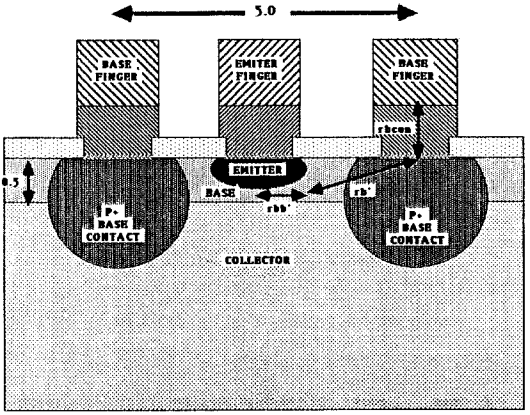

Fig. 10. Note that rbb' is the primary current dependent component of Rb.

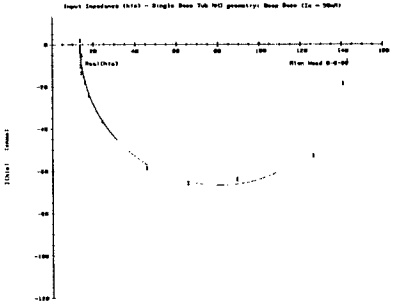

Fig. 11. Base Resistance Extraction From Impedance Circles

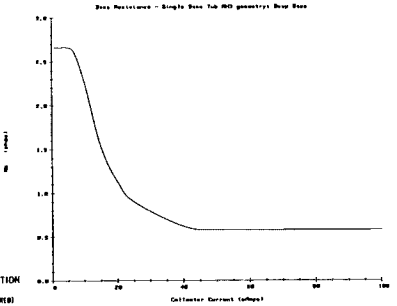

Fig. 12. Plot of Rb vs. Current.

DATA FILE FOR CIRCUIT SIMULATION

```
SIMPLE CLASS 'C' AMPLIFIER (12 CELL RHS WAFFLE)
VCC 9 0 12.5
RS 1 2 50
CB1 2 5 1000PF
LBC1 4 0 .60NH
CBBMM1 5 0 0.570PF
CBBMM2 4 0 56.12PF
LBBM1 5 4 2.41NH
LB  4 55 0.70NH
CEPM05 5 7 17.46PF
RMM 55 5
LC  10 0  0.50NH
CCPM05 6 7 9.54PF
LE  7 0 0.30NH
RECM 10 6
LCC 0 0 50NH
LSERI 8 10 2.859NH
CCSBMM1 10 15 2.807PF
LCSBMM1 15 0 0.090+6NH
LSER2 10 11 2.8592NH
RLOAD 14 0  50
TRL2 11 0 12 0 Z0=10.05 F=870+6E6 NL=0.0739
CSERI 12 13 45PF
LCSER2 13 14 0.77NH
RIN 1 0 RIMB 10 870+6E6
Q1 6 5 7 MOD1
.MODEL MOD1 NPN (BF=66.2 RBM=10 IS=0.758E-14 NF=0.929 NR=0.999
+          RB =0.225 RBM =0.956 IRB = 0.1600
+          CJE=56.6PF VJE=0.767 MJE=1.2
+          CJC=13.90PF VJC=0.575 MJC=0.061
+          RE=0.12 RC=0.982 XCJ=20 TR=7.29 ICRC=400+6 BRM=3.48
+          TF=0.020NS QTF=0  XTF = 3.56 VTF = -24  TR = 9.00NS  )  .
.TRAN 0.05NS 165NS 100NS
.OPTION IM=80 PNT = 00
.OPTIONS LIMPTS=2500 ITLS=50000
.FORM 870+6ES (F6)
.FORM 870+6ES (F6)
.PLOT TRAN V(2) V(5) V(6) (10)(C=0) V(14) (10)(M=1 10)(C=1
.END
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Fig. 13. SPICE File

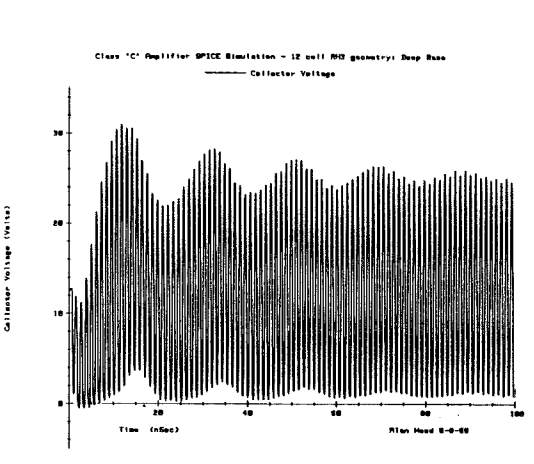

Fig. 14. Collector Waveform To 100ns

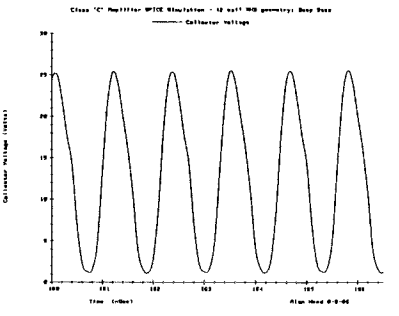

Fig. 15. Collector Waveform 160-166ns

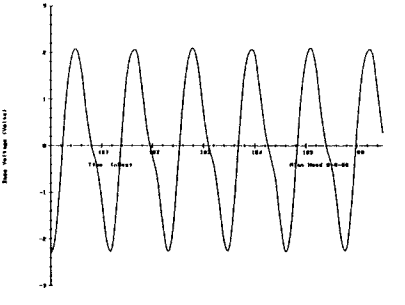

Fig. 16. Base Waveform 160-166ns

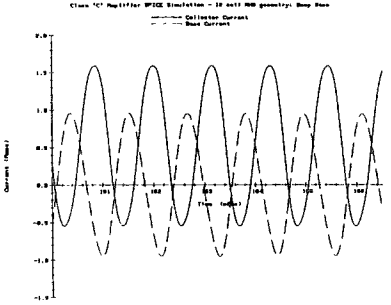
Class 'C' Amplifier SPICE Simulation - 10 volt MRD geometry; Beep Base
Collector Current
Base Current
Current (Amps)
Time (nsec)

Fig. 17. Collector and Base Waveforms 160-166ns

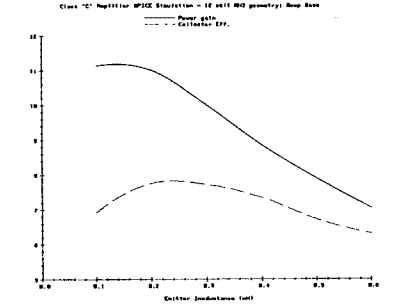
Class 'C' Amplifier SPICE Simulation - 12 volt MRD geometry; Beep Base
Power gain
Collector Eff.
Gain (dB), Eff. (%dB)
Emitter Inductance (nH)

Fig. 18. Amplifier Gain and Efficiency vs. Emitter Inductance

HOW TO SPECIFY PIN DIODE SWITCHES

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7311 G Grove Road
Frederick, MD 21701

I INTRODUCTION

When purchasing PIN diode swithces, it is important that they are completely specified to assure system performance. It is also important that the specification be achievable. This paper is designed to help a systems designer specify realizeable PIN diode switches.

There are six key parameters essential to specify pin diode switches. These are:

1) TYPE i.e., SPST, SPDT, SP3T, DPDT, etc.
2) OPERATING FREQUENCY BAND
3) INSERTION LOSS
4) *ISOLATION*
5) SWITCHING SPEED
6) POWER HANDLING

There are five secondary parameters that may require specification. These are:

1) LOGIC COMPATIBLE DRIVER TYPE AND SPEED.
2) PHASE TRACKING ARM TO ARM AND/OR UNIT TO UNIT.
3) OFF ARM TERMINATIONS.
4) *INTERCEPT POINT OR COMPRESSION POINT*
5) VIDEO TRANSIENTS

II SWITCH TYPE

Most PIN diode switches are of the single pole multiple throw type. They range from single throw up through 8-12 throws. The most popular type is the SPST or pulse modulator type. In general the greater the number of throws, the less popular the switch and, hence the less readily available it is. American Microwave has standard switch designs up through 5 throws *in the three popular bands of interest HF, UHF/VHF, and Microwave.* We also have designs for 8 and 10 throws at HF and Microwave.

The most popular multi-pole switch is the DPDT type, commonly known as the TRANSFER SWITCH. These units are available in UHF/VHF and Microwave bands. High order multi-pole switches are generally referred to as switch matrices, which is a whole subject matter by itself.

III OPERATING FREQUENCY BANDS

American Microwave classifies PIN switches into five operating frequency bands. *They are:*

a) VIDEO which covers from 10KHZ to 2MHZ, not manufactured at AMC.
b) HF which covers 2MHZ to 32MHZ, AMC series SW-0230 switches.
c) UHF/VHF covering 10MHZ to 2000MHZ, AMC series SW-2000 switches.
d) MICROWAVE covering 10MHZ to 20GHZ and above, AMC series SW-218 switches.
e) Milimeter wave switches, 20GHZ and up.

The above bands have loosely defined boundaries which overlap. They are *indicative of the five* different technologies available to the switch

manufacturer as well as four distinct applications areas of switch requirements.

There are some special application bands and technologies such as the high speed, low transient IF switching technology which is reflected in the SW8-0070 series of switches in the AMC catalog.

IV THE PIN DIODE

A simplified equivalent circuit of the PIN diode is shown in figure 1. The forward biased diode is a current controlled resistor. The resistance vs current behavior of a typical PIN diode is shown in figure 2. The reversed biased diode is a voltage controlled capacitor. The capacitance vs voltage of a typical PIN diode is shown in figure 3.

V INSERTION LOSS

Simple,most basic switches have the lowest loss for any given operating band. For a given technology or operating band, insertion loss increases with increasing frequency proportional the square root of frequency in a well designed PIN switch. Insertion loss originates in four basic areas.

a) Conductor or transmission line loss within switch itself due to the presence of microstrip, coaxial line or waveguide interconnecting lines.

b) Resistance losses due to finite resistance of series connected components such as PIN diodes and/or finite "Q" capacitors.

c) VSWR losses due to mismatch of components within the switch or at the terminals of the switch. VSWR losses at the terminals of the switch can be tuned out externally to improve losses, those within the switch must be minimized in design. These actually are the cause for ripples in the insertion loss vs frequency characteristic.

Assuming a switch is well designed, i.e., lowest loss transmission media, lowest resistance diodes and other series components are employed and all internal VSWR's are minimized, the loss of the switch is then dependent on the complexity of the design. In general, multi-throw units are more lossy as the number of throws increases. The addition of off-arm terminations and video filters increases the loss of the switch for a given technology. Also increased on/off isolation will contribute slightly to the loss. The insertion loss is lowest in the least complex switch configurations. For low loss switches, keep the specification simple.

VI ISOLATION

PIN diodes are connected to the transmission line in series or in shunt. Isolation is achieved by reverse biasing series connected diodes or forward biasing shunt connected diodes. The shunt mounted diode provides the most effective means for achieving broadband, relatively frequency independent isolation. It is ideally frequency independent but practically, small parasitic reactances generally affect broadband performance. Isolation is also acheived by reverse biasing series mounted diodes. Isolation for the series mounted diode decreases with increasing frequency.

Series-shunt diode configurations are frequently employed in multithrow broadband switches to achieve relatively high isolation in a simple structure. An example of the performance of a series-shunt connection is shown in figure 4 for the AMC model SW-218-2 switch. Note how the isolation decreases with increasing frequency. Multiple diodes connected in series or in shunt are frequently employed in PIN switches to achieve relatively high isolation over

a broad band of frequencies. The isolation vs frequency characteristic of a shunt connected array of forward biased diodes is the AMC model SW-2184-1A SPST unit, shown in figure 6 which achieves 85dB isolation over the 2-18GHZ band by judiciously spacing four shunt connected diodes. An example of a switch employing an array of reverse biased series connected diodes is the AMC model SW-2000-1, shown in figure 7, which achieves 70dB minimum isolation over the 10-2000MHZ band. It is interesting to note that the SW-2000-1 unit has more insertion loss at the low end of the band than that of the SW-218-1A unit. This of course is due to the finite resistance of the forward biased series diodes in the SW-2000-1 unit.

For narrowband applications, the possibilities are endless for combining and tuning diodes for excellent tradeoffs between insertion loss and isolation. Many designers have employed series and shunt inductors to resonate the capacitance of reverse biased PIN diodes to achieve excellent isolation-insertion loss performance over limited frequency bands. (see reference 1)

VII SWITCHING SPEED

Switching speed of a PIN diode switch is generally defined as the time for the RF to traverse 10% to 90% levels. Other definitions such as the time from 1dB to 60dB levels are occasionally employed for high isolation requirements. The switching speed is generally controlled by two factors, the time required to remove the stored charge from the diode junction and the theoritical maximum speed at which the charge can be removed from the junction. The time required to remove the stored charge from the junction is limited by the transit time of the PIN diode. The transit time is given by

$$It=W1/Vs$$

where Wl= the device I-region thickness (cm)

Vs=maximum saturated velocity= 10exp7 cm/sec

The I-region thickness is related to the breakdown voltage Vb by

$$Wl=Vb/2C$$

Additionally, the stored charge in the forward biased diode junction is related to the monority carrier lifetime of the junction by

$$Qs=I*T$$

where Qs=stored charge (coulombs)

If=forward current (amperes)

T=minority carrier lifetime (seconds)

As a minimum for operation as a PIN switch the diode lifetime is shown vs the lowest operating frequency in figure 8. Further, the transit time as a function of breakdown voltage is shown in figure 9. (see reference 2) For minority carrier lifetimes shorter than 10ns, state-of-the-art PIN drivers can switch in approximately the transition time of the device. Longer lifetimes require higher currents and larger, slower switching transistors causing switching times to be longer than the transition time.

Low intermodulation and harmonic distortion PIN switches require diodes with longer than minimum minority carrier lifetimes and hence switch more slowly.

High power PIN switches require higher Vb diodes which results in slower transition times and slower switching times.

VIII POWER HANDLING

The power handling capability of PIN diode switches is controlled by three parameters. First is the upper operating temperature of the device. Second is the breakdown voltage and third the charge storage capability of the device. For silicon PIN diodes, best reliability is achieved by keeping junction operating temperatures below 200 degrees centigrade. Since series mounted diodes are more dissipative and have poorer heat sinking capabilities than shunt mounted configurations switch designers tend to avoid series configurations in high power applications. Since series configurations are essential to wideband multi-throw switches, these units tend to be the lowest power handling configurations. Hence, high power broadband switches are difficult to realize. One usually ends up trading power for bandwidth.

It is necessary that the breakdown voltage be at least twice the peak RF voltage that the diode will see and that the forward charge stored in the junction be greater than the charge moved on one-half cycle of the RF current waveform. The former requirement will assure that the diode not exceed its voltage breakdown and the latter that the forward biased junction will not be depleted in operation. The elements are essential to linear non-destructive operation of the diode under high power operation.

IX LOGIC COMPATIBLE DRIVERS

The three most popular logic families are Transistor-Transistor-Logic (TTL), Emitter Coupled Logic (ECL) and Metla Oxide Semiconductor (MOS/CMOS).

Of the three, TTL logic is by far the most popular. ECL and CMOS are a distant second. Four of the most popular forms of TTL driver circuits are shown in figure 10. We will confine this discussion to TTL compatible drivers. For best performance, switch drivers must be electrically as well as mechanically integrated in the switch unit. It is possible to achieve clean, transient free switching by designing electrically compatible drivers.

"Unit load" drivers are highly desirable because they are compatible with the widest range of TTL product line I.C.'s. A "unit load" is defined as 40 microamperes maximum source current and 1.6 milliamperes maximum sink current. Drivers are available in multiples of "unit load". True TTL compatibility also requires a logic "low" to be 0-.8 volts and a logic "high" to be 2.0-5.0 volts at the input (0.8-2.0 volts is an undefined region).

All TTL compatible drivers have delay. Generally the driver delay is defined as the time from 50% TTL level to where the RF signal changes by 10%. i.e., 0-10% for turn-on or 100-90% for turn-off. It is caused by energy storage in the driver and/or RF circuitry. The delay is a result of the time required to remove the stored energy before the switch state can be changed. The stored energy can be stored charge in the base region of a switching transistor or stored in various capacitors and inductors in the driver circuit or the bias decoupling circuit. Often this delay is different for turn-on and turn-off. This phenomenon can lead to pulse shrinkage or pulse expansion when the PIN switch is operated in a pulse mode. Since driver delay is consistent from unit to unit in a well designed PIN switch, a systems designer can often pre-trigger the switch and essentially "program-out" the driver delay. When it is not possible to anticipate the delay, it is necessary to specify delay equalization. An example of a PIN switch with equalized delay is the AMC model SW-218-1A series pulse modulator with modulation characteristics shown in figure 11. This unit has on/off delay equalization to 5ns, maximum.

Another phenomenon of driver delay is minimum pulse width. Since delay involves charging and discharging of components within the driver circuit, it isnecessary to "charge" or "discharge" the driver before any RF changes in signal level are observed. This results in a minimum pulse width for any switch with integral logic drivers. The minimum pulse width is approximately equal to the delay in the driver.

X PHASE TRACKING

Often systems require switches that are "phase tracked". A phase tracking requirement is best achieved by first equalizing the time delay between arms of a multi-throw switch (if a multi-throw is indicated) and equalizing the time delay from unit to unit within a production run or product line if required.

Since the PIN switch is made up internally of many elements, i.e., diodes, capacitors and chokes with their accompanying mounting parasitic reactances and losses, it is necessary to control the uniformity of parts and assembly techniques to achieve best phase tracking.

For unit-to-unit phase tracking on a lot-to-lot basis, it is necessary to build a phase standard unit that is maintained at the switch vendor's facility which has an impact on the price of the initial lot of switches.

Typical state-of-the-art phase tracking is as follows:

BAND	PHASE TRACKING
HF	1 Degree
UHF/VHF	2 Degrees
MICROWAVE	10 Degrees

XI OFF ARM TERMINATIONS

Often PIN switches are employed to commutate or switch VSWR sensitive components such as antenna elements in an array, oscillators or amplifiers. Normally switches have an infinite VSWR in the OFF position. Figure 12 shows a switch with off arm terminations having an extra switching section that switch the terminal in question into a matched load when that arm is turned off. This in effect controls and stabilizes the VSWR in both the ON and OFF condition of the switch. You must specify off arm terminations when it is necessary to control OFF VSWR.

Be aware that when the specified arm is commutated or switched there is a period of time when the VSWR is unspecified. This is particularly important in high power switches where momentary high reflected power levels can be troublesome.

The addition of off arm terminations adds complexity to the switch which results in additional insertion loss and poorer phase tracking.

XII INTERCEPT POINT OR COMPRESSION POINT

Compression in a PIN switch is a less well defined parameter than in say an amplifier. So we will limit our remarks in this section to intercept point. The concept of intercept point is well documented in the literature and we will not go into it here. Rather we will examine the elements that control intercept point of PIN diode switches and their tradeoff on overall switch performance.

Intermodulation is a result of nonlinear mechanisms within the PIN diode primarily and occasionally caused by other elements such as nonlinear capacitors, resistors and/or ferrite cores in the bias decoupling chokes. We will confine this discussion to the PIN diode only.

The primary intermod generator in a PIN switch is the forward biased series PIN diode. Intermod is generated in the diode when the stored charge becomes close to being swept out (or depleted) from the I layer region. Hence low intermod switches employ diodes with longer than minimum minority carrier lifetimes and are biased at relatively high forward currents to store a lot of charge in the junction. The degree of linearity is controlled by the percentage of charge depleted from the junction by the RF cycle. Highly linear switches have small percentages of charge depletion.

A secondary intermod generator is the non-linear capacitance vs voltage characteristic of the reversed biased PIN diode. This phenomenon is relatively easily controlled by selecting diodes with flat capacitance vs voltage characteristics and biasing the device into that region of the curve.

XIII VIDEO TRANSIENTS

Refer to figure 13, the equivalent circuit of a typical PIN switch. When the diodes are switched between biasing conditions a change on voltage or current occurs at the bias decoupling element adjacent to the output terminals. This element acts to differentiate the waveform (current for the shunt inductor and voltage for the series capacitor) and cause a pulse, spike or video transient at the output terminal. This transient occurs in all PIN switches but is controllable by various means.

The most effective means of controlling video transients are:

1) Slowing the switching waveform
2) Filtering the video spectrum
3) Balancing or cancelling two equal video transients

The first is very effective when switching speed is not important. Slowing the switching waveform will slow switching speed. The second is effective when the switch operating band is above the frequency band where the video spectrum is concetrated. The addition of high pass filters at the input and output terminals of PIN switches at frequencies above 500MHZ has proven very effective in reducing transients. Typically the highest speed switches (1NS) have at least 90% of the video spectrum below 1GHZ. Filtering has its accompanying side effects. It will often introduce unwanted "ringing" in the switching waveform. Balancing has been employed very effectively as a means of reducing video transients without affecting switching speed or introducing "ringing". Unfortunately present state-of-the-art technology has limited balancing technique to UHF/VHF band. An example of the balancing technique is the AMC SWB-0070 series of IF switches shown in figure 14.

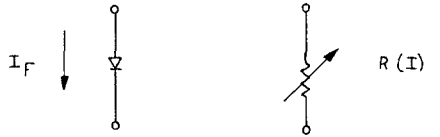
XIV CONCLUSION

Six essential and five supplementary parameters have been presented to aid in the specification of PIN diode switches. Tradeoffs between the various parameters have also been explored. It is hoped that this will help bridge the gap between switch users and switch designers.

A sample specification is presented in figure 15 to serve as a prototype switch specification to aid in bridging the gap.

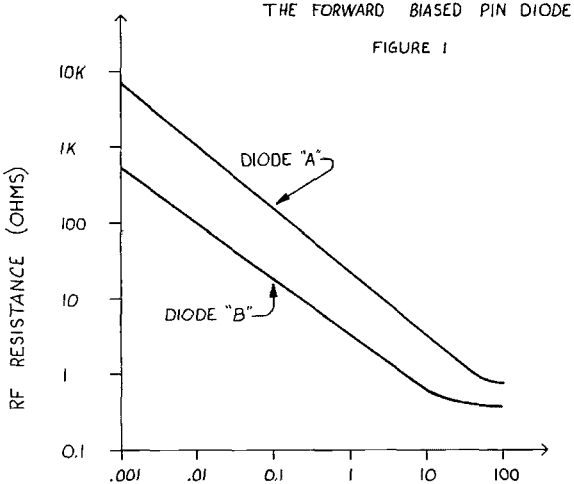
REFERENCES:

1. R.N. Assaly, "PIN Diode Switches for Space Applications", MTT, 1967
2. M/A COMM PIN Diode Designers' Guide, 1983.



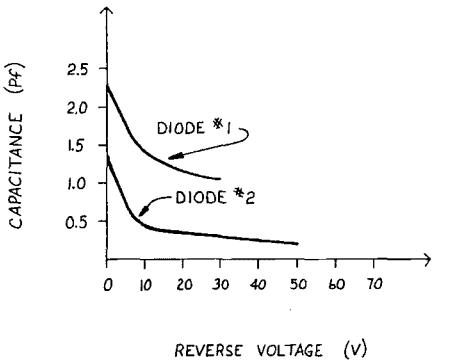
THE FORWARD BIASED PIN DIODE

FIGURE 1



RF RESISTANCE VS. FORWARD BIAS CURRENT

FIGURE 2

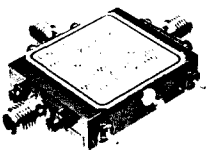


PIN DIODE

CAPACITANCE VS. VOLTAGE

FIGURE 3

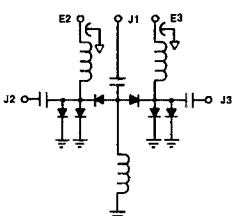
*BROADBAND PIN SWITCH SPDT
SW-218-2
0.3 TO 18 GHz



FEATURES

- 0.3 to 18 GHz Frequency Range
- Low Insertion Loss
- Small Size
- Light Weight
- Rugged Chip and Microstrip Construction

FUNCTIONAL SCHEMATIC



6/85

SPECIFICATIONS

- Frequency Range: 0.3 to 18 GHz
- Insertion Loss: 2.5 dB, Max.
- Isolation: 55 dB, Min.
- VSWR: 2.0 to 1
- Switching Speed: 100 μs typ.
- Bias: Port on: −50ma
  Port off: +30ma
- Power Handling: +20 dBm, CW, Max.
- Operating Temp.: −85° C to +85° C

DESCRIPTION

The SW-218-2 is a SPDT Pin Switch intended for wide band switching applications in commercial and military environments. It has an instantaneous frequency coverage from 0.3 to 18 GHz and features all solid state chip diode and microstrip construction for rugged, reflable operation.

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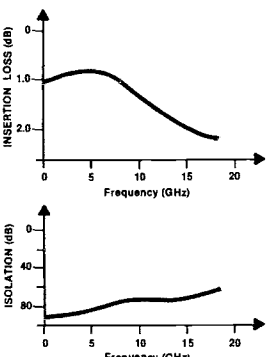
4

SPECIFICATIONS, Cont'd.

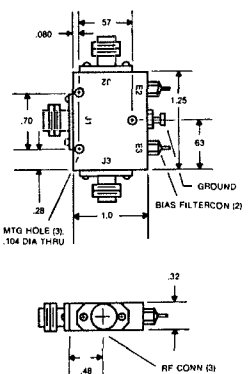
FREQUENCY (GHz)	0.3	0.2	4.0	8.0	12.0	18.0
MAX. INSERTION LOSS (dB)	1.2	1.2	1.1	1.0	1.8	2.5
MIN. ISOLATION (dB)	85	80	75	70	85	55
MAX. VSWR	1.7	1.5	1.5	2.0	2.3	2.3

HUMIDITY, SHOCK, ETC. PER MIL-STD 202C
CONNECTORS: 1) RF: SMA FEMALE
2) BIAS: FEED THRU FILTER-SOLDER PIN
3) CONFIGURATION OPTIONS:
001- ONE MALE AND TWO FEMALE SMA CONNECTORS
002- TWO MALE AND ONE FEMALE SMA CONNECTORS
003- THREE MALE CONNECTORS

TYPICAL PERFORMANCE

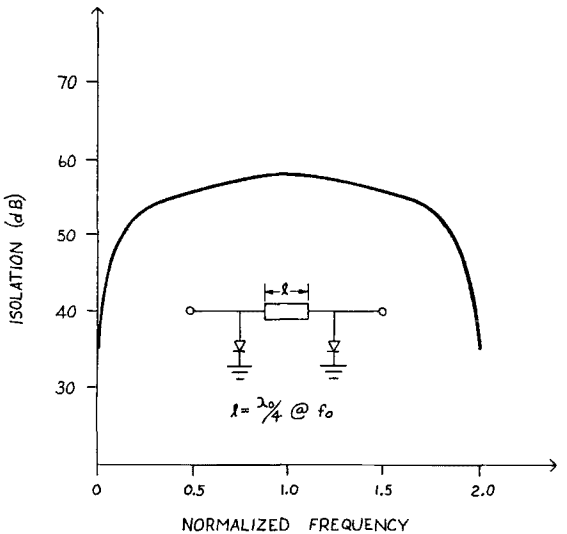


MECHANICAL DATA



SERIES SHUNT CONFIGURATION

FIGURE 4



ISOLATION VS. FREQUENCY, SHUNT ARRAY

FIGURE 5

*SERIES SW-218 WIDEBAND SPST PIN DIODE SWITCHES WITH INTEGRAL DRIVERS

FEATURES

- 0.3 to 18 GHz Frequency Range
- Low Insertion Loss
- Up to 85 dB Isolation
- High Speed - 10 nsec
- Small Size
- Light Weight
- Rugged Chip and Microstrip Construction

DESCRIPTION

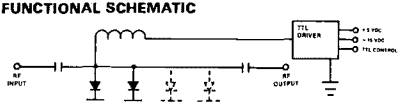
The series SW-218 switches are broadband, high speed, low loss SPST switches with integral drivers. They are powered by +5 and −15 volt supplies and are available powered by ±15 volts. They are available in three models that operate over the entire 0.3 to 18 GHz band. Each features rugged integrated circuit assemblies of chip PIN on a microstrip transmission line and proprietary wideband bias decoupling circuitry.

Switching is accomplished by a TTL compatible driver which is controlled by the user.

SPECIFICATIONS

- Control Impedance - TTL Compatible, One Load. (A Load is 1.6 mA Sink Current and 40 µA Source Current.)
- Control Logic - Logic "0" (−0.3 to +0.7 Volt) for Switch OFF. Logic "1" (+2.5 to +5.0 Volts) for Switch ON.
- Temperature - Operating: −85°C to +85°C Non-operating: −65°C to +125°C
- Humidity, Shock, Etc. - Per MIL-STD 202C

FUNCTIONAL SCHEMATIC



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6

SPECIFICATIONS, Cont'd.

MODEL NO.	CHARACTERISTICS	FREQUENCY (GHz) 0.3 to 1.0	1.0 to 2.0	2.0 to 4.0	4.0 to 8.0	8.0 to 12.4	12.4 to 18.0	SWITCHING* SPEED ON-to-OFF and OFF-to-ON	POWER HANDLING CAPABILITY AVG (WATTS)	Peak 1 µsec. max. pw (WATTS)	POWER SUPPLY + 15 VDC	+ 5 VDC	– 15 VDC
SW-2182-1A	Min Isolation (dB)	30	40	45	45	45	45	10 ns	2	10	55 mA	55 mA	35 mA
	Max Ins Loss (dB)	1.0	1.0	1.0	1.1	1.6	2.0						
	Max VSWR (ON Pos)	1.3	1.3	1.4	1.6	1.9	1.9						
SW-2183-1A	Min Isolation (dB)	40	60	70	70	70	70	10	2	10	65 mA	65 mA	35 mA
	Max Ins Loss (dB)	1.0	1.0	1.1	1.4	1.8	2.3						
	Max VSWR (ON Pos)	1.4	1.4	1.4	1.6	1.9	1.9						
SW-2184-1A	Min Isolation (dB)	45	70	85	85	85	80	10	2	10	75 mA	75 mA	35 mA
	Max Ins Loss (dB)	1.0	1.0	1.2	1.5	2.0	2.5						
	Max VSWR (ON Pos)	1.4	1.4	1.4	1.6	1.9	1.9						

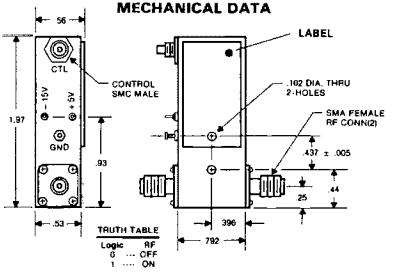
*Switching speeds are 10% to 90% RF and 90% to 10% RF. Standard TTL delay is 20 ns, Max from 50% TTL to 90% RF for turn-off and 50 ns, Max from 50% TTL to 10% RF for turn-on.

FIGURE 6

AVAILABLE OPTIONS

Option No.	Description
001	Two SMA Male RF Connectors
002	One SMA Male and One SMA Female RF Connector
003	Solder Type Control Terminals
004	± 15 Volt Power Supply Requirement (+ 5, – 15 Volt is Standard)
005	50 Ohm Control Impedance
006	Cannon Multipin MDM9SSP
007	Inverted Logic
008	Extend Frequency to 100 MHz
009	20 ns, Max Delay
010	100 ns, Max Switching Speed
011	
012	2 ns, Max Switching Speed

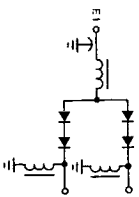
MECHANICAL DATA



FEATURES

- Wide Bandwidth - 10-3000 MHz
- Low Insertion Loss
- Solid State Reliability
- Available up to SP5T
- High Intercept Point
  - +80 dBm 2nd Order
  - +45 dBm 3rd Order
- TTL Control Available

FUNCTIONAL SCHEMATIC



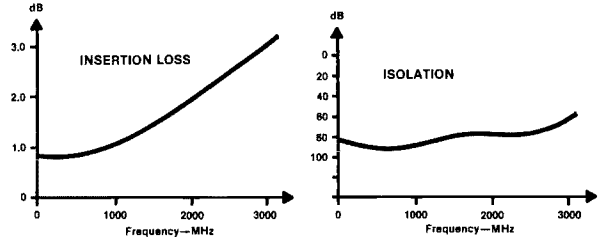
SPST PIN DIODE SWITCH
MODEL SW-2000-1
10-3000 MHz

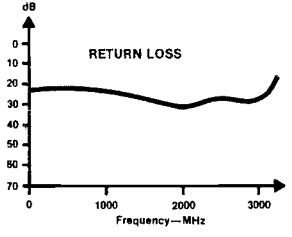
SPECIFICATIONS

- Frequency Range: 10-3000 MHz
- OFF Isolation:
  - 10-1000 MHz 80 dB, Min
  - 1000-2000 MHz 70 dB, Min
  - 2000-3000 MHz 60 dB, Min
- ON Insertion Loss:
  - 10-500 MHz 1.0 dB, Max
  - 500-1000 MHz 1.5 dB, Max
  - 1000-2000 MHz 2.5 dB, Max
  - 2000-3000 MHz 3.5 dB, Max
- VSWR: 50 Ohms
- Harmonic Distortion:
  - 2nd Harmonic: – 60 dBc @ 0 dBm
- Switching Speed: 5 µs, typical
- Bias:
  - ON Port 100 ma, Max
  - OFF Port – 25 µ, Max.
- Temperature Range: – 55 to + 85 Deg C
- RF Connectors: SMA

FIGURE 7

TYPICAL PERFORMANCE





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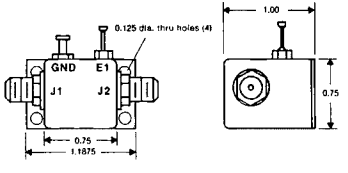
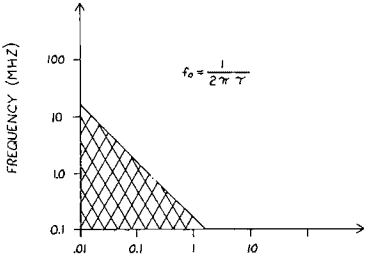
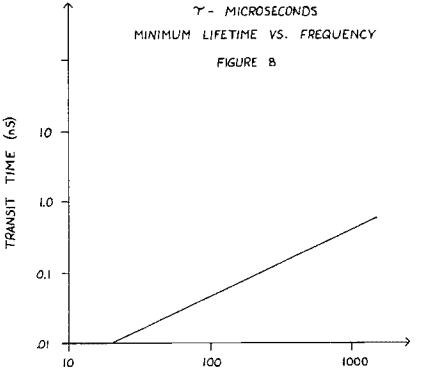


FIGURE 7



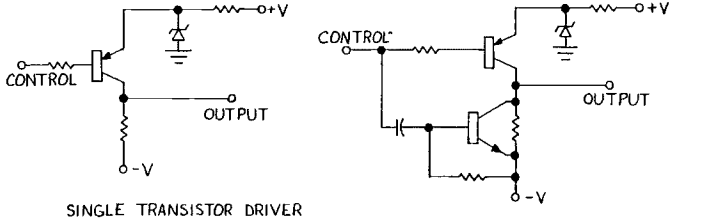
MINIMUM LIFETIME VS. FREQUENCY

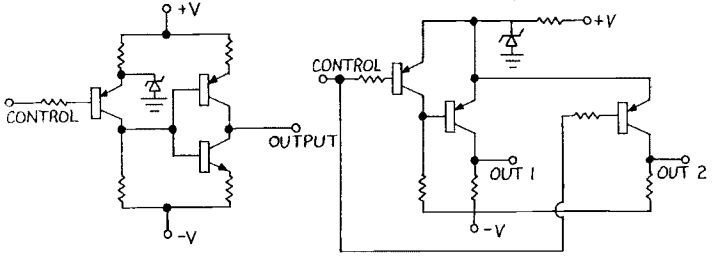
FIGURE 8



TRANSIT TIME VS. BULK BREAKDOWN VOLTAGE

FIGURE 9





TTL DRIVER CIRCUITS
FIGURE 10

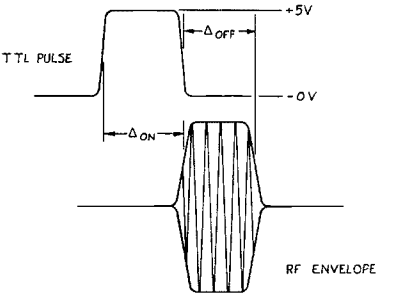


FIGURE 11

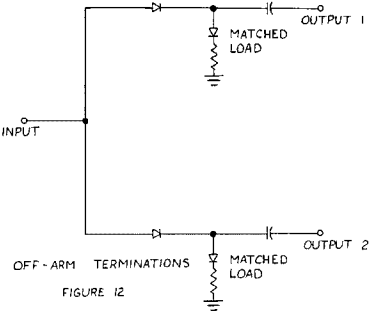
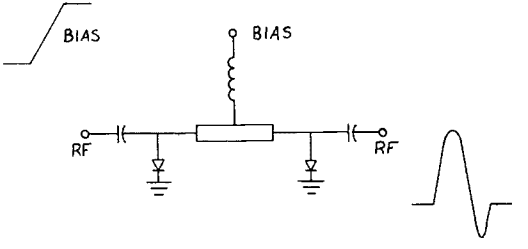
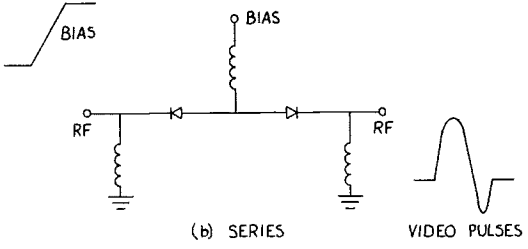


FIGURE 12

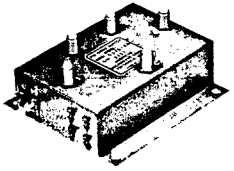




PIN SWITCH EQUIVALENT CIRCUITS

FIGURE 13

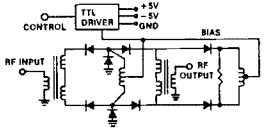
SWB-0070 SERIES
HIGH SPEED I.F. SWITCHES
WITH TTL DRIVERS
50 - 90 MHz



FEATURES

- HIGH SPEED: 10 ns, Max
- LOW TRANSIENT: 50 mv, Max
- Reverse Polarity Protection
- 300% Overload Protection for Up To 2 Minutes
- Rugged Microstrip Construction
- Integrated TTL Drivers
- HIGH ISOLATION: 70 dB, Min
- Off-arm Terminations
- SPST Thru SP8T Configurations

FUNCTIONAL SCHEMATIC (SPST)



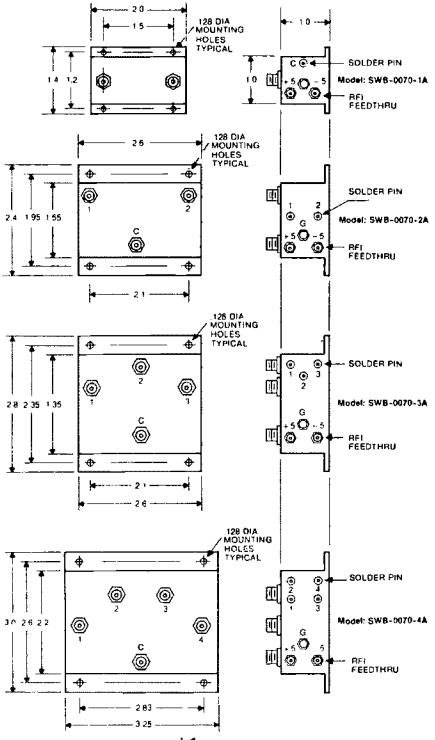
SPECIFICATIONS

TYPE	MODEL
SP5T	SWB-0070-1A
SP2T	SWB-0070-2A
SP3T	SWB-0070-3A
SP4T	SWB-0070-4A
SP5T	SWB-0070-5A
SP6T	SWB-0070-6A
SP7T	SWB-0070-7A
SP8T	SWB-0070-8A

- Frequency Range: 50-90 MHz
- Insertion Loss: 1.5 dB, Max
- Isolation: 70 dB, Min
  80 dB, Typ
- Switching Speed: TTL Delay: 5 ns, Max
  10%-90% RF: 10 ns, Max
  90%-10% RF: 10 ns, Max
- Video Transients: 50 mv, Max
- Return Loss: Input: - 17 dB, Min
  Output (on): - 17 dB, Min
  Output (off): - 14 dB, Min
- Intermodulation:
  3rd Order: 2 Tones @ +7 dBm, - 50 dBc

FIGURE 14

MECHANICAL DATA



14

AMERICAN MICROWAVE CORPORATION

SWITCH SPECIFICATIONS DATA SHEET

CUSTOMER:_____ MODEL:_____ OPT:_____

1.0 CONFIGURATION:

2.0 FREQUENCY BAND (GHZ):

3.0 INSERTION LOSS:

3.1) MAXIMUM:
3.2) VARIATION:

4.0 ISOLATION:

4.1) MINIMUM:
4.2) TYPICAL:

5.0 SWITCHING SPEED:

5.1) 50% TTL TO 90% RF
5.2) 50% TTL TO 10% RF
5.3) 10% RF TO 90% RF
5.4) 90% RF TO 10% RF

6.0 VSWR:

6.1) INPUT
6.2) OUTPUT (ON)
6.3) OUTPUT (OFF)

7.0 RF POWER:

7.1) CW
7.2) PEAK POWER
7.3) PULSE DUTY RATIO

8.0 CONTROL: NO DRIVER ☐
TTL DRIVER ☐
TTL DECODER ☐

9.0 POWER SUPPLY:

VOLTAGE	CURRENT (mA)
+5	
+15	
-5	
-15	

10.0 CONNECTORS:

10.1) RF: SMA N BNC TNC
10.2) POWER: MULTI-PIN SOLDER PIN
10.3) CONTROL: SOLDER PIN SMC SMA

11.0 INTERCEPT POINT:

11.1 3rd ORDER
____dBm @ ____dBm input power

11.2 2nd ORDER
____dBm @ ____dBm input power

12.0 VIDEO TRANSIENTS:

____MV, MAX

13.0 PHASE TRACKING:

____DEGREES MAXIMUM DEVIATION

FIGURE 15

A Low Noise Fiber Optics Receiver/Amplifier in VHF Range

by
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Signetics Corporation
P.O.Box 3409, Sunnyvale, Ca 94088-3409

Despite numerous advantages, the relatively high cost of fiber-optic transmission prevented its wide-spread industrial acceptance. High bandwidth-distance products, a prerequisite for cost-effectiveness, could not be achieved with relatively inexpensive components. The latest technological advances on both transmitter and receiver sides, however, are about to change that.

Transmittar

Starting at the transmitter side (Figure 1), the two major problems of the past were the unavailability of inexpensive, light emitting diode (LED) transmitters, capable of 10-20 MHz modulation rates, and the compounded problem of cost and reliability of laser diodes, required for large channel capacity, single mode, long-distance systems.

In examining the present status of the fiber-optic industry we observe, however, that new generations of LEDs, used in most *short-range*, multimode transmitters, can achieve wide modulation bandwidths, enabling system designers to develop cost-effective systems. For example, commercially available 820-850 nanometer AlGaAs surface emitting devices have significantly decreased in price and can be used up to and beyond 100 MHz (200 MBaud). InGaAsP LEDs can be used in the 1.3μm range. Their highly doped versions can be modulated up to bandwidths of several hundred MHz at the expense of lower output power.

InGaAsP laser diodes can go well beyond 1GHz. Their higher output power and an order of magnitude narrower spectral widths make these devices the ideal choice for *long-range*, very high data rate telecommunication systems.

Racmivar

The key to cost effectiveness at the receiver side is the ability to offer monolithic IC building blocks that can match those high transmitter data rates with bandwidth, large dynamic range and low noise. These kinds of IC building blocks weren't readily available in the past. Consequently, system designers had to choose between limiting data rates to below 20 MBaud or using costly hybrid modules.

Signetics' solution to the problem is the introduction of the SE/NE5212 trans-impedance amplifier (TIA).

Although the real meaning is different, "trans-resistance" and "trans-impedance" are used interchangeably in practice. These names designate that these types of amplifiers are current-driven at their inputs and generate voltage at their outputs. The transfer function is therefore a ratio of output voltage to input current with dimensions of ohms. Since the input is current driven, the input resistance must be low, which means low input voltage swings, no capacitive charge/discharge currents and wide frequency response with a generous phase margin.

Alternative approaches to the TIA, such as high input impedance FET preamplifiers with a shunt input resistor, tend to be more bandwidth limited. They exhibit integrating characteristics, and therefore must be

equalized by a differentiating second stage to achieve broad frequency response. The integrating input stage, however, is prone to overload with signals that have high low-frequency content. If the amplifier overloads for any reason, the integrated waveform cannot be restored by differentiation and dynamic range suffers despite the low noise characteristics.
Since the trans-impedance configuration does not have this problem, its superior dynamic range, inherently large bandwidth and compatibility with low cost IC technologies make it an attractive approach.

The NE5212

The NE5212 TIA is a low noise, wide band integrated circuit with single signal input and differential outputs, ideally suited for fiber optic receivers in addition to many other RF applications.
As shown in Figure 2, a differential output configuration was chosen to achieve good power supply rejection ratio and to provide ease of interface with ECL type post-amplifier circuitry. The input stage (A1) has a low noise shunt-series feedback configuration. The open loop gain of A1 (R_F=infinite) is about 70; therefore, we can assume with good approximation an input stage trans-resistance equal to the value of R_F=7.4 KOhms. Since the second stage differential amplifier (A2) and the output emitter followers (A3 and A4) have a voltage gain of about two, the input to output trans-resistance is twice the value of R_F, about 14.5 KOhms. The single-ended trans-resistance is half of this value.
Returning to the input stage (Figure 3), a simple analysis can be used to determine the performance of the TIA. The input resistance, R_{in}, can be calculated as

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{R_F}{1 + A_{VOL}} = \frac{7400}{1 + 70} = 104 \text{ Ohms}$$

More exact calculations lead to a slightly higher value of 110 Ohms.
The collector-base capacitance ($C_{\mu 1}$=0.12 pF) of Q1 is by far the largest contributor to the input capacitance due to the Miller-effect:

$$C_{in} = C_{\mu 1} (1 + 70) = 9 \text{ pF}$$

Thus, while neglecting driving source- and stray capacitances, C_{in} and R_{in} will form the dominant pole of the entire amplifier:

$$f_{-3dB} = \frac{1}{2\pi R_{in} C_{in}} = \frac{1}{2\pi R_F C_{\mu 1}} \qquad f_{-3dB} = \frac{1}{2\pi \, 7.4 \times 10^{3} \times 0.12 \times 10^{-12}} = 180 \text{ MHz}$$

Although significantly wider bandwidths could have been achieved by a cascode input stage configuration, the present solution has the advantage of a very uniform, highly de-sensitized frequency response because the Miller-effect dominates over external photodiode and stray capacitances. As an example, a relatively high source-capacitance of 4 pF would decrease the bandwidth by only about 30% . Consequently, the NE5212 will be relatively insensitive to PIN photodiode source capacitance variations. Since the dominant pole of the amplifier is at the input node, PIN diode source capacitance will not degrade phase margin.

Package parasitics

Package parasitics, particularly ground-lead inductances and parasitic

capacitances, can significantly degrade frequency response. To minimize parasitics, the NE5212 is offered in a 14-pin as well as an 8-pin package. The 14-pin version uses multiple grounds to minimize ground wire-bond inductances and leaves pins adjacent to the input unconnected. This will minimize parasitic capacitance and feedback from the outputs. Since the 8-pin version cannot afford all these techniques, its frequency response is inevitably compromised.

While the surface mount SO-14 version has a typical bandwidth of 150 MHz, the SO-8 version achieves 125 MHz. The difference in bandwidth can be utilized advantageously by choosing the appropriate package type and bandwidth as dictated by a particular system requirement.

Further bandwidth modifications can be achieved by a small capacitance between input and output or input and ground. Since the NE5212 has differential outputs, both peaking and attenuating type frequency response shaping are possible.

Fighting noise

Since most currently installed and planned fiber optic systems use non-coherent transmission and detect incident optical power, receiver noise performance becomes important. The SE/NE5212 goes a long way towards solving this problem. Its input stage configuration achieves a respectably low input referred noise current spectral density of 3 $pA/\sqrt{Hz}$, measured at 10 MHz. This low value is nearly flat over the entire bandwidth. The trans-resistance configuration assures that the external high value bias resistors, often required for photodiode biasing, will not contribute to total system noise. As shown in the following equation [1], the equivalent input RMS noise current is determined by the quiescent operating point of Q_1, the feedback resistor, R_F, and the bandwidth, Δf, however, it is not dependent on the internal Miller-capacitance. The noise current equation is then

$$\overline{i_{eq}^2} = 4kT\frac{\Delta f}{R_F} + 2qI_{BQ1}\Delta f + 2qI_{CQ1}\frac{1}{\beta_{dc}} + \omega^2(C_s + C_{\pi 1})^2\Delta f + 4kT\, r_{bQ1}\,\omega^2 C_s^2\Delta f$$

Using design values of I_{CQ1}=0.5 mA, R_F=7.4kOhms, β=50 and Δf=100 MHz, the frequency independent term yields 25 nA_{RMS} noise. Design values for the frequency-dependent term are: C_s=1.3 pF, $C_{\pi 1}$=0.7pF and r_{bQ1}=170 Ohms. The measured integrated noise was 33 nA.

Testing the NE5212

Connecting the NE5212 in an actual fiber optic pre-amplifier configuration, dynamic range, transient response, noise and overload recovery tests are easily measured (Figure 4) . In order to replicate actual parasitic capacitances, effects of the photodiode bias network and circuit layout effects, the test circuit should closely resemble the real application conditions. If the intention is to use the device in die form, then the actual hybrid circuit mounting techniques should be used while testing.

In the test circuit shown, an 850 nm modulated laser light source feeds an HP-HFBR2202 PIN photodiode which is mounted in close proximity to the NE5212 input. The R-C filter in series with the photodiode eliminates

possible disturbances from the power supply. Both differential outputs are AC coupled through 33 Ohm resistors in order to match to the 50 Ohm test system. In most applications these matching resistors are unnecessary. Performance evaluation in the linear region, including amplitude and phase response and power supply rejection can be accomplished by a network analyzer and S parameter test set (Figure 5). The simple equations given in the figure for the calculation of trans-resistance, R_T , are accurate for $R>>R_{in}$, where R_{in} is the input resistance of the NE5212.

General purpose RF applications.

Besides the main fiber-optic receiver applications, many other interesting possibilities exist for the the NE5212. Simplicity and ease-of-use are the prevailing characteristics of this device. For instance, amplifiers with 20 dB gain can be built requiring only one external gain setting resistor (Figure 6). The voltage gain of the differential configuration with no load at the outputs can be calculated as follows:

$$v_{out} = i_{in} \times R_T = \frac{v_{in}}{R_s + R + R_{in}} R_T \quad \text{and} \quad A_v = \frac{v_{out}}{v_{in}} = \frac{R_T}{R_s + R + R_{in}}$$

where Rs is the signal-source resistance, R is the external gain setting resistor and R_{in} is the input resistance of the NE5212. Substituting the actual values:

$$A_v = \frac{14000}{R_s + R + 110}$$

where all values are in Ohms. The graph of Figure 6 is an experimental verification of this formula in a single-ended, 50 Ohm system, using the test configuration of Figure 5. Note the 6 dB loss due to the single-ended configuration and another 6dB due to the 50 Ohm load.

As in all other RF applications, attention to power supply bypassing, clean grounds, and minimization of input stray capacitances is required for optimum performance.

Another useful application of the NE212 is as a voltage controlled amplifier, using a DMOS FET device biased into the linear region (Figure 7). An operational amplifier with supply-to-ground output swing and supply-to-ground input common mode range (such as the Signetics NE5230) can provide adequate gate control voltage even with a single 5V power supply. This type of circuit can have 25dB AGC range at 50 MHz and 45dB at 10MHz with less than 1% harmonic content. AGC range is determined by the ON-resistance range of the FET and capacitive drain to source feedthrough. If lowest RF feedthrough were required, the FET should be used in a shunt configuration rather than in a series.

Turning towards an entirely different area of application, where contrary to the NE5212s' capabilities, poor phase margins are mandatory, a simple crystal oscillator with buffered output can be built using a minimum number of external components (Figure 8). The feedback signal is taken from the non-inverting output, while the inverting output provides a low impedance (15 Ohm) output drive. The crystal operates in its series resonance mode. Figure 9 shows a varactor tuned version with a large tuning range. In Figure 10 the circuit has been optimized for stability at the expense of tuning range.

In RF amplifier applications it is often desirable to limit the amplifier bandwidth in order to minimize noise and RFI. The 100-150 MHz bandwidth of the NE5212 can be easily modified by connecting a capacitor to the input pin. The device bandwidth then becomes

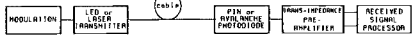
$$f_{-3dB} = \frac{1}{2\pi R_{in} (C_{in}+C_{EXT})}$$

where R_{in} is the input resistance, C_{in} is the input capacitance as specified in the data sheet and C_{EXT} is the external capacitance. For example, a C_{EXT}=33 pF will reduce the amplifier bandwidth to 42 MHz with a single pole roll-off. The transfer curve is shown in Figure 11. Single-ended to differential conversion is another useful application for the device. Impedance matching is easily accomplished by resistors connected in series with the outputs.

The NE5212 was designed using an advanced oxide-isolated bipolar process. This technology advantageously combines the required characteristics of low noise, large bandwidth, and relatively low cost, due to its high density. The under $2.00 quantity-price of the device, coupled with the capability of up to 300 MBaud data rates will lead to further cost-reduction of fiber-optic receivers. Due to its versatility, many non-fiber optic applications are also possible.

Reference:

[1] Robert. G. Meyer, Robert. A. Blauschild: "A Wide-Band Low-Noise Monolithic Transimpedance Amplifier," IEEE Journal of Solid-State Circuits, Vol. SC-21 No 4, pp 530-533, Aug. 1986.



Fiber optic transmission system, using trans-resistance pre-amplifier.

Figure 1

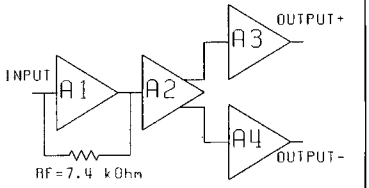
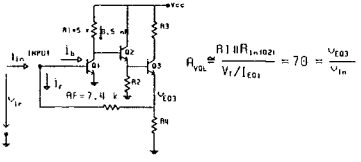


Figure 2.

NE5212 block diagram showing the trans-resistance pre-amplifier with the internal feedback resistor and the buffered differential outputs.



$$A_{VOL} \cong \frac{A1 \| R_{in1021}}{V_f / I_{E01}} = 70 = \frac{V_{E03}}{V_{in}}$$

This simple shunt-series input stage has some hidden features besides its very low noise. Due to the Miller-effect, the collector- base capacitance of Q1, multiplied by a voltage gain of 70, forms the dominant pole with RF, while desensitizing frequency response to source capacitance variations.

Figure 3.

HP3577A NETWORK ANALYZER	SINGLE ENDED	DIFFERENTIAL
HP3577AB S-PARAMETER TEST SET	$A1 = \frac{V_{out}}{V_{in}} A = 521 \cdot A$	$A1 = \frac{V_{out}}{V_{in}} A = 2 \cdot 521 \cdot A$
PORT 1 PORT 2	$Ro = Zo \left\| \frac{1+.522}{1-.522} \right\| = 93$	$Ro = 2Zo \left\| \frac{1+.522}{1-.522} \right\| = 66$

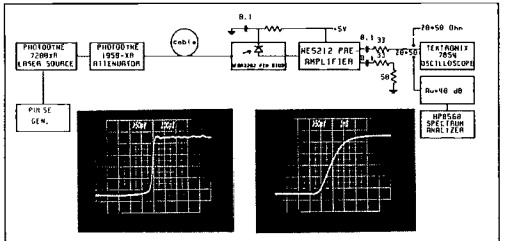
Z0=50 Z0=50

0.1uF 33 0.1uF OUT IN OUT 33 0.1uF

51 50

The frequency response can be conveniently measured with an S-parameter network analyzer. The 1 kOhm input resistor acts as a voltage to current converter and the resistors at the output do the impedance matching. The curves show a smooth, wide band response with ample phase margin. Trans-resistance and output resistance can be calculated from the S-parameters as shown in the table.

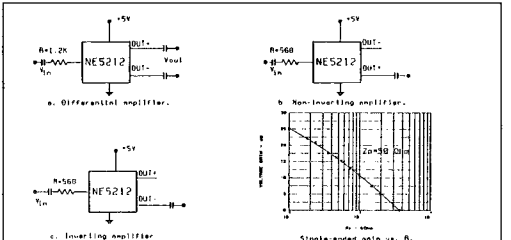
Figure 5.



a. Stimulus b. Response

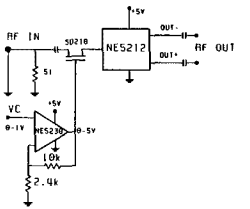
Figure 4.

Dynamic range, impulse response and noise test circuit.



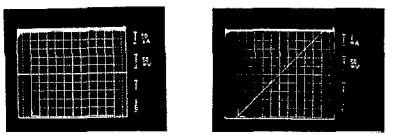
A 150 MHz, 20 dB amplifier requires only one external gain setting resistor. Differential or single ended operation with or without inversion is possible.

Figure 6.



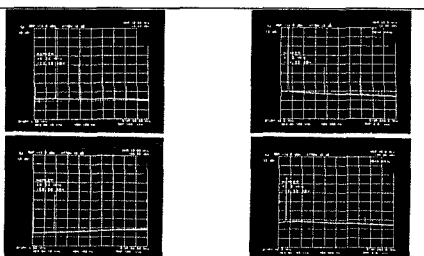
This variable gain RF amplifier has less than 1% distortion, 25 dB range at 50 MHz and 45 dB range at 10 MHz, with a 0-1 V control signal.

Figure 7



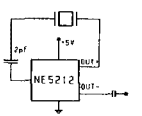
FET resistance in its linear region at Vgs=0V (left) and at Vgs=5V (right).

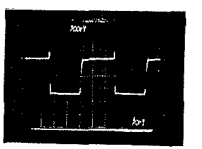
Figure 7b



Performance data of the RF attenuator of Figure 7.

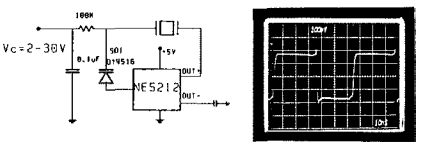
Figure 7a





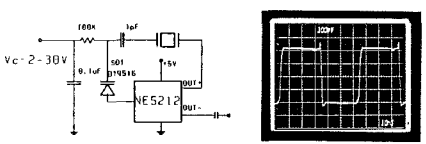
This 16 MHz crystal oscillator has minimum component count and operates in the series resonant mode. Output provides independent 50 Ohm drive capability.

Figure 8



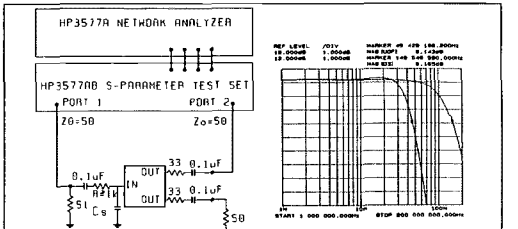
Varactor tuned crystal oscillator with 0.28% tuning range

Figure 9.



Varactor tuned oscillator with 1 ppm/V supply sensitivity.

Figure 10.



Setting bandwidth with shunt input capacitor, Cs.

Figure 11.

A Thermally Tuned VCO

Albert Helfrick

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Electronic tuning of an oscillator is almost universally accomplished with a varactor diode. There are, however, some applications where the use of the varactor poses some problems. One such example is a high power oscillator where the high voltage present in the oscillator tuned circuit causes either conduction of the diodes or diode breakdown. Likewise, a pulsed oscillator using a varactor diode can cause a transient frequency shift at turn-on. A high power or pulsed oscillator frequency can be controlled using heated ceramic capacitors without the problems of a varactor diode.

Figure 1 shows an oscillator using a pair of temperature-compensating ceramic capacitors heated with a resistor for frequency control. Although the example circuit operates at a relatively low power level, the technique can be adapted to oscillators of practically any power level. For the demonstration circuit, two common N750 ceramic disc capacitors were used. The dipped insulation was removed from the capacitors using a file and a ceramic-based resistor was sandwiched between the two capacitors. Thermal heat sink compound was used to insure good thermal contact between the resistor and capacitors. The ceramic resistor was used because of the relatively high power dissipation of this resistor for its small size. A good source of flat ceramic resistors is the DIP or SIP resistance pack where all of the resistors can be placed in parallel.

Figure 2 shows the frequency-voltage and the frequency-time characteristics of the test oscillator. As suspected, the oscillator shows a significant time delay between the applied control voltage and the frequency change. This limits the applications for such an oscillator and precludes any applications requiring rapid frequency correction. An oscillator of this sort would be suited for the control of industrial heating equipment, where frequency control is necessary because of FCC requirements, but tolerances are loose. Another application is for radar transponders where a high power oscillator is pulsed but the frequency control is loose (0.3%).

One of the significant disadvantages of the demonstration thermally-tuned oscillator is the use of a capacitor with a high temperature coefficient. Unless the temperature coefficient exactly compensates for the temperature variation of the oscillator inductor, the oscillator will be unstable with ambient temperature. Of course, the oscillator is to be used in an electronically stabilized system and the temperature instabilities will be corrected. However, the inherent instabilities subtract from the possible tuning range of the system. To achieve nominal operating frequency the capacitor must be adjusted to a temperature equal to or higher than the highest desired ambient temperature. This is not an impossible situlation, as it is often done in crystal ovens and temperature stabilized voltage references.

As an example, if the capacitor were operated at a nominal temperature of 85 C for a maximum ambient of 70 C, the maximum temperature variation would be 15 degrees negative and as much positive variation as the components would allow. For maximum frequency variation, the nominal operating temperature of the controlled capacitor would be midway between the maximum temperature that the heated capacitor would allow and the highest ambient temperature expected. The significant disadvantage of this is that there would be a "warm up" period in order to bring the temperature of the heated capacitor to the operating point. In the case of the demonstration oscillator, standard off-the-shelf components were used which were relatively large and had a significant thermal inertia. Small geometry ceramic capacitors with integral heating elements could be fabricated to reduce the thermal inertia and improve the thermal coupling to reduce this problem to an acceptable level.

A solution to the warm-up problem is shown in Figure 3. In this example the oscillator tuned circuit is resonated with two capacitors. The capacitors have identical values and equal but opposite temperature coefficients. Therefore, the combination of the two temperature coefficients would theoretically be equal to zero.

In this example, each capacitor would be individually heated, allowing the oscillator frequency to be increased by heating the negative coefficient capacitor or lowered by heating the positive coefficient capacitor.

Two advantages are available from this arrangement. First, the oscillator will be more ambient-stable as previously explained. Secondly, the tuning range of the oscillator would be twice that obtained with a single capacitor, as each capacitor could be heated from the ambient to the maximum temperature the capacitor would allow. In addition, the capacitors do not need to be preheated to a temperature above the ambient and thus there would be a saving of power. Since one capacitor would provide an upward variation of frequency while the second capacitor would provide a similar downward frequency variation, the total variation is twice what a single capacitor would supply.

From a practical standpoint, positive temperature capacitors are rare. A quick check of major capacitor manufacturer's literature indicated that only P100 temperature coefficient capacitors were available. In addition, there was no standard corresponding negative coefficient, the closest being N080 or N150. A parallel combination of equal P100 and N150, for example, will produce an equivalent temperature coefficient of N50. Since most inductors require a negative temperature coefficient capacitor for temperature stabilization, this was not considered as a significant deterrent.

The significant problem was the fact that the largest positive temperature coefficient of off-the-shelf capacitors was only 100 PPM/C. For many applications, much larger coefficients would be desired. One manufacturer of ceramic capacitors was contacted to determine the range of positive temperature coeffi-

cient capacitors available. It was learned that positive temperature coefficient capacitors were available to P600 and higher. These were not generally off-the-shelf capacitors, but are practical capacitors.

One practical application of the thermally-tuned oscillator is to stabilize a power oscillator for use in the ISM (industrial, scientific and medical) band. This frequency band is set aside by the FCC for RF heating, burglar alarms, and motion and position sensing. The nominal frequency of the ISM band is 915 MHz and the tolerance is +/- 13 MHz, which is primarily to accomodate free-running oscillators. The tolerance of +/- 1.4% is achievable with a careful design of a low power oscillator. There are good reasons to include additional frequency stability into the design of an ISM oscillator. Achieving the desired stability would be more difficult for higher power oscillators. In addition it may be desirable to purposely offset the frequency of an ISM oscillator so that more than one system could coexist at a single location. This offsetting would ebb the permissable tolerance and require a more stable oscillator.

Figure 4 shows a block diagram of a stabilized 915 MHz oscillator using an inexpensive color burst crystal and an inexpensive ECL divider. In this example, an old-design phase/frequency detector with separate pump-up and pump-down outputs is used. There are several LSI frequency synthesizer chips available with the separate outputs. To use a conventional single-ended output phase detector, a window comparator would be required to provide the separate up and down control outputs.

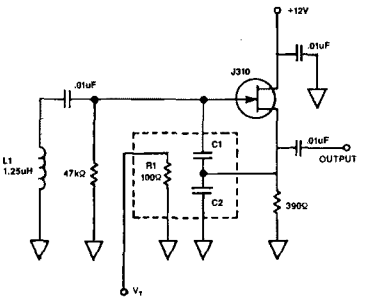
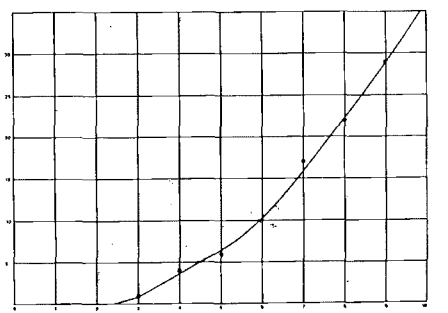


Figure 1. 30 MHz Test oscillator circuit diagram.



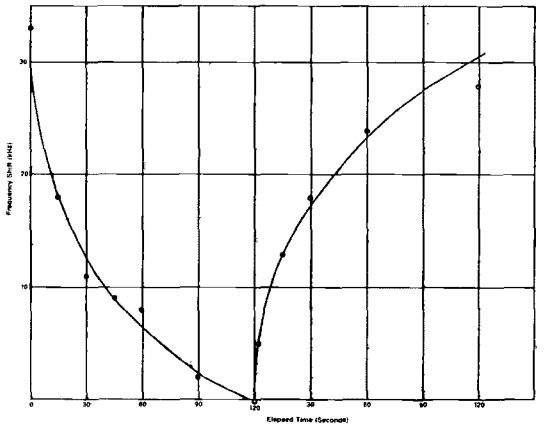


Figure 2(b). Time-Frequency Dependence

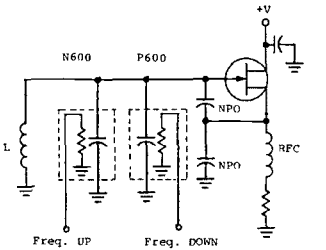


Figure 3. Oscillator configuration with positive and negative temperature coefficient capacitors.

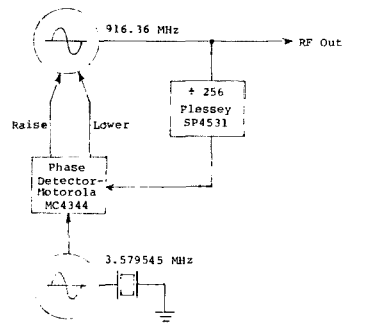


Figure 4. Stabilized oscillator application.

Computer-Aided Design of a Bipolar Transistor Amplifier

by

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Introduction

To be competitive in the RF and microwave hardware industry, companies must develop sophisticated components and systems at competitive prices -- with delivery schedules that tax the most experienced engineers. In response to growing market requirements many companies are turning to computer-aided engineering (CAE) and design (CAD) software to reduce design time and manufacturing costs.

Different design techniques and problems must be understood in order to be efficient with computer-aided design. The purpose of this paper is to present many of the necessary design techniques typically used in developing a new component. The design of a medium power bipolar transistor amplifier serves as an example of how to use these new computer-aided tools in designing modern hardware.

Design Outline

The complete procedure used for this example will be as follows:

1) Device Modeling

2) Device Characterization

3) Synthesizing A Matching Network

4) Small Signal Simulation

5) Large Signal Simulation

6) Fine Tuning the Design

7) Generating the Layout

8) Results

9) Conclusions

Device Modeling

The first part of any active design begins with the DC characterization of the active device. For this example the device was a bipolar transistor, MRA0500-19L, manufactured by TRW. This device is a linear power transistor designed for Class "A" medium power linear amplifiers with a useable frequency range from 100 to 500 GHz. The transistor is a multi-cell device with internal matching and produces 19 watts @Vce=19 volts and Ic=3.5 amps when compressed 1 dB. The small signal gain is 8 dB minimum.

In order to predict device performance, a suitable model must be used in conjunction with a nonlinear simulator program (mwSPICE) that can provide power measurement and S-parameters [1]. The Gummel-Poon model [2] for an NPN was used for this example. Initially, the I-V and C-V characteristics [3] were measured to obtain the parameters for the BJT model.

Table I lists the key parameters in evaluating the device. The performance of the mwSPICE circuit file listed in Figure A-1, Appendix A, was used for simulation. The default values of other model parameters (not listed) were used during the analysis. Further details concerning

Table I. Key BJT Model Parameters.

Parameter	Description	Value	
IS	Transport Saturation Current	1.5E-3	Amp
BF	Maximum Foward Beta	85	
VAF	Forward Early Voltage	52	Volt
IKF	Beta Knee Current	80	Amp
ISE	Base Emitter Leakage Current	4E-5	Amp
NE	Base Emitter Leakage Coefficient	1.35	
VAR	Reverse Early Voltage	6	Volt
RB	Zero Bias Base Resistance	0.08	Ohms
RE	Emitter Resistance	0.115	Ohms
RC	Collector Resistance	0.35	Ohms
CJE	Base Emitter Capacitance	200p	Farad
VJE	Base Emitter Potential	0.20	Volt
MJE	Base Emitter Coefficient	3.5	
TF	Forward Transit Time	115p	Sec
XTF	TF Bias Coefficient	3.5	
VTF	TF Vbc Coefficient	3.0	Volt
ITF	TF High Current Parameter	4.5	Amp
CJC	Base Collector Capacitance	115p	Farad
VJC	Base Collector Potential	0.22	Volt
MJC	Base Collector Coefficient	0.185	

device model characterization will soon appear in an article in RF Design Magazine. Table II provides a description of key features of the mwSPICE circuit file.

Table II. Circuit File Summary of Figure A-1.

Circuit Data/Block	Content
subcircuit "TRAN"	Describes all of the bond lead inductances and all internal parasitics associated with the packaged device.
subcircuit "NET"	Supplies the biases to "TRAN."
MODEL block	Describes the parameters used in the analysis.
SOURCE block	Provides a quiescent bias point. The AC input is used for the S-parameter measurement.
CONTROL block	Lists the frequencies over which the S-parameters will be measured with the stepped bias condition for I-V generation.
SPICEOUT block	Lists the desired data for output and the name of the S-parameter file where the data will be saved.

Device Characterization

Using the aforementioned circuit file, a simulation of the primary characteristics, I-V and S-parameters, was performed. In addition, to ensure that the mwSPICE model predicted the correct device performance, a comparison was made between the measured and mwSPICE-predicted I-V and S-parameter data over the design band of 170 to 230 MHz.

Figure 1 shows the comparison of the measured and simulated I-V characteristics while Table III provides the S-parameter comparison of the packaged device. As seen in Figure 1 and Table III, the theoretical and measured data agree quite well.

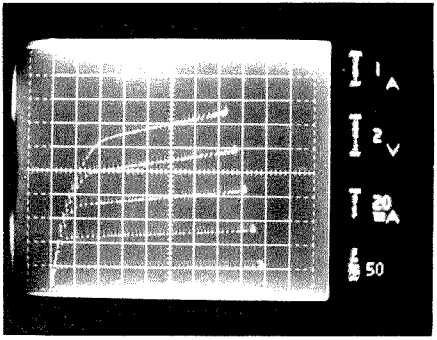

Figure 1(a). Measured I-V curves.

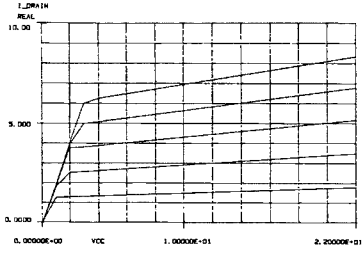

Figure 1(b). mwSPICE-produced I-V curves.

Table III. Comparison of Measured and Theoretical S-Parameters.

Measured S-Parameters

```
! MEASURED BY A NETWORK ANALYZER
! VDS=19V, IDS=3.5A
# GHZ S MA R 50
```

! FREQ	M(S11)	A(S11)	M(S21)	A(S21)	M(S12)	A(S12)	M(S22)	A(S22)
170.000	0.992	175.197	0.699	69.035	0.013	48.455	0.814	174.903
180.000	0.992	174.885	0.676	65.900	0.013	47.980	0.813	175.069
190.000	0.992	174.573	0.653	62.764	0.013	47.504	0.813	175.235
200.000	0.992	174.261	0.630	59.628	0.014	47.028	0.813	175.401
210.000	0.991	173.978	0.614	57.017	0.014	46.477	0.814	175.401
220.000	0.990	173.696	0.598	54.405	0.014	45.925	0.816	175.401
230.000	0.989	173.413	0.583	51.794	0.014	45.374	0.817	175.401

mwSPICE-produced S-Parameters

```
!  GENERATED BY mwSPICE
!  TEMPERATURE =   27.000 DEG C      8/26/86        20:24:8
#  S  GHZ  MA  R   50.0
```

! FREQ	M(S11)	A(S11)	M(S21)	A(S21)	M(S12)	A(S12)	M(S22)	A(S22)
170.000	0.986	175.620	0.700	69.790	9.6E-03	47.600	0.818	176.150
180.000	0.986	175.340	0.675	68.380	0.010	48.300	0.816	175.830
190.000	0.985	175.050	0.653	66.950	0.011	48.850	0.813	175.520
200.000	0.984	174.750	0.635	65.490	0.012	49.260	0.811	175.190
210.000	0.984	174.450	0.620	63.990	0.012	49.560	0.808	174.870
220.000	0.983	174.140	0.608	62.460	0.013	49.690	0.805	174.530
230.000	0.982	173.830	0.598	60.890	0.014	49.710	0.801	174.190

Synthesizing A Matching Network

With the DC/AC characterization verified, we were then ready to synthesize, in E-Syn [4], an input and output matching network based on the S-parameter file that was generated from the mwSPICE model. For a power design, the output was matched for maximum output power while the input was designed for the best match.

The input matching network utilized Chebyshev bandpass networks. Several circuits were provided during synthesis which satisfied the matching requirements. However, the Figure A-2 circuit was selected because it provided a DC block for the base of the BJT.

The results of a power contour analysis revealed that S22 was the best match for maximum power; this occurred due to internal matching by the manufacturer. For this example, the nominal output impedance of the device was used as the load to be matched in E-Syn. The output circuit was then synthesized using a Chebyshev transformer (Figure A-3) and matched to an output impedance of 5.2 Ohms.

Small Signal Simulation

The two networks synthesized in E-Syn were incorporated into the original circuit file (Figure A-1) to create the Figure A-4 circuit file. Figure A-4 is a Touchstone/mwSPICE circuit file modified to include S-parameters of the device (S2PA) and allow for immediate cross-checking of return loss and gain in both the linear (Touchstone) and nonlinear (mwSPICE) simulators.

The Touchstone simulation of the complete circuit (Figure 2) shows that the amplifier has a maximum input and output return loss of -7.6 dB and the gain varies from 14.5 dB at the low end of the band to 12.8 dB at the high end. A tabular listing of the Figure 2 circuit file, Table IV indicates that the circuit is unconditionally steble for this simulation.

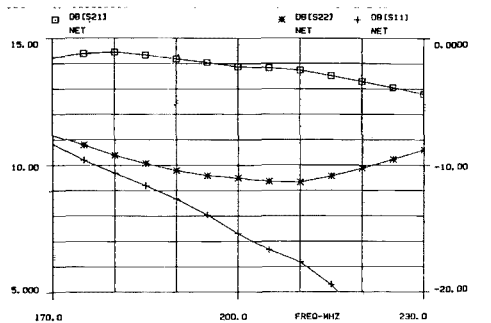

Figure 2. Small signal response in Touchstone.

Table IV. Small Signal Results.

FREQ-MHZ	DB[S21] NET	DB[S11] NET	DB[S22] NET	K NET
170.000	14.224	-8.331	-7.660	1.158
175.000	14 389	-9.598	-8.405	1.158
180.000	14.455	-10.619	-9.227	1.159
185.000	14 337	-11.594	-9.867	1.163
190.000	14 186	-12.648	-10.421	1.168
195.000	14 042	-13.890	-10.816	1.170
200.000	13.871	-15.367	-11.015	1.172
205.000	13.820	-16.647	-11.288	1.182
210.000	13.735	-17.609	-11.348	1.191
215.000	13.517	-19.407	-10.864	1.191
220.000	13.285	-21.900	-10.259	1.191
225 000	13.050	-26.221	-9.548	1.191
230.000	12.801	-37.245	-8.795	1.191

Large Signal Simulation

mwSPICE was then used in conjunction with the circuit file (Figure A-4) to to simulate the large signal performance of the complete circuit. An input power level of 1 watt (+30 dBm) was used during the simulation because the device was designed for a particular application. Figure 3 shows the simulated output power and gain vs. input power.

At the 1-watt drive level, the device response was in the linear region; therefore, both the linear and nonlinear simulators should have yielded the same results. This was verified by comparing the graphs of Figures 2 and 4.

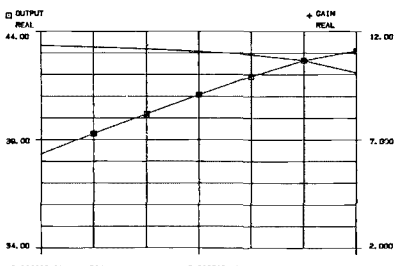

Figure 3. Output power and gain vs. input power response in mwSPICE.

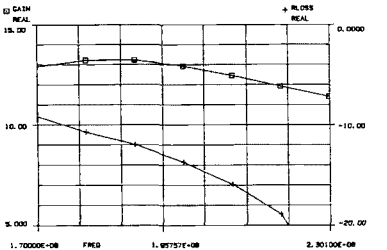

Figure 4. Return loss and gain vs. frequency response in mwSPICE.

The results of the mwSPICE Fourier analysis (Table V) then indicated that the second harmonic had the highest level at -31 dBc.

Table V. mwSPICE-Produced Fourier Analysis of Circuit.

DC COMPONENT = 1.345D+00 HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	2.300D+08	1.779D+01	1.000000	-29.160	.000
2	4.600D+08	5.108D-01	.028709	-119.318	-90.158
3	6.900D+08	1.229D-01	.006910	-55.691	-26.531
4	9.200D+08	5.701D-02	.003204	-12.316	16.844
5	1.150D+09	3.966D-02	.002229	1.091	30.251
6	1.380D+09	3.140D-02	.001765	2.539	31.700

Fine Tuning the Design

Next, the variables were tweeked using the tune mode in Touchstone to achieve a flatter gain response. In addition, parameters to generate the layout were added to the circuit file, which resulted in Figure A-5.

The modified circuit file design was cross-checked in mwSPICE. The results (Tables VI and VII and Figures 5 and 6) demonstrated close agreement between the programs. The mwSPICE gain response was 1 dB less than the Touchstone response due to bias circuitry contained in the SPICEOUT data block which was ignored by Touchstone but had a loading affect on mwSPICE performance.

Table VI. Touchstone Tabular Results of the Final Circuit Design.

FREQ-MHZ	DB[S21] NET	DB[S11] NET	DB[S22] NET	K NET
170.000	11.292	-6.835	-2.235	1.158
180.000	12.001	-12.127	-2.430	1.159
190.000	11.891	-16.194	-3.092	1.168
200.000	11.737	-19.846	-3.737	1.172
210.000	11.846	-21.765	-4.264	1.191
220.000	11.613	-20.603	-4.292	1.191
230.000	11.225	-14.417	-4.110	1.192

Table VII. mwSPICE Tabular Results of the Final Circuit Design.

FREQ MHZ	INPUT POWER (dBm)	OUTPUT POWER (dBm)	GAIN (dB)	RLOSS (dB)
170.00	30.00	40.08	10.089	- 7.60
180.00	30.00	40.88	10.88	-12.80
190.00	30.00	41.16	11.16	-17.51
200.00	30.00	41.08	11.08	-18.13
210.00	30.00	40.79	10 79	-20.27
220.00	30.00	40 41	10.41	-23.56
230.00	30.00	39.98	9.97	-16.48

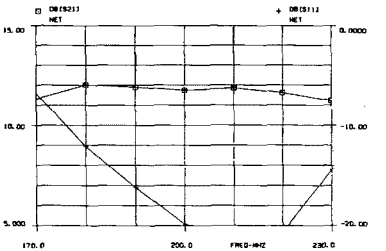

Figure 5. Final circuit file gain response in Touchstone.

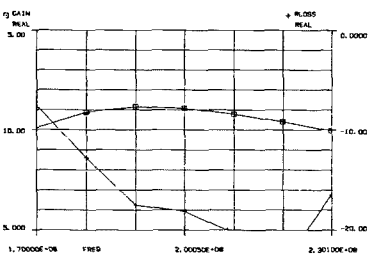

Figure 6. Final circuit file gain response in the mwSPICE.

Generating the Layout

A circuit layout was then generated by the CAD drawing program MiCAD [6] and transformed by the postprocessing program MlCmask [7] to drive a laser photoplotter -- thus creating the mask for manufacturing the circuit.

The layout modification does not interfere with the design analysis -- MiCAD only reads the necessary physical description while the simulators Touchstone and mwSPICE only read those portions of the circuit file required for a particular simulation.

To add microstrip lines for all lumped elements, in MiCAD we added PAD1 statements which set up transmission lines, their lengths, and the gap desired between them. The PARA statements simply identify parasitics which are to be ignored by MiCAD in the layout. Allowing a number of layouts and "mapping" of repeat components and parts to different drawings, MiCAD files were set up as follows:

Layer 0: Used the autoprocessed file input from Figure A-5 to create the 1:1 mask drawing file. Text, ground pads, and bias circuitry were added without using the *circuit file*.

Layer 1: Held the corner markers and alignment markers.

Layer 2: Held the substrate etched drawing with dimensions and Layer 1 markers copied to it

Layer 3: Held the transistor outline which was copied into the necessary locations on Layer 0 as needed.

Layer 4: Provided the assembly drawing.

The completed mask layout is shown in Figure 7 and the associated assembly drawing appears in Figure 8.

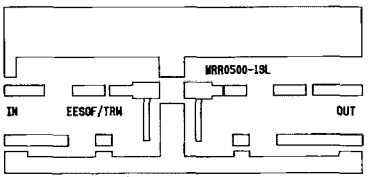

Figure 7. Amplifier mask layout generated by MiCAD.

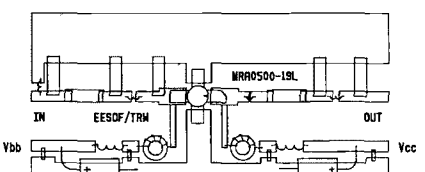

Figure 8. Amplifier assembly drawing generated by MiCAD.

The Results

The final design was then built and tested on a scalar network analyzer. The schematic for the final amplifier design is shown in Figure 9.

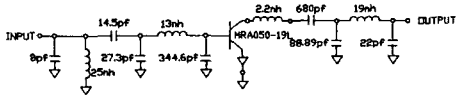

Figure 9. The final bipolar transistor amplifier design.

The measured results (Figure 10) confirm the accuracy of the circuit design illustrated in the mwSPICE response (Figure 11). Although the dip in the return loss for the measured response was at a lower frequency than predicted and the gain was slightly lower than predicted, the nature of both responses was the same.

The device used in the test amplifier was selected from a group of 10 devices used during the device modeling procedure. Since the parameters of the 10 devices were averaged and then used in the circuit file, any single device would not provide a measured response identical to the predicted response. However, if all 10 devices had been rotated in the test amplifier to generate a measured average response, the measured and predicted responses would have been identical.

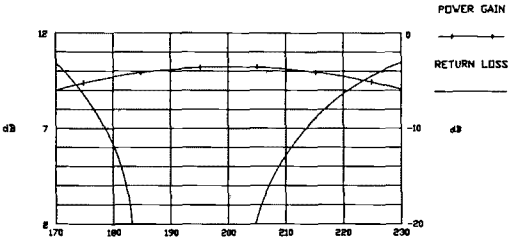

Figure 10. Measured gain response of the actual circuit.

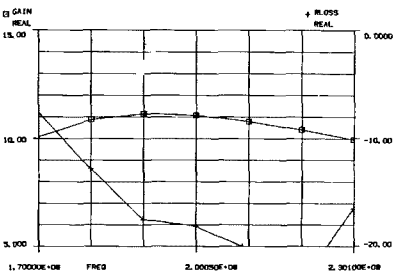

Figure 11. mwSPICE circuit file response.

Conclusions

The design techniques detailed in this paper are representative of typical CAE/CAD designs for achieving a working model. These techniques are especially important in anticipating circuit sensitivities to manufacturing tolerances. With computer technology rapidly improving engineering efficiency and accuracy, we will soon see computer-aided testing (CAT) available which will enable an engineer to take measured results from automatic network analyzers and *automatically* update the theoretical model.

The successful prediction of the actual performance of this RF amplifier demonstrates the accuracy of CAE/CAD products. The fact that engineers can now evaluate linear and nonlinear characteristics of circuits before they are manufactured dramatically saves both time and money.

APPENDIX A

CAD CIRCUIT FILES

```
! FILE :SP_SPAR
! GENERATE I-V curves and S-PARAMETERS FROM MWSPICE MODEL

DIM
  FREQ MHZ
  CAP  PF
  IND  NH
CKT
  MSUB ER=2.55 H=28.5 T=1.35 RHO=1 RGH=0.02
  MLIN_T1      1   2          W=300 L=500
  IND_LBIN     2   3          L=0.25
  CAP_CMATCH   3   0          C=345
  IND_LB       3   4          L=0.20
  S2PA_Q1      4   5   6      [MODEL=QNPN AREA=1.0]
  IND_LE       6   0          L=0.18
  IND_LC       5   7          L=0.05
  MLIN_T2      7   8          W=300 L=500
     DEF2P     1   8          TRAN
  TRAN_X1      1   2
     DEF2F     1   2          NET
MODEL
  QNPN  NPN      IS =1.5E-3 BF=85    VAF=52 IKF=80
              +  ISE=4E-5   NE=1.35  VAR=6
              +  RE =0.115  RC=0.35
              +  RB=0.08
              +  CJE=200pf VJE=0.20 MJE=3.5
              +  TF =115PS XTF=3.5  VTF=3.0   ITF=4.5
              +  CJC=115Pf VJC=0.22 MJC=0.185
SOURCE
        NET     ICS_IBB   0  1       DC=0.042
        NET     IVS_VCC   2  0       DC=19.0
CONTROL
        NET     DC IVS_VCC 0 22 1.0 ICS_IBB .020 .100 .020
        NET     AC LIN  7 170MEG 230MEG
        NET     OPTIONS ACCT LIST NODE LIMPTS=5e3
SPICEOUT
        NET     DC ALL
        NET     SP TRAN_X1   B:EESOF.S2P 50
```

Figure A-1. I-V and S-parameter circuit file.

```
! ------------------------ E-SYN  07/21/86 ------------------------
!
!                    LUMPED CHEBYSHEV BANDPASS NETWORK
!                   FREQUENCY : 170.0000 to 230.0000 MHz
!    INPUT FILE   : EESOF.S2P
!    OUTPUT TERM : R = 50.00000 Ohms
!                              3 RESONATORS
!    0.010000 dB RIPPLE          0.542478 dB MIL          0.000000 dB SLOPE
!
! ------------------------------------------------------------------

                              R = 50.00000  Ohms
          PLC     1    0  L = 31.73057   nH  C = 10.57711 pF
          CAP     1    2  C = 15.38323   pF
          CAP     2    0  C = 27.30423   pF
          IND     2    3  L = 15.17621   nH
          CAP     3    0  C = 344.6401   pF
                          S = EESOF.S2P
------------------------------------------------------------------
```

Figure A-2. Synthesized input circuit created in E-Syn.

```
! ------------------------ E-SYN  08/26/86 ------------------------
!
!                    LUMPED CHEBYSHEV TRANSFORMER NETWORK
!                   FREQUENCY : 170.0000 to 230.0000 MHz
!    INPUT TERM  : R = 5.200000 Ohms
!    OUTPUT TERM : R = 50.00000 Ohms
!                              ORDER = 2
! ------------------------------------------------------------------

                              R = 5.200000  Ohms
          IND     1    2  L = 6.742091   nH
          CAP     2    0  C = 88.88526   pF
          IND     2    3  L = 23.11017   nH
          CAP     3    0  C = 25.93112   pF
                          R = 50.00000  Ohms
------------------------------------------------------------------
```

Figure A-3. Synthesized output circuit created in E-Syn.

```
! FILE:SP_CKT
! COMPLETE MODEL OF DEVICE AND COMPLETE CIRCUIT

DIM
  ! standard units of measure
CKT
  MSUB ER=2.55 H=28.5 T=1.35 RHO=1 RGH=.02
  MLIN_T1      1   2          W=300 L=500
  IND_LBIN     2   3          L=0.25
  CAP_CMATCH   3   0          C=345
  IND_LB       3   4          L=0.20
  S2PA_Q1      4   5   6      [MODEL=QNPN AREA=1.0]
  IND_LE       6   0          L=0.18
  IND_LC       5   7          L=0.05
  MLIN_T2      7   8          W=300 L=500
     DEF2P     1   8          TRAN

  CAP_CM1      1   0          C=10.58
  IND_LM1      1   0          L=31.73
  CAP_CM2      1   2          C=15.38
  CAP_CM3      2   0          C=27.30
  IND_LM2      2   3          L=15.18
  CAP_CM4      3   0          C=344.6
  TRAN_X1      3   4
! S2PA         3   4   0      B:EESOF.S2P
  IND_LM3      4   5          L=6.74
  CAP_CM5      5   6          C=680
  CAP_CM6      6   0          C=88.89
  RES_RM7      6   0          R=1E6
  IND_LM4      6   7          L=23.11
  CAP_CM7      7   0          C=25.93
  RES_RMB      7   0          R=1E6
     DEF2P     1   7          NET

MODEL
  QNPN  NPN     IS =1.5E-3 BF=85    VAF=52 IKF=80
              + ISE=4E-5   NE=1.35  VAR=6
              + RE =0.115  RC=0.35
              + RB =0.08
              + CJE=200pf  VJE=0.2  MJE=3.5
              + TF =115PS  XTF=3.5  VTF=3.0 ITF=4.5
              + CJC=115pf  VJC=0.22 MJC=0.185
```

Figure A-4. E-syn input and output networks combined and modified in Touchstone (page 1 of 2)

```
SOURCE
       NET     1CS_1BB   0 20        DC=.042
       NET     CAP_CB1   20  0       C=35E6
       NET     CAP_CB2   20  0       C=1E3
       NET     1ND_LB1   20 21       L=500
       NET     CAP_CB3   21  0       C=470
       NET     1ND_LB2   21  3       L=100

       NET     1VS_VCC   30  0       DC=19.0
       NET     CAP_CC1   30  0       C=35E6
       NET     CAP_CC2   30  0       C=1E3
       NET     1ND_LC1   30 31       L=500
       NET     CAP_CC3   31  0       C=470
       NET     1ND_LC2   31  4       L=100

       NET     1VS_V1N   40  0   AC=1.0 PWR=(30 30 0 1.7E8 2.3E8 .1e8)
       NET     RES_R1N   40  1       R=50
       NET     RES_ROUT  7   0       R=50
CONTROL
       NET     TRAN 40PS 25NS  0  40PS
       NET     PWR 1VS_V1N RES_R1N
       NET     AC L1N 13 170MEG 230MEG
       NET     DC 1VS_VCC 0 22 1.0 1CS_1BB .020 .100 .020
!      NET     FOUR 200MEG V(7)
       NET     OPTIONS ACCT LIST NODE LIMPTS=5e3
!      NET     TEMP 27.0
SPICEOUT
       NET     PWR RES_R1N 1 0 RES_ROUT 7 0
       NET     DC ALL
       NET     AC ALL
!      NET     SP TRAN_X1 B:EESOF.S2P 50
OUT
   NET DB[S21] GR1
   NET DB[S11] GR1A
   NET DB[S22] GR1A
   NET K
FREQ
  SWEEP 170 230 5
GR1D
  RANGE 170 230 10
  GR1 5 15 1
  GR1A -20 -0
```

Figure A-4. E-Syn input and output networks combined and modified in Touchstone (page 2 of 2)

```
! FILE:SP2_CKT WITH COMPLETE CIRCUIT FILE DESIGN INCLUDING LAYOUT
VAR
  W50=189
DIM
! Standard units of measure
CKT
  MSUB ER=2.55 H=28.5 T=1.35 RHO=1 RGH=.02
! MLIN_T1     1   2           W=300 L=500
! IND_LB1N    2   3           L=0.25
! CAP_CMATCH  3   0           C=345
! IND_LB      3   4           L=0.20
! S2PA_Q1     4   5    6      [MODEL=QNPN AREA=1.0]
! IND_LE      6   0           L=0.18
! IND_LC      5   7           L=0.05
! MLIN_T2     7   8           W=300 L=500
!    DEF2P    1   8           TRAN
   MLIN       10   1          W^W50  L=524
   CAP_CM1    1   0           C=8              para
   IND_LM1    1   0           L=25             para
   CAP_CM2    1   2           C=14.5           PAD1 W^W50 S=200 L=900
   CAP_CM3    2   0           C=27.3           para
   IND_LM2    2   3           L=13             PAD1 W^W50 S=412 L=900
   CAP_CM4    3   0           C=344.6          para
   MLIN_T1    3   30          W=300 L=500
! TRAN_X1     3   4
   S2PA       30  40  0    B:EESOF.S2P        SPAC L=450
   MLIN_T2    40  4           W=300 L=500
   IND_LM3    4   5           L=2.2            PAD1 W^W50 S=200 L=426
   CAP_CM5    5   6           C=680            PAD1 W^W50 S=200 L=900
   CAP_CM6    6   0           C=88.89          para
   RES_RM7    6   0           R=1E6            para
   IND_LM4    6   7           L=19             PAD1 W^W50 S=390 L=900
   CAP_CM7    7   0           C=22             para
   RES_RM8    7   0           R=1E6            para
   MLIN       7   8           W^W50 L=500
    DEF2P     10  8           NET
MODEL
  QNPN  NPN      IS =1.5E-3 BF=85    VAF=52 IKF=80
              +  ISE=4E-5   NE=1.35  VAR=6
              +  RE =0.115  RC=0.35
              +  RB =0.08
              +  CJE=200pf  VJE=0.2  MJE=3.5
              +  TF =115PS  XTF=3.5  VTF=3.0 ITF=4.5
              +  CJC=115pf  VJC=0.22 MJC=0.185
```

Figure A-5. Final circuit file designed for layout generation (page 1 of 2)

```
SOURCE
       NET      ICS_IBB    0 20        DC=.042
       NET      CAP_CB1   20  0        C=35E6
       NET      CAP_CB2   20  0        C=1E3
       NET      IND_LB1   20 21        L=500
       NET      CAP_CB3   21  0        C=470
       NET      IND_LB2   21  3        L=100

       NET      IVS_VCC   30  0        DC=19.0
       NET      CAP_CC1   30  0        C=35E6
       NET      CAP_CC2   30  0        C=1E3
       NET      IND_LC1   30 31        L=500
       NET      CAP_CC3   31  0        C=470
       NET      IND_LC2   31  4        L=100

       NET      IVS_VIN   40  0   AC=1.0 PWR=(30 30 0 1.7E8 2.3E8 .1e8)
       NET      RES_RIN   40  1        R=50
       NET      RES_ROUT   7  0        R=50
CONTROL
       NET       TRAN 40PS 25NS  0  40PS
       NET       PWR IVS_VIN RES_RIN
       NET       AC LIN 13 170MEG 230MEG
!      NET       DC IVS_VCC 0 22 1.0 ICS_IBB .020 .100 .020
!      NET       FOUR 200MEG V(7)
       NET       OPTIONS ACCT LIST NODE LIMPTS=5e3
!      NET       TEMP 27.0
SPICEOUT
       NET       PWR RES_RIN 1 0 RES_ROUT 7 0
!      NET       DC ALL
!      NET       AC ALL
!      NET       SP TRAN_X1 B:EESOF.S2P 50
OUT
   NET DB[S21] GR1
   NET DB[S11] GR1A
   NET DB[S22]
   NET K
FREQ
  SWEEP 170 230 10
GR1D
  RANGE 170 230 10
  GR1 5 15 1
  GR1A -20 -0
```

Figure A-5. Final circuit file designed for layout generation (page 2 of 2)

APPENDIX B

BIBLIOGRAPHY

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[3] TECAP, Hewlett Packard, Copyright 1985.

[4] E-Syn program, EEsof, Inc., Copyright 1986.

[5] Touchstone program, EEsof, Inc., Copyright 1984.

[6] MiCAD program, EEsof, Inc., Copyright 1985.

[7] MICmask program, EEsof, Inc., Copyright 1985.

LOW-NOISE PREAMPLIFIER DESIGN FOR NMR

by

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1. INTRODUCTION

An important component in any nuclear magnetic resonance (NMR) imaging or spectroscopy system is a low-noise preamplifier. The required minimization of its noise figure can be obtained only by careful design. it must go hand in hand with an optimization of the "noise figure" of the NMR receive coil. The latter requires that the coil quality factor Q is made as high as possible. Other receiver system components such as cables, protection circuits, matching networks, transmit/receive (T/R) switches etc. should not be neglected in a low-noise design. They can easily add many tenths of a dB to the overall receiver noise figure.

2. QUALITATIVE LOW-NOISE DESIGN

The most critical item in a low-noise preamplifier is its input device. Bipolar transistors have the advantage to provide a relatively large bandwidth at higher frequencies (20-200 MHz). They must be selected for a high current gain, a large gain-bandwidth product FT of several Gigahertz and especially a low base-region bulk resistance. The latter can be reduced by paralleling two or more transistors. Due to their high input impedance junction field-effect transistors are suitable for low-noise narrow-band preamplifiers. They should exhibit a high transconductance which increases with the electron mobility in the channel. Since the latter is much higher in gallium-arsenide than in silicon GaAs-MESFET's are also good candidates for low noise NMR preamplifer designs.

As far as circuit design is concerned, the following rule should be obeyed: Eliminate all parasitic series or parallel impedances between base-emitter or gate-source terminals. This implies that, for example, by-passed emitter resistors must not be used and biasing resistors have to be chosen very high compared to the transistor input impedance.

3. QUANTITATIVE DESIGN

The expanded noise equivalent circuit of a preamplifier or its input transistor is shown in Figure 1. Ys=Gs+jBs is the source admittance producing the noise current Is. Y=G+jB is the input admittance of the noise-less (F=1) ideal amplifier of voltage gain A. The amplifier noise is in good first-order approximation represented by the input related equivalent noise voltage and current generators V and I. At higher frequencies they may be partially correlated, an effect which can be represented by the additional current generators (YC)V=(GC+jBC)V where YC is the so-called correlation admittance. Table 1 summarizes the important noise formulas. The noise figure F defined as the ratio of the total amplifier output noise power to the output noise due to the source resistor only is given by Equation 1. F is minimized by chosing an optimum source admittance Ys=Gs+jBs as given by Equation 3. The minimum noise figure obtainable is expressed in Equation 4. The following relationship

(Equation 5) shows that the noise figure has a parabolic dependence on the source susceptance Bs. The same is partially true for Gs. It is interesting to note that the formulas for F do not explicitly depend on the input admittance Y. Its effect is contained in the noise generators V and I. In many cases, especially at lower frequencies, the correlation admittance Yc is negligible. The optimum source conductance Gc(opt) is then given by the simple expression I/V.

4. OPTIMUM SOURCE ADMITTANCE

The analysis suggests a simple algorithm for determining the optimum source admittance Ys(opt) to minimize the noise figure F:

a. Determine the preamplifier input admittance Y=G+jB.
b. Measure the output RMS noise voltage VL(Gs=oo) for a shorted input and VL(Gs=0) for a open-circuited input.
c. Determine from Equation 6 a trial optimum source conductance Gs(opt).
d. Measure the noise figure with this source resistor as a function of parallel source susceptance Bs. The value of Bs which minimizes the noise figure is Bs(opt)=-Bc.
e. Repeat step b with Bs=-Bc and obtain the final value of Gs(opt) which will not be much different from the previously determined one.

It is interesting to note that Bs(opt) is independent of Gs and that in the above procedure it was not necessary to determine the correlation explicitly. Note that if there is no correlation (Yc=0) then the optimum source impedance is real and simply given by Rs=1/Gs=V/I.

In order to minimize the preamplifier and the NMR system noise figure it is now important that the receiver coil input impedance is matched by a transformation network to the optimum source admittance given by Equation 3 or 6 in Table 1. The question may arise: What should the input impedance Y of the preamplifier be? Since the formulas for the noise figure and the optimum source admittance Ys(opt) are independent of Y the answer is: It does nor matter as long as the source , in an NMR system the receiver coil, is matched to Ys(opt). Since the input impedance of NMR head or body receiver coils is dependent on the size of the patient to be imaged one can use a variable matching network in order to minimize the noise figure or one should use a preamplifier with a very low F.

5. MEASUREMENT TECHNIQUES

Since most NMR system operators have liquid nitrogen available in their facilities the so-called two-temperature method of noise figure measurement is very suitable. The preamplifier output noise voltage is measured with the source resistor Rs=1/Gs first at room temperature T1, (V1), and then dipped into liquid nitrogen (T2=77 degree Kelvin, V2). From the curve of Figure 2 (courtesy Dr. Howard Hart, GE-CRD) and the output noise voltage ratio V2/V1 the noise figure F is obtained. The advantage of this method is its low cost and its suitability for noise measurements in a complete NMR system. It also permits an easy determination of F as a function of source resistance without impedance transformation networks. Accurate measurements can be made with the fine HP-8970A noise figure meter (10-1500 MHz), but only in a 50 Ohm system. A comparison between the two methods resulted in good agreement For all NMR low-noise preamplifier measurements one should use only the HP346A and not the 346B noise source.

6. RESULTS: NOISE FIGURE MEASUREMENTS

In Figure 3 the measured noise figure is shown as a function of source resistance Rs=1/Gs for a preamplifier of a low-field NMR system (0.12 Tesla, 5.1 MHz). A cascode configuration of 2 junction field-effect transistors (U-310) is used in the input stage. The optimum source resistance is approximately 750 Ohm. Feedback damping has been employed in order to increase the bandwidth of the receiver coil without degrading the noise performance too much. It is interesting to note that Rs(opt) remains the same with and without feedback (RF=00) whereas the input impedance changes drastically from 1700 Ohm, -82 degrees to 250 Ohm, 22 degrees. This preamplifier was connected directly to an NMR receive coil tuned to Zin=750 Ohm. For RF=00 a noise figure of F=0.5 dB and for RF=20 kohm//1pF, F=0.7 dB was obtained. These measurements demonstrate also that the optimum source resistor is for junction field-effect transistors relatively high. Figure 4 shows F at 5.1 MHz as a function of the source admittance phase angle. For $\varnothing$=+-45 degree a capacitor or inductor having a reactance of of X=1000 Ohm was connected in parallel to a source conductance of 1mS. The minimum of the noise figure F occurs for $\varnothing$=0 indicating that the correlation admittance Yc is zero. This means that the input related noise voltage and current generators V and I in the equivalent circuit of Figure 1 are uncorrelated. The curve demonstrates that even relatively small deviations from the optimum source conductance by a capacitive or inductive component results in a noise figure degradation of several tenths of a dB. One concludes that for noise optimization it is necessary to control especially the phase angle of the source admittance Ys. In practical terms this means that a few undesired picofarads in parallel to a preamplifier input can degrade F. On the other hand Figure 3 demonstrates that deviations from Gs(opt) are not that critical because that curve has a relative broad minimum. Figure 5 shows the circuit diagram of this J-FET preamplifier.

At higher frequencies bipolar transistors can be used, especially if a large bandwidth is desired, for example for a preamplifier covering the imaging and the spectroscopy frequencies. (64, 59, 26, 16 MHz). Their optimum source resistor is much lower (Rs(opt)=40...100 Ohm). Figure 6 shows the frequency response of the noise figure for an amplifier using MA-42197 bipolar devices demonstrating that F-values of less than 1 dB can be achieved over a large frequency range. In Figure 7 the noise figure is plotted as a function of the source resistor and the source susceptance for 64 MHz.

Figure 8 demonstrates an example of a preamplifer for which the correlation admittance Yc is not zero. The minimum noise figure occurs for a source susceptance of Bs=-3mS. (Parallel inductance with a reactance of XL=330 Ohm). By not neglecting the correlation effect expressed by the correlation admittance Yc one obtains in this case a noise figure improvement of about 0.2 dB. This amplifier used a by-passed emitter resistor in the first stage which probably caused the noise correlation.

7. SUMMARY AND CONCLUSION

In order to obtain good NMR image quality low-noise preamplifiers are required. With careful design and by providing the optimum source impedance noise figures of 0.5 dB can be achieved. At higher frequencies the correlation between V and I in the noise equvalent circuit should not be neglected if the noise figure is to be minimized.

REFERENCES

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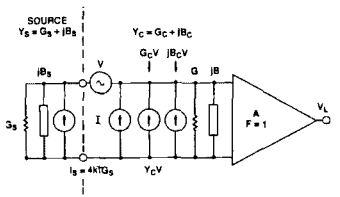
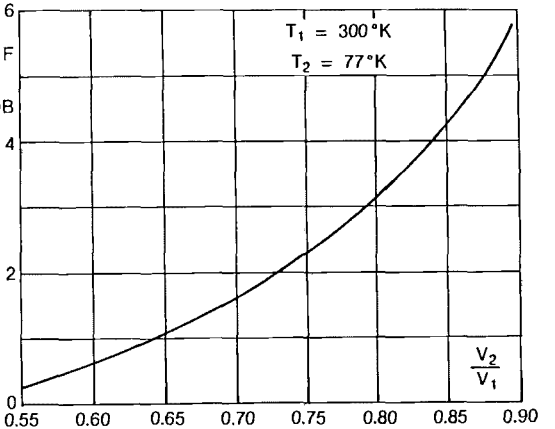
2. W.A. Edelstein, P.A. Bottomley and L.M. Pfeiffer: "A signal-to-noise calibration procedure for NMR imaging systems." Med. Phys. , 11, 180, (1984).



EQUIVALENT AMPLIFIER NOISE CIRCUIT INCLUDING CORRELATION BETWEEN VOLTAGE AND CURRENT NOISE SOURCES

FIGURE 1

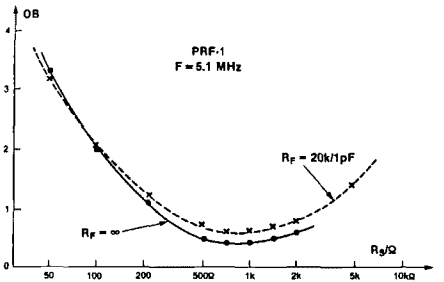


LIQUID NITROGEN METHOD: NOISE FIGURE AS A FUNCTION OF THE NOISE VOLTAGE RATIO V_2/V_1.

FIGURE 2

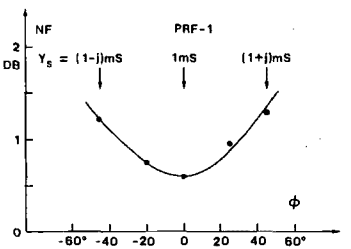
①	$F = 1 + \frac{V^2\lvert Y_S+Y_C\rvert^2 + I^2}{I_S^2} = \text{MINIMUM}$	
②	$\partial F/\partial B_S = 0$	$\partial F/\partial G_S = 0$
③	$B_S(OPT) = -B_C$	$G_S(OPT) = \sqrt{I^2 + G_C^2 V^2}/V$
④	$F_{MIN} = 1 + \frac{V^2}{2kT}(G_S(OPT) + G_C)$	
⑤	$F = F_{MIN} + \frac{V^2}{4kTG_S}\left[(G_S(OPT) - G_S)^2 + (B_S(OPT) - B_S)^2\right]$	
⑥	$Y_C = 0$: $G_S(OPT) = \lvert G + jB\rvert \cdot \frac{V_L(G_S=0)}{V_L(G_S=\infty)}$	

TABLE 1: NOISE FORMULAS



NOISE FIGURE VS SOURCE RESISTOR

FIGURE 3



NOISE FIGURE AS A FUNCTION OF THE SOURCE ADMITTANCE PHASE ANGLE

FIGURE 4

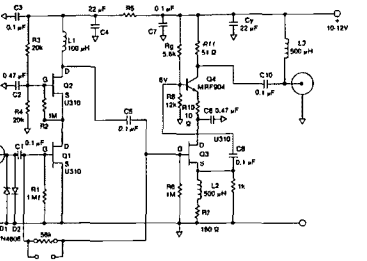
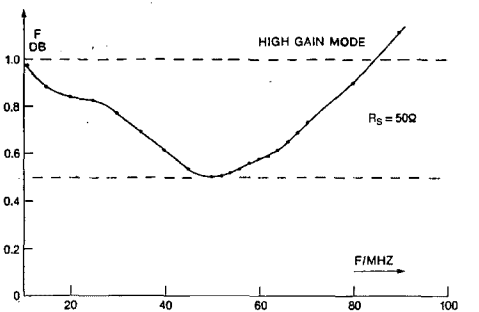


FIGURE 5



LNA-V-1: NOISE FIGURE F VS FREQUENCY

FIGURE 6

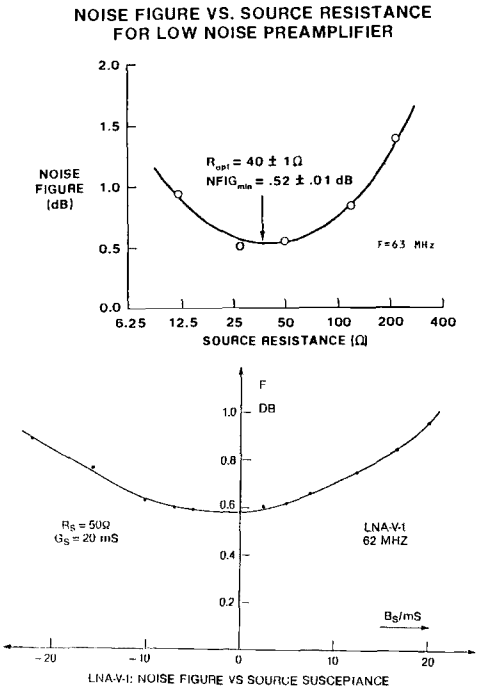


FIGURE 7

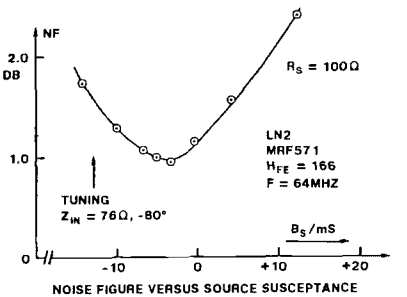


FIGURE 8

A Complex Impedance Meter

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The idea of this instrument was conceived through the better understanding of the Smith chart that I was able to receive in the late '70s. It took a few years, until around 1980, to get around to building one, verifying the concept. I remember that it was an antenna that defied tuning, and a 2-meter version of the instrument was built.

As is apparent in the Smith chart, all mismatches reflect power. At an open end of a transmission line a voltage maximum will occur. This corresponds to a point at the right edge of a Smith chart. At a shorted end there will be a voltage minimum (the left edge), and in the case of a perfect match, there will be equal voltage along the line (chart center). Correspondingly, loads with some imaginary part, inductors and capacitors combined with the load, will move vertically from the center, inductors up and capacitors down. They will not move on a straight line, like their resistive counterparts, but along some resistive circle, and the unity circle if the resistive part is a match. In the vicinity of the center, this vertical movement is approximately a straight line. How do we detect and indicate these deviations, then?

A wise man, Magnus Koch at the Chalmers U. of Technology, Göteborg, Sweden once told me, "If you can measure something with a bridge, do it!" As the years have gone by, I have found them to be words of wisdom, and they certainly apply here. A bridge, how to make a bridge that can detect in what direction something takes off on a Smith chart?

One does not have to! As you go along a transmission line away from, say a shorted end, you start at the leftmost end, and we all know that after $\lambda/8$, looking back, we will see an inductance with $j\omega L = Z_o$. After another $\lambda/8$, making $\lambda/4$ total, it looks like an open circuit, and so on. After one turn around the chart we have traveled $\lambda/2$ along the line. Let us now put four little detector diodes, monitoring the voltage on the line, spaced $\lambda/8$ apart, one in each "compass direction" around the chart. Well, you say, you can not do that! It introduces a mismatch! True, but all four diodes do the same. Since they are mutually cancelling, AT THAT FREQUENCY, plus a little line loss, it does not matter.

Let us excite the line and try various loads at the other end. The last diode is to be positioned where the loads will be applied, or an integer multiple of $\lambda/8$, in which case the indicators will change sign and label.

Referring to the basic schematic, Figure 1, let us look at a short circuit. D4 will obviously get no voltage at all to detect, but D2 will get twice the normal. D3 and D1 will not see any change. Due to the way D2 and D4 are turned, a negative voltage will appear at their summing point. An open circuit will produce the opposite, with a positive voltage from D4 and no voltage from D2. In both cases, D1 and D3 will detect equally strong

signals, but of opposite signs, so their sum is zero. In a similar way it works for imaginary deviations from the matched condition. Just imagine the chart rotated 90 degrees!

The beauty of the Smith chart, or at least one of them, is preserved in this apparatus. It is the fact that near perfect loads will be treated especially carefully and accurately. The concept is clearly not limited to 50 ohm lines. One can imagine the use of perhaps a 5 ohm line in a test fixture for measuring transistor input impedances.

A limitation is the bandwidth. I would say that the function is very satisfying within a 10% band centered around the design frequency. That is certainly more than enough for most "band" operations, be it ham radio, cellular mobile, radar, microwave link or CB. An exception from the bandwidth limitation is of course the well-matched load, which will appear as such, no matter what the frequency.

The maximum possible frequency of operation that can be achieved remains to be determined. The diodes have to be operating, of course, and can always be spread by multiples of $\lambda/8$ if physically necessary, but the bandwidth will suffer. Hewlett-Packard has been kind enough to supply me with some zero bias diodes good to 10 GHz, but in spite of a lot of care, they got damaged by static electricity. Using regular "hot carrier" diodes will work to at least 1 GHz, but a signal level of at least -15 dBm is necessary for good signals. A possible method of building the instrument for microwave frequencies is shown in Figure 2.

Practical Aspects

It may be more desirable to have the testplane outside the connector, as opposed to just behind it. This is possible by just adding some line after the last diode. This may actually be the preferred method, since all the diodes then will be mounted in an identical manner on the line, thereby balancing each other better. They will then have to be permutated, changing the order from 1-2-3-4 to 4-1-2-3.

It is also possible to measure remote (100λ) objects. By leaving the end of the line open, one can determine to what extent the chart is rotated, and either change the frequency slightly to get the open located on the right, or add some cable, or just remember the position. The insertion loss of the cable limits the sensitivity, of course, but I have derived useful information about a load with a 20 dB attenuator in line and +10 dBm excitation. This corresponds to a VSWR of 1.02:1 or 40 dB return loss. With the same level of excitation I can detect the difference between a "perfect" load and one of 70 dB reflection. To observe that mismatch on a Smith chart, you would have to use a microscope, since it corresponds to a distance from the center of half the thickness of a human hair.

Displaying the voltages on an X-Y oscilloscope (or a plotter for swept signals) is very convenient. It then becomes apparent that the outline of the displayed field, corresponding to the circular border of the Smith chart, is not really circular, but somewhat diamond shaped. Should this be disturbing, a 6 dB attenuator can be left on the measurement port. It is "transparent"

enough to make good measurements through. It also provides the necessary DC return path for the diode currents, that may not be present in the load or source.

The matching impedance of the source is not critical at all. A mismatch there reflects part of the power back to the source, but what travels down the line is what counts.

With zero bias diodes it should be possible to use a regular signal generator for the source, with levels of 1 mV (-47 dBm), and measure receiver inputs without driving them into non-linear regions.

Other Applications

Substituting the "perfect" load with a resonant circuit opens up a few interesting applications. The output from the jX detector becomes very sensitive to changes in frequency, being zero at resonance. This can be used to measure deviation, modulation, PLL step response and maybe even phase noise. The higher the Q of the attached resonant circuit, the more sensitivity. A VCO can be locked to a cavity or a stub, by feeding back the DC signal.

Another application could be a distance meter, connecting both outputs to an UP/DOWN counter, with an antenna for a load. The sine/cosine information in the reflected signal will run the counter up or down, and one count for every half wavelength will be gathered. This may be a good detector for doppler radar burglar alarms, eliminating false alarms from objects that are just swinging back and forth in the wind.

Conclusion

A detector has been described, that in sensitivity far exceeds the common VSWR meter, and furthermore provides information about the complex nature of the load, while still being of the same simplicity as a VSWR meter. The tradeoff is bandwidth. Also, it has other potential uses, as outlined, that a VSWR meter has not.

Acknowledgements

To Magnus Koch, as mentioned above, and to Ingvar Svensson, my teacher at TGG, Göteborg, who had the ability of explaining the Smith chart so vividly that this concept surfaced in one of his more absent-minded students' mind! If all teachers were like him, this world would be a much better place.

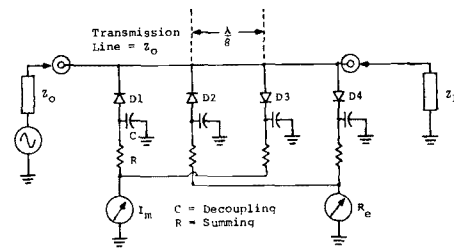


Figure 1(a). Basic Schematic of Impedance Meter.

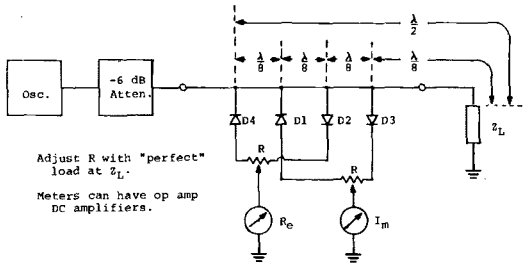


Figure 1(b). Circuit with measurement plane outside 'unknown' connector. Note diode numbering change.

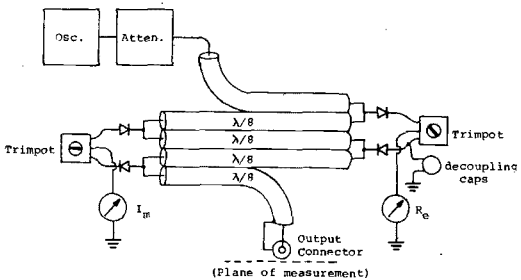


Figure 1(c). Practical construction method.

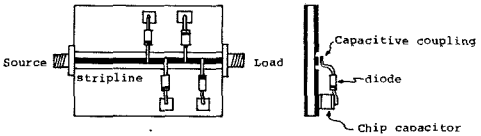


Figure 2. Possible microwave construction method.

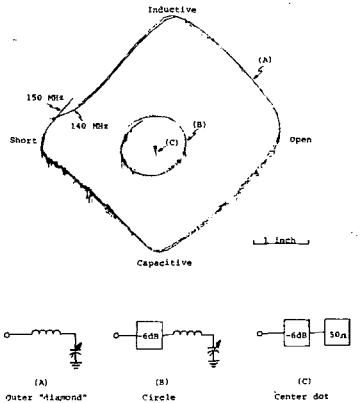


Figure 3. Display of measurements made with Impedance Meter.

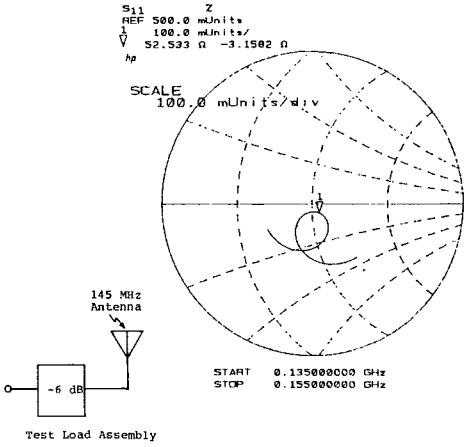


Figure 4. Top plot was made with a Hewlett-Packard 8510 Network Analyzer. The bottom plot is the same load measured with the Impedance Meter. Shapes of the curves are nearly identical, with some differences in rotation of the display and the calibration of the center dot (50 ohm load).

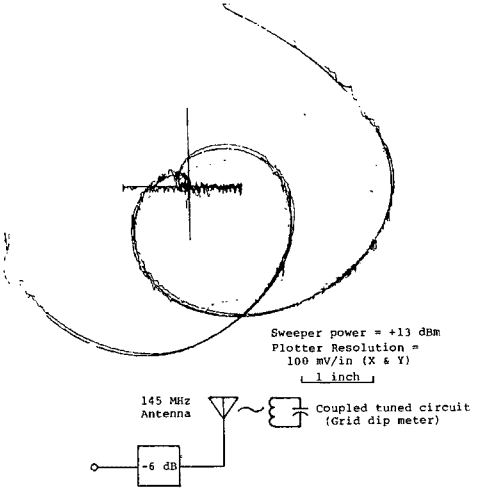
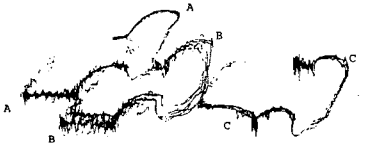
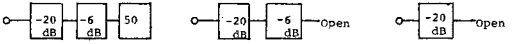


Figure 5. Effects of an additional tuned circuit, coupled to the antenna. As would be predicted, a high-Q response (small loop) occurs at the additional resonant frequency. Light coupling does not greatly disturb the primary antenna response.



Sweeper power = +13 dBm
Plotter resolution = 5 mV/in
(X & Y)

1 inch



Plot A: "perfect" load.

Plot B: 52 dB return loss, (20 + 6) X 2.

Plot C: 40 dB return loss.

Figure 6. Sensitivity demonstration - High sensitivity display can discern difference between "perfect", 52 dB return loss and 40 dB return loss loads. Plot A is a magnification of the center dot in Figure 3.

Efficiency of Envelope-Tracking RF Power-Amplifier Systems

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ABSTRACT

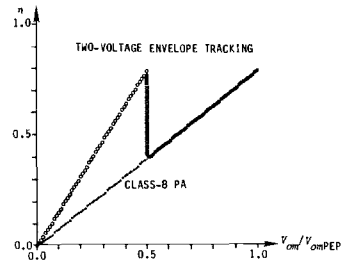
Envelope tracking is a technique for increasing the efficiency of a linear RF power amplifier (PA) by varying its supply voltage to track the envelope of the RF signal. Potential advantages of envelope tracking over other techniques include simple circuitry and usability at any RF frequency, RF bandwidth, and signal bandwidth. Instantaneous power and efficiency characteristics are derived using ideal class-B PAs so that the results can easily be scaled for use with practical PAs. The average efficiencies are then determined as functions of the supply-voltage ratio for a variety of amplitude-modulated signals. The improvement in average efficiency can be quite significant but naturally depends upon the specific type of signal and its peak-to-average ratio. For example, the 28-percent average efficiency of a single-voltage PA with a Rayleigh-envelope signal of 10-dB peak-to-average ratio can be increased to 48 and 57 percent by two- and three-voltage envelope tracking, respectively.

1. INTRODUCTION

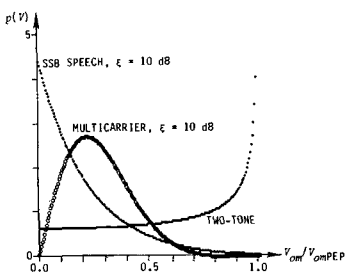
Envelope tracking is a technique for increasing the efficiency of a linear RF power amplifier (PA) by varying its dc supply voltage to track the envelope of the desired output signal. The improvement in efficiency is achieved because the efficiency of almost any PA is proportional (or approximately proportional) to the ratio of its output voltage to its PEP-output voltage. The improvement in efficiency is especially significant when the signal to be amplified has a high peak-to-average ratio, which causes a linear PA to operate in a low-power, low-efficiency region most of the time.

Consider, for example, the curves in Figure 1. The instantaneous efficiency of an ideal class-B PA increases from zero to 78.5 percent as its output increases from zero to peak-envelope power (PEP). The two-tone test signal has a 3-dB peak-to-average ratio and spends most of its time at amplitudes near PEP, hence the ideal class-B PA amplifier has an average efficiency of 61 percent. However, the speech and multicarrier signals more commonly encountered during actual use have larger peak-to-average ratios (e.g., 10 dB), resulting in average efficiencies on the order of 30 percent.

If the PA is operated from half of the full supply voltage, the instantaneous efficiency increases from zero to 78.5 as the RF-output voltage increases from zero to half of the PEP-output voltage, doubling the instantaneous efficiency for low-amplitude signals. For larger instantaneous outputs, the PA must be operated from the full supply voltage, dropping the instantaneous efficiency to that of an ordinary class-B PA. Nonetheless, the average



(a) Instantaneous efficiency



(b) Probability densities

Figure 1. Efficiency and distribution characteristics.

efficiency for signals with a 10-dB peak-to-average ratio is increased from approximately 30 percent to approximately 48 percent.

The block diagram of a two-voltage envelope-tracking system is shown in Figure 2. The envelope of the input signal is detected and compared to a threshold value. When the envelope is larger than the threshold value, V_{DDRF} (the dc supply voltage for the RF PA) is switched to the full dc supply voltage V_{DD}. Otherwise, V_{DDRF} is switched to the lower supply voltage αV_{DD} to reduce power dissipation in the RF PA. The lower supply voltage can be obtained from an efficient switching regulator or from a center connection in a series of batteries.

The concept is readily extended to three or more supply voltages. However, the use of a larger number of supply voltages adds to circuit complexity, thus eliminating one of the advantages of envelope tracking. The supply voltage to the RF driver amplifiers can also be varied to reduce their power consumption. In addition, a switched compensation network can be added to correct for gain and phase changes associated with operation of the PA from different supply voltages.

A number of techniques [1 - 6] are known for implementing high-efficiency RF power amplifiers (e.g., classes D, E, and F) and for combining PAs to increase efficiency (e.g., envelope elimination and restoration, outphasing, and Doherty). Envelope tracking is thus neither the only technique nor necessarily the best technique for improving efficiency. However, it may be the most practical or most effective technique in certain situations, such as when

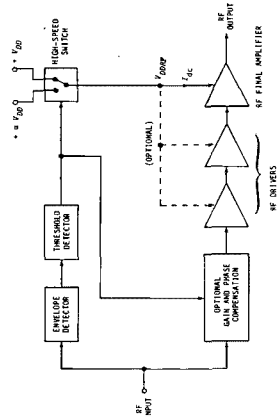


Figure 2. Block diagram of envelope-tracking system.

- The operating frequency is too high for implementation of high-efficiency RF PAs,
- The signal bandwidth is so large that class-S envelope modulators are impractical or inefficient,
- The frequency range of operation is larger than that of the transmission-line couplers required by the outphasing and Doherty techniques, or
- Economic or space considerations do not permit implementation of a class-S envelope modulator.

The objective of this paper is to determine the improvement in efficiency that can be achieved by applying two- or three-voltage envelope tracking to a class-B linear RF PA. While the use of multiple supply voltages in audio PAs has been discussed in the literature [7, 8], little consideration has been given to analogous techniques for RF PAs. To obtain generally applicable results, ideal class-B PAs are assumed. Predictions for a practical PA can be obtained by scaling the results presented here by the efficiency of the PA at peak output.

2. INSTANTANEOUS EFFICIENCY

The characteristics of ideal and practical class-B PAs are discussed in [1]. It is useful to recall that the dc input current for an ideal class-B PA is

$$I_{dc} = \frac{2}{\pi}\frac{V_{om}}{R} \quad , \tag{1}$$

where V_{om} is the output envelope voltage (i.e., $V_{om} \sin \omega t$) and R is the load resistance. Note that I_{dc} is *not* dependent upon supply voltage.

A two-voltage envelope tracking system employs supply voltages of V_{DD} and αV_{DD} where $\alpha < 1$. Linear operation of the RF PA requires its supply voltage to be at least as large as the desired output voltage. The threshold comparison (Figure 2) required to vary the V_{DDRF} (as in Figure 3) is described by

$$V_{DDRF} = \begin{cases} \alpha V_{DD}, & 0 < V_{om} < \alpha V_{DD} \\ V_{DD}, & \alpha V_{DD} < V_{om} < V_{DD} \end{cases} \quad , \tag{2}$$

The resultant dc input power is therefore

$$P_{\ell} = \begin{cases} \alpha V_{DD} I_{dc}, & 0 < V_{om} < \alpha V_{DD} \\ V_{DD} I_{dc}, & \alpha V_{DD} < V_{om} < V_{DD} \end{cases} \quad , \tag{3}$$

The instantaneous dc-input power curves and the corresponding efficiency curves are shown in Figure 4. Note the abrupt decrease in power consumption and increase in efficiency when the V_{DDRF} is switched from the higher supply voltage to the lower supply voltage.

The three-voltage envelope-tracking concept is analogous to the two-voltage concept but employs supply voltages $\alpha_1 V_{DD}$, $\alpha_2 V_{DD}$, and V_{DD}, where $\alpha_1 < \alpha_2 < 1$. The voltage-switching algorithm is described by

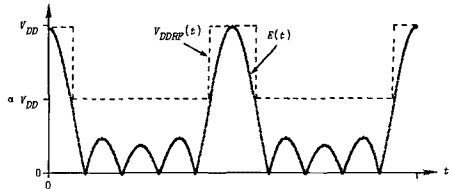


Figure 3. Waveforms in two-voltage envelope-tracking system.

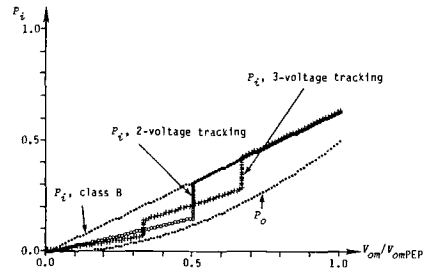
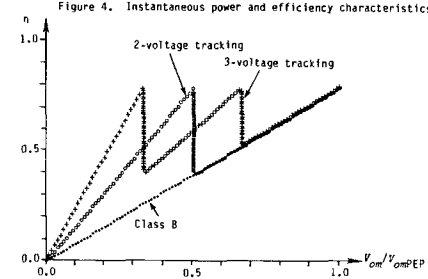


Figure 4. Instantaneous power and efficiency characteristics.



$$V_{DDRF} = \begin{cases} a_1 V_{DD}, & 0 < V_{om} < a_1 V_{DD} \\ a_2 V_{DD}, & a_1 V_{DD} < V_{om} < a_2 V_{DD} \\ V_{DD}, & a_2 V_{DD} < V_{om} < V_{DD} \end{cases} \tag{4}$$

and the corresponding dc input power is

$$P_i = \begin{cases} a_1 V_{DD} I_{dc}, & 0 < V_{om} < a_1 V_{DD} \\ a_2 V_{DD} I_{dc}, & a_1 V_{DD} < V_{om} < a_2 V_{DD} \\ V_{DD} I_{dc}, & a_2 V_{DD} < V_{om} < V_{DD} \end{cases} . \tag{5}$$

The instantaneous power input and efficiency curves are also shown in Figure 4.

3. AVERAGE POWER INPUT AND EFFICIENCY

Average efficiency [1, 9] is defined as the ratio of the average RF-output power to the average dc-input power; i.e.,

$$\eta_{AVG} = P_{oAVG} / P_{iAVG} . \tag{6}$$

The average powers are determined by integrating the instantaneous powers weighted by the envelope probability-density function (p.d.f.) over the range of envelope values:

$$P_{oAVG} = (1/2) \int_0^{V_{omPEP}} V_{om}^2\, p(V_{om})\, dV_{om} \tag{7}$$

and

$$P_{tAVG} = \int_0^{V_{omPEP}} P_t(V_{om})\, p(V_{om})\, dV_{om} \quad . \tag{8}$$

The peak-to-average ratio is defined by

$$\xi = P_{oPEP} \,/\, P_{oAVG} \quad . \tag{9}$$

A number of useful p.d.f.s are defined in [5] and [9]. For the uniform p.d.f., the dc input power and maximum-efficiency values of α, α_1, and α_2 can be determined analytically. However, for the other p.d.f.s, the evaluation is most readily accomplished numerically.

Selected Signals

Single-sideband suppressed-carrier (SSB/SC) transmitters are commonly tested with a two-tone signal, while full-carrier AM transmitters are commonly tested with a single-tone modulating signal. Some types of amplitude companders are said to produce a nearly uniform amplitude distribution. Quadrature amplitude modulation (QAM) is being used with increasing frequency in data-transmission systems because of its ability to pack a large number of bits into a single data symbol. All of these selected signals have relatively low peak-to-average ratios.

The average efficiency of two-voltage envelope tracking with the four selected signals is shown in Figure 5 as a function of the transition ratio α. The maximum average efficiency attainable with both two- and three-voltage envelope tracking as well as the corresponding average efficiency for a single supply voltage are given in Table 1. For these signals, two-voltage tracking

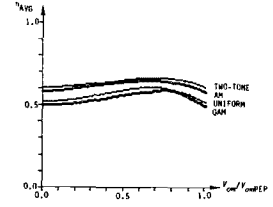


Figure 5. Average efficiency of two-voltage tracking with selected signals.

SIGNAL	ξ, dB	η_{AVG} class-B	Two-Voltage Tracking max η_{AVG}	α	Three-Voltage Tracking max η_{AVG}	α_1	α_2
Two-tone	3,0	0,614	0,673	0,71	0,701	0,56	0,82
AM	4,3	0,587	0,655	0,66	0,687	0,50	0,79
Uniform	4,8	0,524	0,615	0,67	0,658	0,52	0,78
QAM	4,8	0,484	0,605	0,71	0,653	0,57	0,76
Rayleigh	5,0	0,455	0,580	0,63	0,635	0,50	0,73
Rayleigh	6,0	0,423	0,561	0,61	0,621	0,48	0,71
Rayleigh	7,0	0,387	0,540	0,58	0,607	0,45	0,68
Rayleigh	8,0	0,350	0,519	0,55	0,592	0,42	0,65
Rayleigh	9,0	0,314	0,498	0,52	0,578	0,39	0,61
Rayleigh	10,0	0,280	0,479	0,49	0,566	0,36	0,57
Rayleigh	11,0	0,250	0,462	0,45	0,556	0,33	0,53
Rayleigh	12,0	0,223	0,448	0,42	0,547	0,30	0,49
Rayleigh	13,0	0,198	0,435	0,39	0,540	0,28	0,46
Rayleigh	14,0	0,177	0,424	0,36	0,534	0,25	0,42
Rayleigh	15,0	0,158	0,414	0,33	0,529	0,23	0,39
Rayleigh	16,0	0,140	0,405	0,30	0,524	0,20	0,35
Rayleigh	17,0	0,125	0,397	0,28	0,520	0,18	0,32
Rayleigh	18,0	0,112	0,390	0,25	0,516	0,17	0,29
Rayleigh	19,0	0,099	0,383	0,23	0,513	0,15	0,27
Rayleigh	20,0	0,089	0,377	0,21	0,509	0,14	0,24
Laplacian	5,0	0,401	0,537	0,55	0,601	0,40	0,68
Laplacian	6,0	0,386	0,527	0,53	0,594	0,38	0,67
Laplacian	7,0	0,369	0,516	0,52	0,585	0,37	0,65
Laplacian	8,0	0,350	0,504	0,50	0,576	0,36	0,64
Laplacian	9,0	0,330	0,490	0,48	0,566	0,34	0,62
Laplacian	10,0	0,308	0,475	0,47	0,555	0,32	0,60
Laplacian	11,0	0,286	0,459	0,45	0,543	0,31	0,58
Laplacian	12,0	0,263	0,443	0,43	0,531	0,29	0,56
Laplacian	13,0	0,240	0,425	0,41	0,518	0,27	0,53
Laplacian	14,0	0,217	0,408	0,39	0,505	0,25	0,51
Laplacian	15,0	0,195	0,391	0,37	0,492	0,24	0,49
Laplacian	16,0	0,175	0,375	0,35	0,480	0,22	0,46
Laplacian	17,0	0,157	0,359	0,33	0,469	0,20	0,43
Laplacian	18,0	0,140	0,345	0,31	0,459	0,19	0,41
Laplacian	19,0	0,125	0,332	0,29	0,449	0,17	0,38
Laplacian	20,0	0,111	0,320	0,27	0,441	0,14	0,36
Gaussian AM	5,0	0,478	0,594	0,66	0,645	0,54	0,76
Gaussian AM	10,0	0,431	0,565	0,65	0,644	0,54	0,72
Gaussian AM	15,0	0,405	0,610	0,62	0,671	0,53	0,66
Gaussian AM	20,0	0,397	0,653	0,58	0,707	0,52	0,61
Laplacian AM	5,0	0,455	0,595	0,65	0,648	0,54	0,73
Laplacian AM	10,0	0,425	0,598	0,62	0,655	0,54	0,70
Laplacian AM	15,0	0,405	0,590	0,59	0,678	0,53	0,65
Laplacian AM	20,0	0,397	0,570	0,57	0,709	0,52	0,61

Table 1. Maximum average efficiencies and corresponding voltage ratios.

makes a significant improvement in average efficiency but three-voltage tracking makes only a small additional improvement.

Multicarrier and SSB/SC Voice

The envelope of bandlimited Gaussian noise has a Rayleigh distribution [10]. The envelope of the sum of a large number of independent RF carriers (with either FM or AM) also tends to have a Rayleigh distribution. The average efficiency of two-voltage envelope tracking with Rayleigh-envelope is shown in Figure 6 for peak-to-average ratios of 5, 10, 15, and 20 dB. The maximum average efficiency (obtained with proper choice of α) is shown in Figure 7 for peak-to-average ratios from 5 to 20 dB. Average-efficiency contours for three-voltage envelope tracking with $\xi = 10$ are shown in Figure 8.

For $\xi = 5$ dB, the improvements are similar to those obtained with the four selected signals. However, the improvement in average efficiency becomes much more significant as the peak-to-average ratio increases (Figure 8). For example, at $\xi = 10$ dB, the 28-percent average efficiency of a single-voltage PA is increased to 48 percent by two-voltage envelope tracking and to 57 percent by three-voltage tracking. For $\xi = 20$ dB, the average efficiency is increased from a meager 8.9 percent to 38 and 51 percent by two- and three-voltage envelope tracking, respectively. Note that the effect of the transition voltage increases as the peak-to-average ratio increases.

The envelope of an SSB/SC signal produced by speech has a Laplacian (one-sided exponential) distribution. The average efficiency as a function of transition voltage is shown in Figure 9 for Laplacian-envelope signals with

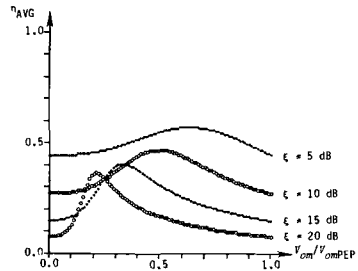


Figure 6. Average efficiency of two-voltage tracking with Rayleigh envelope.

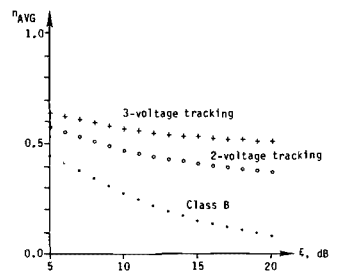


Figure 7. Maximum average efficiency of two-voltage tracking for Rayleigh envelope.

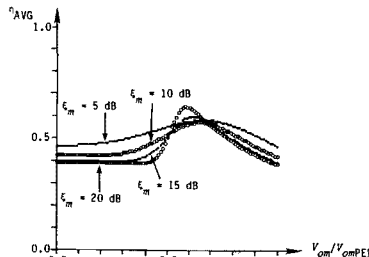


Figure 11. Average efficiency of two-voltage tracking with Laplacian-AM signals.

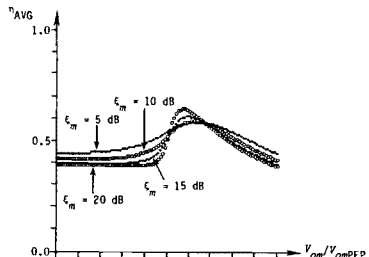


Figure 12. Maximum average efficiencies and corresponding voltage ratios.

added by envelope tracking are:

- PA gain and phase variation with supply voltage and
- Envelope distortion produced by finite switching time.

Gain and Phase Variation

Virtually all solid-state power transistors (whether BJT or FET) contain significant voltage-variable capacitance. In addition, most FETs have inherently nonlinear transfer characteristics. As a result, variation of the supply voltage produces unwanted amplitude and phase modulation of the output signal.

Typical curves of gain and phase variation for a bipolar RF-power transistor [11] suggest maximum deviations of 2 dB and 5°. However, the contours further suggest that simultaneous reductions in supply voltage and drive result in nearly constant gain and phase characteristics.

In general, determination of the carrier-to-intermodulation (C/I) level requires numerical evaluation based upon a particular signal and PA characteristic. However, some idea of the tolerable gain and phase changes can be obtained by considering the spectrum of squarewave modulation.

Squarewave amplitude modulation between two levels that differ by 0.42 dB results in third-order IMD products 30 dB below the carrier. Squarewave phase modulation produces third-order products whose amplitude is $2\Delta\phi/3\pi$ relative to a unity-amplitude carrier. Consequently, a phase jump of 5.7° (0.1 rad) produces a C/I ratio of 30 dB. It therefore appears that phase variations are not likely to be a problem, while gain variations must be compensated if they

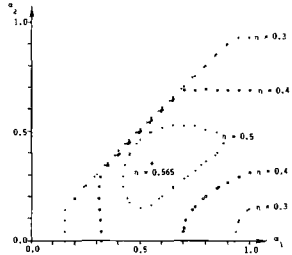


Figure 8. Average-efficiency contours for three-voltage tracking with Rayleigh envelope, ζ = 10 dB.

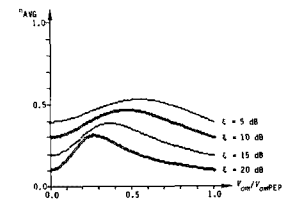


Figure 9. Average efficiency of two-voltage tracking with Laplacian envelope.

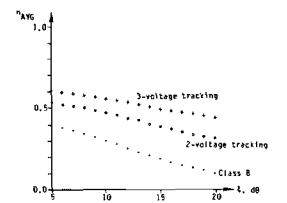


Figure 10. Maximum average efficiency for Laplacian envelope.

peak-to-average ratios of 5, 10, 15, and 20 dB. The maximum attainable average efficiency as a function of peak-to-average ratio is shown in Figure 10 and values of α are given in Table 1.

The average-efficiency characteristics for a Laplacian envelope are similar to those for a Rayleigh envelope. For a typical 10-dB peak-to-average ratio, the 30.8 percent efficiency of class B is increased to 47.5 percent by two-voltage envelope tracking, and to 55.5 percent by three-voltage envelope tracking.

Amplitude Modulation

The modulating signals for full-carrier AM typically have either Gaussian distributions (corresponding to music or the sum of a variety of sounds) or Laplacian distributions (corresponding to speech). The average-efficiency curves for two-voltage envelope tracking with these two signals are shown in Figures 11 and 12 for several modulation peak-to-average ratios.

The maximum average efficiencies and the corresponding transition voltages are given in Table 1. Since the RF peak-to-average ratio for these signals is relatively low, their average-efficiency characteristics are similar to those of the selected signals.

4. PRACTICAL CONSIDERATIONS

Application of envelope tracking requires consideration of intermodulation distortion (IMD) as well as efficiency. The two principal sources of IMD

exceed 0.42 dB.

Switching Time

Delays in switching to the higher supply voltage can distort the envelope, producing IMD. In general, the C/I ratio depends upon both the type of signal and the transition ratio α. However, useful insight is obtained by considering the results of simulations of two-tone signals with $\alpha = 0.5$.

A pure delay in the voltage transition produces a C/I of 30 dB or more when the delay is less than 0.1 s / B(Hz). Similarly, a linear (ramp) transition between voltage levels produces a 30-dB or better C/I ratio provided the total risetime does not exceed 0.6 s / B(Hz). These do not appear to produce unreasonable switching-time requirements for most applications. For example, delays of up to 35 μs or risetimes of up to 200 μs can be tolerated for ordinary SSB voice with bandwidth $B = 3$ kHz.

5. CONCLUSIONS

Envelope tracking can be implemented by adding relatively simple and inexpensive hardware to an existing RF power amplifier. This paper shows that it can produce significant increases in average efficiency for amplitude-modulated signals with large peak-to-average ratios. The power-supply switching-time requirements are quite reasonable for voice-bandwidth signals. Envelope tracking should therefore be considered when improved efficiency is desired.

6. ACKNOWLEDGEMENTS

This paper is based in part upon work sponsored by Spar Aerospace Limited, Ste-Anne-de-Bellevue, Quebec, Canada.

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Direct Single Sideband Modulation of Transmitter Output Switcher Stages

Florin G. Tinta

Abstract

A new technique allows to obtain Single Sideband (SSB) Pulse Duration Modulation without using intermediate DSB signals.

The technique employs instantaneous voltage comparison between modulating and carrier waveforms and between their harmonic conjugates. Timing signals are generated at instantaneous value equality. Through a set of logic gates, these timing signals are applied to a system of master flip-flops, driving switching output stages for power RF transmitters.

In the simplest implementation two such master flip-flops drive differentially the halves of a switching bridge generating a three-level output (1,0,-1). All digital FFT based real-time processing can generate output signals free of the third and all even harmonics using high efficiency five-level bridges operated in the top 92% of their nominal power output.

I INTRODUCTION

In general, SSB signals are obtained from Double Sideband Suppressed Carrier (DSB) signals. DBS modulators have always been used as a first explicit processing step of the transmitted signal.

The most conventional method consists in eliminating one of the sidebands of the DSB signal by filtering at low power level.

A second method uses phase shifting and several versions of this phase-shift method exist [1], [2]. The output of two DSB modulators supplied with harmonic conjugate (i.e., 90° phase shifted) modulating and carrier waveforms are combined by linear addition. This cancels one of the sidebands and enhances the other if the modulators and the phase-shifting networks are ideal. It implies perfect balancing of modulator non-linearities and requires practically very delicate control of amplitudes and phases.

A third method [3] for SSB generation has four DSB modulators, low-pass filters and a final adding circuit. Again, perfect balancing is required for mutual cancellation of the unwanted sidebands.

Pulse Duration Modulation (PDM or PWM) can be applied directly for amplitude modulation of RF carriers [4].

The pulse duration is tailored in such a way that there is a linear relation between the magnitude of the modulating signal and the fundamental amplitude of the pulse train. As a result, the pulse duration is related to the

magnitude of the modulating signal in a non-linear way. The fundamental amplitude A_1 of a periodic sequence of bipolar pulses of duration t_o, period T_c and unit amplitude is given by:

$$A_1 = 4/\pi \sin(\pi t_o/T_c) \quad (1)$$

This relation leads to modulation techniques based on instantaneous voltage comparison between a sinusoidal carrier and the modulating signal. This will be discussed later in more detail. Full amplitude modulated transmitters using such techniques have been built [5]. Possible extension to the generation of DSB signals has been also indicated [5] and practical circuits presented [6]. Indirect generation of SSB signals by adding phase shifted DSB PDM appears also feasible. Limitations of methods of combining outputs of DSB modulators have been mentioned [5]. Alternative ways of producing SSB PDM signals using Kahn's approach [7] were considered. The method of envelope elimination and restoration has received some refinements by using feedback loops[8]. Nevertheless, this approach has some inherent limitations in the phase tracking circuit (for complex and extended dynamic range modulating signal) and is basically indirect, in the sense that the SSB signals are generated by conventional means at low level. A PDM power amplifier using transistor switching bridges for the envelope restoration allowed to obtain an SSB transmitter with unusually high efficiency [9].

The object of the following paper is the generation of SSB PDM waveforms without the explicit use of DSB signals at a level of efficiency at least comparable with the best AM PDM modulated systems. Digital processing of the transmitted signal makes it possible to generate more efficient waveforms which are reducing loss in harmonic power and filtering circuit difficulties.

II SWITCHING CONCEPTS

a. DSB Pulse Duration Modulator

This is presented mostly for conceptual definitions. Figure 1 shows the block diagram of a Double Sideband Suppressed Carrier Pulse Duration Modulator designed to drive differentially a full switching bridge. Two master flip-flops, F1 and F2 are triggered by two pairs of voltage comparators C1 and C2.

The modulating signal in "normalized" to the carrier amplitude, i.e., its amplitude to smaller and at most equal (for m = 1) with the amplitude of the carrier.

The first comparator pair C1 receive the carrier c(t) and the modulating signal s(t) while for the second comparator pair the sign of one of these voltages is reversed.

At instantaneous voltage equality one can have "positive" or "negative" crossing of the applied waveforms if one connects the relative magnitude of their first time derivatives and it is rather simple to produce separate signals corresponding to these two situations.

In the example selected in Figure 1, one uses distinct comparators. C1+ produces a positive trigger forming pulse when the carrier exceeds the modulating signal immediately after crossing, while C1- produces the positive trigger where the carrier "goes under" the modulating signal.

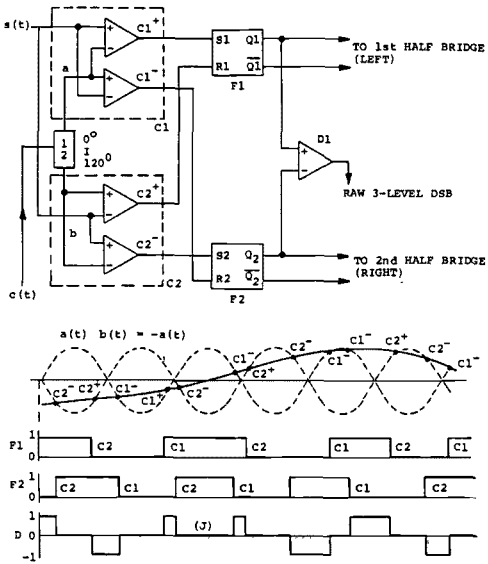

Figure 1. DSB Pulse Duration Modulation

The second comparator pair operates in a similar way. The situation shown in Figure 1 corresponds to a 180° phase shift of the carrier.

F1 is set at positive crossings s(t) by c(t) and reset at positive crossings of s(t) by -c(t).

F2 is set by negative crossings of s(t) by -c(t) and reset at negative crossings of s(t) by c(t).

The outputs of F1 and F2 shown in Figure 1 correspond to a sinusoidal carrier and slow-varying, sign-changing modulating signal. They drive the independently controlled halves of a three-level switching bridge whose basic arrangement is indicated in Figure 2. Biasing, snubbering and circuit details are left aside for clarity.

One can see from that in this arrangement the output signal delivered by the transformer U depends upon the difference of the switching commands given by F1 and F2. For a bipolar (output), PDM requires at least a three-state or three-level (1,0,-1) configuration.

In a three-level bridge, such a differential arrangement has definite advantages in switching conditions for transistors, easing snubbing problems. It is evident that at zero mediated transitions, the U-C circuit will include a pair of conducting transistors (Q1 and Q2, Q3 and Q4).

Of course, an identical three-level waveform can be obtained by using a less sophisticated difference circuit, also represented in Figure 1.

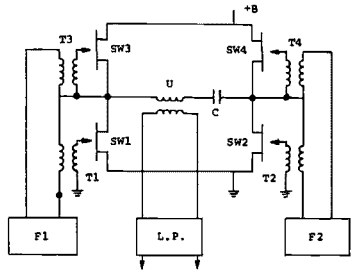

Figure 2. Three Level (Bipolar) PDM Bridge

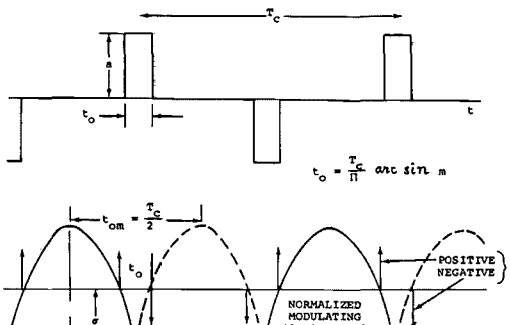

Figure 3. Bipolar Pulse Duration Modulation by a DC Signal

This waveform satisfies condition (1) for a DBS (SC) radio frequency Pulse Duration Modulation. The duration of a pulse defined by the alternating crossing of 180° phase shifted carrier waveforms satisfies the equivalent relation:

$$t_o = T_c/\pi \text{ arc sin } m \qquad (2)$$

Figure 3 illustrates the situation for a constant normalized modulating signal of amplitude m (the modulation index). Polarity reversal of the modulating signal (region j in Figure 1) results in the 180° phase shift characteristic of DSB (SC) modulated signals.

b. Three Level SSB Pulse Duration Modulator

The switching bridge of Figure 2 can be used to generate bipolar SSB PDM signals. A different control of the two driving flip-flops is required.

In Figure 4, F1 and F2 are controlled by a combination of command signals originated in four pairs of comparators and logic gates. An upper side band PDM signal is generated by this arrangement; the lower side band can be alternatively generated by reversing a couple of internal connections. Like in the phase-shifting method [2] [3] harmonic conjugates of at least the modulating signal are generated by 90° (or 45° alternates) phase shifting all pass filters, but the similarity ends at this point. An explicit DSB is nowhere generated in this circuit.

Comparator pairs C3 and C4 are supplied with the modulating and carrier signals, the latter being shifted with 180° in phase (sign reversal) for C4.

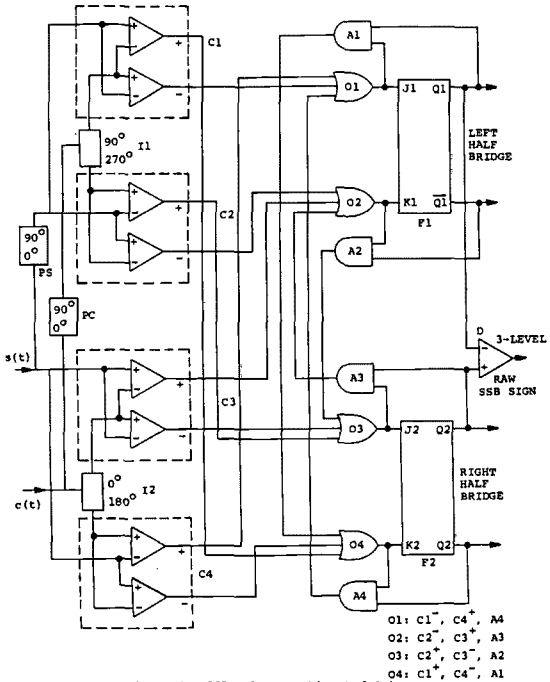

Figure 4. SSB Pulse Duration Modulator

Comparator pairs C1 and C2 are supplied with the harmonic conjugates [1] of the same signals. This implies the use of 90° (or 45° alternates) phase shifting all pass filters for the modulating signal at least. For a sinusoidal carrier a single frequency phase shifter can be employed.

Regular as well as J-K type flip-flops may be used. In Figure 4, clock inputs for J-K flip-flops and some delay circuits have been not represented in order to preserve with more clarity the basic concept. Clock signals can be used for further refinements of this modulation technique.

The outputs of F1 and F2 (which are not DSB PDM signals) are applied differentially to the switching bridge of Figure 2. The bridge produces three level waveforms which in general may contain successive pulses of the same polarity. One can show that for carrier to modulating signal frequency ratios R>3 the maximum number of successive pulsed of same polarity is two. Figure 5 shows the particular case of the upper SSB PDM signal produced for R = 3, at a modulating index m = .65. The sequence is bipolar, with no successive pulses of same polarity.

For m = 1, the SSB pulse duration modulation produced by this technique uses the full half period, i.e., generates a square wave with direct transitions from +1 to -1 and vice versa and gets the maximum power which can be generated by a full switching bridge.

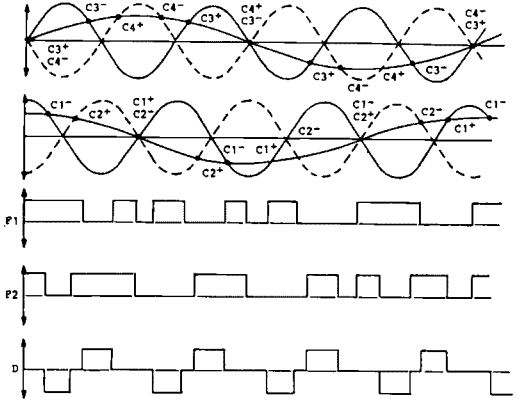

Figure 5. Direct Generation of Constant Amplitude Raw SSB Signal (m = .65, R = 3)

This can be simply demonstrated by considering sinusoidal constituents of the modulating and carrier waveforms. Let us consider the time angle θ_c of the carrier when the instantaneous values of the modulating sinusoid of amplitude m and of a sinusoidal carrier of unit amplitude become equal in absolute value. The time angle for the modulating signal is θ_c/R, where $R = f_c/f_m$. Both angles are measured from a common origin. Flip-flop transitions appear when:

$$\sin \theta_c = \left| m \cdot \sin (\theta_c/R) \right| \qquad (3)$$

The absolute value condition represents the fact that conjugate comparator pairs receive sign changed carrier signals.

Equation (3) is transcendental and can be solved by numerical methods (one of the solutions has been used in Figure 5).

If m = 1, we have $\sin \theta_c = \left| \sin \theta_c/R) \right|$ (4)

and the solutions are given by the following:

$$n \cdot \pi \pm \theta_c = \theta_c/R \qquad (5)$$

The solutions of equation (7) extend to all trigonometric functions and in particular to

$$\cos \theta_c = \left| \cos (\theta_c/R) \right| \qquad (6)$$

which represents the condition for instantaneous value equality of the harmonic conjugate waveforms.

This means that upward and downward transitions in the paired flip-flop outputs Q1 and $\overline{Q1}$, Q2 and $\overline{Q2}$ (Figure 4) are simultaneous. This implies two level transitions from 1 to -1 and vice versa. The result is a square wave: QED.

III DIGITAL GENERATION OF SSB-PDM SIGNALS

A review of digital alternatives of the operations involved in SSB-PDM generation is given below. In addition, the case of five level (2,1,0,-1,2) switching bridges is considered. For multi-level switching bridges which can generate waveforms with reduced harmonic content at high power level, analog approaches, although possible for a certain dynamic range, do not seem practical.

The relative situation of SSB-PDM generation methods is given in Figure 6. For generality indirect methods based on low level analog DSB/SSB signal production followed by envelope AM-PDM restoration are also indicated. Dotted lines show various possible combinations of methods.

a. Harmonic Analysis and Conjugation of Signals

The modulating signal can be sampled and subject to real-time FFT processing for bandwidths covering at least the audio frequency range by using now readily available microprocessors and allied circuits. This may constitute a first step for digitally generating 90° phase shifted response, i.e., the harmonic conjugate of the modulating signal.

For the carrier quadrature signals can be simply generated by divide-by-four flip-flops [10].

Initially, the application of SSB-PDM signal generation was considered for emergency transmissions in the LF

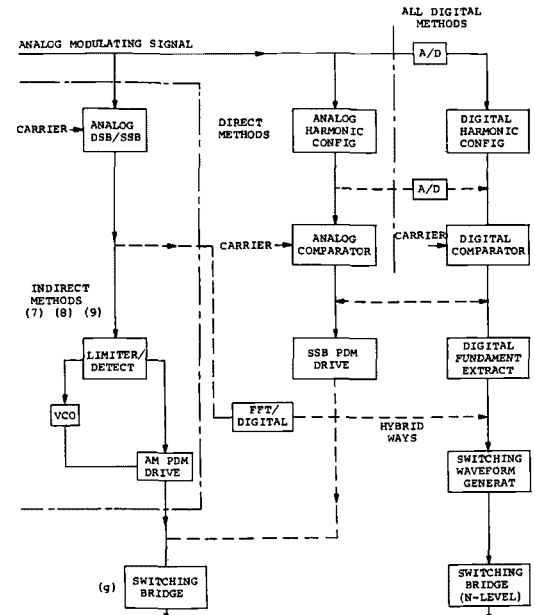

Figure 6. Map of SSB PDM Methods

range, but it appears that with fast processors the scope and the frequency range of such transmissions can be considerably enlarged.

Digital harmonic conjugation of signals will not be discussed further in this paragraph. Analog constant phase delay, all pass filters have been constructed over wide frequency ranges. Our experience showed that they can be very adequate for carriers in the 2 to 32 MHz range (4 octaves) in spread spectrum transmission techniques.

b. Digital Comparison

High resolution video frequency A/D are commercially available. The digitized modulating signal can be compared with the stored or analytically generated carrier waveform, at a normalized scale.

Negative and positive waveform crossing in the sense defined previously can be easily defined and their timing accuracy is determined by the clock rate ratio to the highest frequency involved in the signals.

This operation can be done in parallel (or in a serial way, by successive sampling) for sign changed carrier and for the harmonic conjugated of the modulating signals generated in either analog or digital way.

c. Digital Evaluation of the SSB Fundamental

The fact that the SSB-FDM signal is a succession of pulses of constant amplitude makes the evaluation of the fundamental component by numerical methods straightforward. Because no power generation is considered at this level, it is advantageous to use unipolar (1,0) pulse sequences instead of bipolar (1,0,-1).

Th fundamental can be simply evaluated by the sum of sampled values of a sinusoidal by the gated clock pulses.

The simplicity of operations involved allows their implementation in real time with the help of now commercially available microprocessors, for ranges of modulating and carrier signals covering many telecommunications applications.

Digital evaluation of the fundamental for an analog generated SSB is somewhat more complex, but still it can be performed in real time using FFT algorithms. This is indicated in Figure 6 as a hybrid way which may be considered an extension of the Kahn's method [7].

d. Five Level Switching Bridges

Bipolar five level waveforms generation can be generated by a switching bridge of the type represented in Figure 7. The normalized (supply) levels are 2,1,0,-1 and-2. A generic example is given in Figure 8a.

Up to a scale factor of $\pi/4$, the fundamental amplitude is given by:

$$A = \int^{u} 2 \cos wdw + \int^{v} \cos wdw = \sin u + \sin v$$

$$A = 2 \sin \frac{u+v}{2} \cos \frac{u-v}{2} \qquad (7)$$

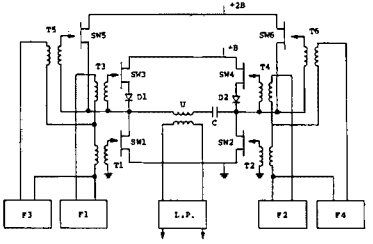

Figure 7. Five Level (Bipolar) Switching Bridge

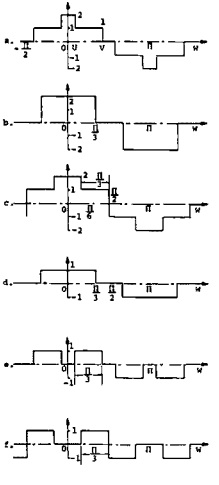

Figure 8. Switching Waveforms Eliminating the 3rd Harmonic in SSB PDM

Natural limitations can be described by:

$$\pi/2 \geq v \geq u \geq 0 \qquad (8)$$

The symmetry of the waveform eliminates even harmonics.

The third harmonic can be eliminated if:

$$\sin 3u + \sin 3v = 0 \qquad (9)$$

which, considering (8) leads to the conditions:

$$v - u = \pi/3 \qquad (10)$$

or

$$v + u = 2\pi/3 \qquad (11)$$

The fundamental amplitude of a five level waveform satisfying (10) results from (7).

$$A(\bar{1}) = 2 \sin \frac{u+v}{2} \cdot \frac{\sqrt{3}}{2} = \sqrt{3} \sin(v - \pi/6) \qquad (12)$$

This relation indicates that an analog timing method similar to the one presented in Section II is possible.

Condition (11) leads to a different relation:

$$A(\bar{1}) = \sqrt{3} \cos(v - \pi/3) \qquad (13)$$

$$A(\bar{1})M = \sqrt{3} \qquad (13a)$$

The maximum amplitude of the fundamental following relation (13) corresponds to $\sqrt{3}$, for $u = v - 60°$, a three level degnerate waveform shown in Figure 8b.

For decreased fundamental amplitude while satisfying limitation (8) u shall decrease also, while v shall grow. The minimum amplitude obtainable in this way corresponds to 3/2 for $u = 30°$, $v = 90°$. This satisfies in the same time condition (10) and is the maximum which can be obtained according to the relation (12).

A particular solution of (13), corresponding to u = 42°, v = 78° given $A(\lambda) = 1.647$ and simultaneously eliminate the third and the fifth harmonic. Such a waveform can be used for high efficiency phase modulated or keyed transmitters. From this level down one has to reduce both u and v under the condition (10) up to u = o, as shown in Figure 8c. In this range one has again elimination of the fifth harmonic for u = 6° and v = 66°.

The amplitude of the fundamental at u = o, v = 60 is half of the value given by (13a).

$$A(\lambda)L = \sqrt{3} \sin \frac{\pi}{6} = \frac{\sqrt{3}}{2} \qquad (14)$$

Below this fundamental level one can generate third harmonic free waveforms by splitting the pulse in the center and moving the two halves toward $v = \pm \pi/2$ limits. Such a waveform is shown in Figure 8d. One can show that for third harmonic elimination the duration of each resulting pulse should be $\pi/3$.

In split pulse mode the amplitude of the fundamental is

$$A(\lambda)S = \sin v - \sin u = 2 \sin \frac{v-u}{2} \cos \frac{v+u}{2} \qquad (15)$$

where u indicates this time the o to 1 transition. For

$$v - u = \pi/3 \text{ and } v = \pi/2$$

one gets the minimum findamental amplitude

$$A(\lambda)m = \cos \pi/3 = 1/2 \qquad (16)$$

Below this level the third harmonic cannot be eliminated, in switching waveforms with only four switching transitions (or maximum two pulses) per half period.

The power range in which the amplitude of the fundamental can be continuously varied and the third harmonic eliminated is given by the ratio:

$$P = \frac{A(3)^2}{A(3)m} = 12 \qquad (19)$$

which corresponds to the top 92% of the maximum power output. The complications of adaptive transitions between various modes involved in extending the range have to be traded against high power LC filtering hardware.

IV CONCLUSION

The renewed interest in SSB communications comes at a time when the development of fast switching electronics appears to give the possibility of new approaches in generating and modulating power RF signals. New modulation systems are made possible by circuitry developed for digital techniques. Such applications in the audio domain are now well established.

Advances in Fast Digital Signal Processing may result in further reconsideration of traditional modulation methods leading to new levels of quality, efficiency and adaptability. Application Specific Integrated Circuits (ASIC) allowing extremely rapid FFT may contribute to the spread and economic viability of complex modulation techniques in conventional and spread spectrum communications. The present paper gives indirectly some hints on future development possibilities.

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Chapter II

PIN Diodes and the Theory of Microwave Operaton

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A. The PIN Diode – An Extension of the PN Junction

1. Structure

The PIN diode should not be thought of as something physically different from the PN junction discussed in Chapter I, but rather different in a sense of degree. In Chapter I we saw that with the abrupt junction the width of the depletion zone is inversely proportional to the resistivity of the P or N region, whichever has the lesser impurity doping concentration. As the width of the depletion zone increases, the capacitance per unit area of the junction decreases. This effect is very beneficial for a diode which is intended for use as a microwave switch because the lower the capacitance the higher the impedance of the diode under reverse bias, and the more effective the device is as an "open circuit."

The limiting case of high resistivity material is undoped (or "intrinsic") *I* silicon. In practice, of course, no silicon material is without some impurities. A practical PIN diode, then, consists of an extremely high resistivity P or N zone between low resistivity (highly doped) P and N zones at its boundaries, as shown in Figure II-1. To distinguish unusually heavily or lightly doped material, special nomenclature has evolved. Heavily doped P and N materials are referred to as P+ and N+, respectively. To identify very lightly doped, high resistivity P and N material, the Greek letters are used; thus high resistivity P material is called *π-type* and high resistivity N material is called *ν-type*. Recognizing that perfectly intrinsic material is not practically obtainable, the I region of a PIN diode can consist of either *ν*- or *π*-type material. The result-

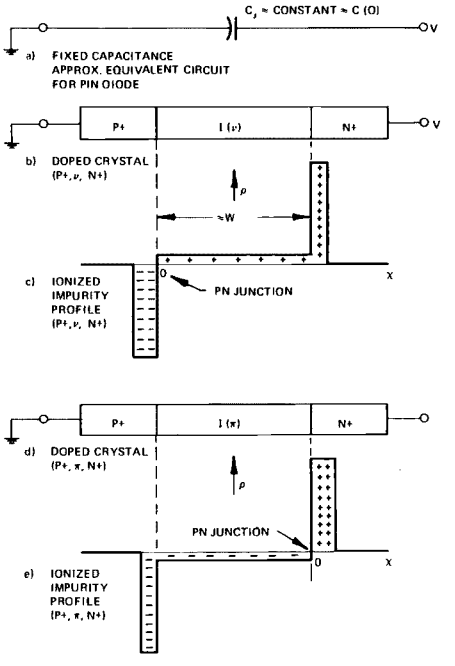

Figure II-1 Profiles for the Two PIN Diode Types

ing diodes are indistinguishable from a microwave point of view; however, the actual junction forms at opposite ends of the intrinsic zone depending on the choice. This distinction is diagrammed for both cases in Figure II-1.

The first type shown in Figure II-1(b) shows a P+, ν, N+ diode structure. If the I region is of sufficiently high resistivity, what few impurity atoms it has will be ionized and the depletion zone will extend throughout the I region and include a small penetration into both the P and N regions. Because of the heavy doping in the P+ and N+ zones the depletion zone will not extend very far into them, and the depletion zone will be essentially equal to the I layer width, W_I. The alternate diode structure, P+, π, N+ is shown schematically in Figure II-1(d). Here the depletion zone width is likewise approximately equal to the width of the intrinsic layer but the junction is formed at the N+ interface rather than that of P+. Controlling the location of the junction has important consequences from the standpoint of passivating the diode chip, but no impact on performance. Most PIN diodes use ν material for the I region and the junction is formed at the P+ interface.

2. *C(V) Law and Punchthrough Voltage*

In the preceding section it was assumed that the I layer is of such high resistivity that, even with no applied bias, the depletion zone extends across the I layer to the P+ and N+ zones. Under such circumstances C_j is practically independent of applied voltage. At zero voltage the depletion zone has already extended through the I region; as further reverse bias is applied to the diodes, little further widening of the depletion zone proceeds because of very high impurity concentrations and correspondingly large availability of ionizable donors and acceptors in the P+ and N+ regions.

The PIN diode which actually does have so high a resistivity I layer that it is depleted at zero bias is called a *zero punchthrough* diode, because the depletion zone has "punched through" to the high conductivity zones even before bias is applied.

Such a situation, however, represents an idealization. Not all practical diodes are zero punchthrough. A more *general definition of the PIN is a semiconductor diode which consists of two heavily doped P and N regions separated by a substantially higher resistivity P or N region.*

Figure II-2 shows schematically a practical PIN diode with ionized impurity profiles at zero bias and at punchthrough. At zero bias a

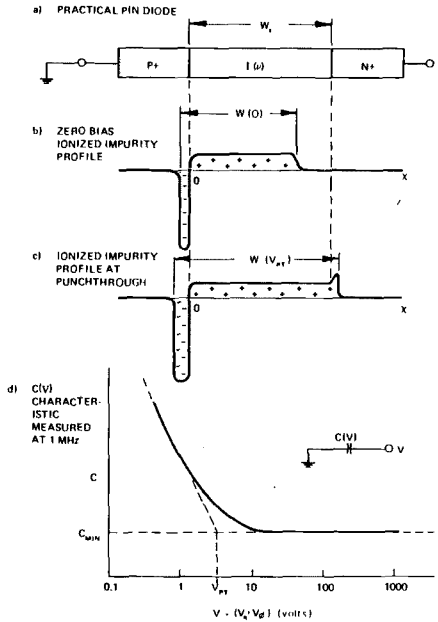

Figure II-2 Practical PIN and Reversed Punchthrough Characteristics

large portion, but not necessarily all, of the I region impurities have been ionized and the depletion zone, W(0), may be somewhat less than the I layer width, W. As reverse bias voltage is applied to

this diode, depletion layer spreading occurs, and the capacitance, shown in Figure 11-2(b), decreases until the depletion layer has spread definitely to the N+ region, as shown in Figure 11-2(c). At this voltage the depletion layer width, $W(V_{PT})$, is approximately equal to W_I. Further spreading of the depletion layer into the low resistivity P+ and N+ regions is, for most applications, negligible. The voltage at which the depletion zone just reaches the N+ contact is the punchthrough voltage, V_{PT}.

Because in practice the resistivity levels in the P+, I, and N+ regions do not change abruptly, the resulting capacitance versus voltage characteristics have a *soft knee*. Therefore the punchthrough voltage is not directly measureable with precision. However, the practical diode usually does have two definable slopes in its C(V) characteristic, *when plotted using semilog paper as shown in Figure 11-2(d). By convention, the voltage intersection of these two straight line projected slopes is called the punchthrough voltage.*

It is to be emphasized that this C(V) characteristic is what one obtains when the measurements are made at relatively low frequencies, typically 1 MHz. At microwave frequencies, the dielectric susceptibility of silicon is much larger than the conductivity of ν or π material; thus, the capacitance is effectively equal to the minimum capacitance for all values of reverse bias, as is shown in the following discussion of dielectric relaxation.

3. Capacitance Measurements and Dielectric Relaxation

If the capacitance of a PIN diode which does not punch through at zero bias is measured at zero bias, a larger value of capacitance will be measured at a low frequency (such as 1 MHz) than would be measured at microwave frequencies (such as with a slotted line measurement at 1 GHz). The reason is that silicon, in addition to being a variable conductor, also has a high dielectric constant. Therefore, its bulk differential equivalent circuit appears as a parallel combination of conductance and capacitance. The relative current division between these two equivalent circuit parameters varies with the frequency of the applied signal, higher frequency currents being carried mostly by the capacitive path.

To illustrate this point, consider Figure 11-3 which shows a PIN diode below punchthrough. The portions of the P+ and the I regions which are depleted represent the depletion zone, or "swept region." The remainder of the I region is "unswept" and can be modelled, as shown in Figure 11-3(c), as a parallel resistance-capacitance circuit, represented by the equivalent circuits elements, C_{US} and R_{US}.

The division of current through C_{US} and R_{US} depends upon the ratio of the susceptance of C_{US} to the conductance ($1/R_{US}$). This ratio in turn depends on the dielectric constant of silicon to its bulk resistivity. The frequency at which the current division between these two elements is equal (i.e., when the susceptance is equal to the conductance) is defined as the *dielectric relaxation frequency*, f_R, of the material.

When the operating frequency, f, is equal to or greater than 3 f_R, the total capacitance represented by the series combination of C_{SW} and C_{US} is approximately equal to C_J (within 10%), the parallel plate capacitance of the totally depleted I region. This value corresponds to the minimum capacity C_{MIN} measured beyond punchthrough at low frequency.

This point is a major one in the practical characterization of PIN diodes intended for microwave switching applications. It means that practical measurements of the capacitance of a PIN junction can be made at 1 MHz, and the values so attained will represent a good approximation to the actual capacitance applicable at microwave frequencies. This test only requires that sufficient bias voltage is used during the low frequency measurement to insure that the I region is fully depleted. A check to determine whether the I region is in fact fully depleted can be made simply by plotting the C(V) characteristic for a few representative diodes from the production lot to determine at what minimum bias voltage the measured capacitance reaches what is essentially its minimum value.

The remaining required quantity to determine the applicability of the low frequency C_{MIN} as a representation for the microwave capacitance, C_J, is an estimate of the relaxation frequency for the I region of the diodes being measured. High purity silicon material used to make PIN diodes typically has resistivity in the range of 500-10,000 Ω-cm prior to the diffusion and/or epitaxial growth steps used to achieve the low resistivity P+ and N+ regions. However, after the high temperature processing needed to realize these regions, the resistivity of the I region is always less than that of the starting crystal. Typical values for I region resistivity are in the range of 100-1000 Ω-cm. The dielectric relaxation frequency for the unswept portion of the I region can be written in terms of the equivalent circuit parameters, directly from the definition which

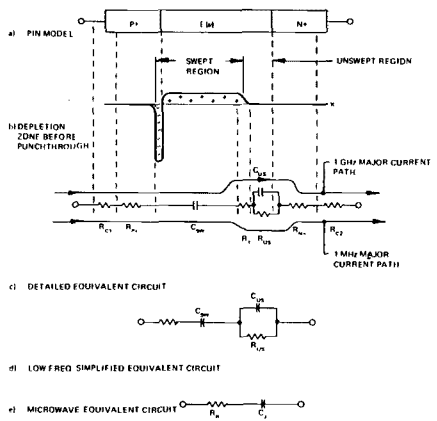

Figure II-3 Reverse Bias PIN Equivalent Circuit

requires that the conductance and capacitive susceptance be equal at f_R. The result is

$$f_R = \frac{1}{2\pi R_{US} C_{US}} \tag{II-1}$$

In turn, the specific values for R_{US} and C_{US} can be written in terms of the length, L, and the area, A, of this unswept region together with the bulk resistivity, ρ, and the absolute dielectric constant, $\epsilon_0\epsilon_R$, as follows

$$R_{US} = \frac{\rho L}{A} \tag{II-2}$$

$$C_{US} = \frac{\epsilon_0 \epsilon_R A}{L} \tag{II-3}$$

Substituting these expressions into Equation (II-1) together with the value $\epsilon_R = 11.8$ for silicon yields Equation (II-4), which gives the dielectric relaxation frequency directly in GHz when the resistivity, ρ, is known.

$$f_R = \frac{1}{2\pi \epsilon_0 \epsilon_R \rho}$$

$$f_R = \frac{153}{\rho(\text{ohm-centimeters})} \quad \text{(gigahertz)} \tag{II-4}$$

This expression is shown graphically in Figure II-4.

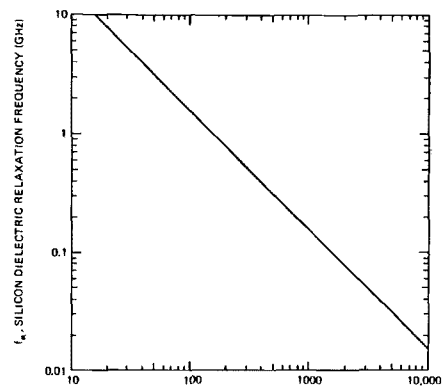

Figure II-4 Dielectric Relaxation Frequency in Silicon of Various Resistivities

Strictly speaking, since the final resistivity of the I layer of a practical diode depends upon the actual processing steps used to fabricate the diode, one could not know beforehand what dielectric relaxation frequency would apply for a particular diode unless a method for determining the magnitude of ρ as realized in a final device were available. Usually a PIN diode has an I layer resistivity of at least 100 Ω-cm, which corresponds to f_R = 1.53 GHz. Thus for operating frequencies of 5 GHz or more the simplified equivalent circuit in Figure II-3(e) can nearly always be applied.

An experimental method does exist for the determination of I layer resistivity through the measurement of the punchthrough voltage and knowledge of the I layer width, which usually is known with reasonable accuracy by the diode manufacturer. To make the calculation, Equation I-10 is solved for V_{PT} at which the depletion layer is equal to the I region width, W. Recognizing that for a PIN the impurity concentration of the N+ contact, N_A, is much larger than the impurity concentration in the I region, N_D, the result becomes

$$V_{PT} = \frac{eN_D W^2}{2\epsilon_0 \epsilon_R} \tag{II-5}$$

But the resistivity of the I region is related to the donor impurity density according to

$$\rho = \frac{1}{N_D e \mu_N} \tag{II-6}$$

where μ_N is the *electron mobility* (i.e., the effective drift velocity of electrons in the I region per unit applied electric field) and e is the charge of a single electron. Substituting this result in Equation (II-5) gives

$$\rho = \frac{W^2}{2V_{PT}\epsilon_0 \epsilon_R \mu_N} \tag{II-7}$$

$$\rho = \frac{(2.4 \times 10^8) W^2}{V_{PT}} \text{(ohm-centimeters)}$$

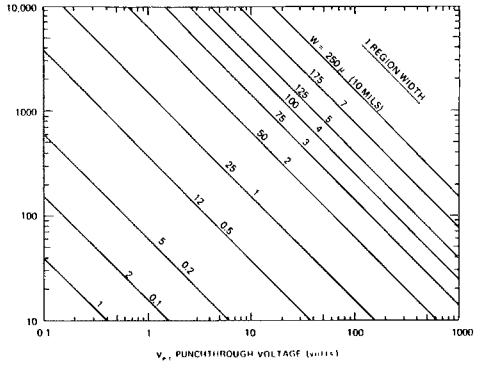

Figure II-5 Punchthrough Voltage vs. I Region Resistivity for Various I Region Widths

where ϵ_R = 11.8 (silicon)

μ_N = 2000 (centimeters²/volt-second)*

W = I region width (centimeters)

V_{PT} = punchthrough voltage (volts)

Thus, for example, if a particular diode having an I region width of 0.0025 cm (1 mil) is found to have a punchthrough voltage of 10 V, the resultant average resistivity is 150 Ω-cm. Equation (II-7) is shown graphically in Figure II-5 for various values of I region width, W.

B. Microwave Equivalent Circuit

1. Charge Control Model

Transit Time Limit of the I-V Law

In Chapter I the I-V characteristic for a PN junction was given (Equation (I-1)). The same characteristic applies for the PIN *at*

*This mobility value is representative for electrons in high resistivity N type silicon, as shown in Figure II-8. Thus, this method of I region width determination is limited by the accuracy with which mobility can be estimated.

low frequencies, for which the RF period is long compared with the *transit time* of an electron or hole across the I region.

The discussion to follow using a simple carrier transit time model is only approximate. Real diodes have more complex carrier flow, which is non uniform, subject to applied voltages (i.e., nonlinear), and so forth. The approximation is useful, as it permits estimates of frequency behavior and switching speed. The transition between low and high frequency behavior occurs when this transit time is equal to the RF period. To estimate the transit time, recall that the injection of carriers into the depletion zone occurs under forward bias by diffusion. That is, once forward bias is applied it reduces the magnitude of the built-in junction potential, causing holes to diffuse from the P to the N region and electrons to diffuse in the opposite direction.

The mechanics of this diffusion charge transport are described by *diffusion constants* for holes and electrons, D_P and D_N respectively. Diffusion, being the flow of carriers from a region of high to lower density, is described in terms of a current density proportional to the spatial gradient of charge density according to Equations (II-8) and (II-9).

$$\text{(For holes)} \quad \vec{J}_P = -eD_P(\nabla p) \tag{II-8}$$

$$\text{(For electrons)} \quad \vec{J}_N = -eD_N(\nabla n) \tag{II-9}$$

where

J = current density

e = unit charge *magnitude* = ($+1.6 \times 10^{-19}$ coulomb)

$D_{P,N}$ = diffusion constants for holes and electrons respectively

∇p = spatial gradient of hole density

∇n = spatial gradient of electron density

To illustrate diffusion, let us estimate the approximate *transit time* for holes, the slower moving carrier, across the depletion zone of a PN junction of width W. A one dimensional analysis is used, and Equation (II-8) becomes

$$J_P = -eD_P \frac{dp}{dx} \tag{II-10}$$

The minus sign is required (D is defined as a positive constant) since current flow is opposite to the direction of increasing charge density. Figure II-6 shows a simplified model of the PIN and majority carrier profiles. The gradient dp/dx is abrupt at the P/I interface and an exact analysis would require an analytic representation of p(x). However, as an approximation, we use the *average gradient of the hole density across the I region*, or

$$\frac{dp}{dx} \approx \frac{P_P}{W}$$

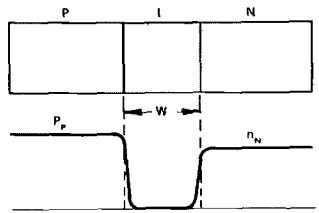

Figure II-6 Depletion Zone Model Used to Estimate Transit Time Frequency

Equation (II-10) then becomes

$$J_P = P_P e v_P \approx -eD_P \frac{P_P}{W}$$

where J_P has been written explicitly using carrier velocity, v_P, and the density of carriers participating in the hole current flow. But the hole transit time, T_P equals W/v_P; therefore

$$\text{Transit Time} = T_P \approx \frac{W^2}{D_P} \tag{II-11}$$

Accordingly, we can expect that the low frequency I-V characteristic (Equation (I-1)) can no longer be used at frequencies for which the RF period is comparable to T_P. If a transition frequency, f_T, is defined for the PIN diode at which

$$f_T = \frac{1}{T_P}$$

then

$$f_T = \frac{D_P}{W^2}$$

Frequently, the mobility, μ, rather than the diffusion constant, D, is evaluated for semiconductor materials. These two constants are related according to the Einstein relationship

$$D = \mu \frac{kT}{e} \quad \text{(centimeters}^2\text{/second)} \qquad \text{(II-12)}$$

where D = diffusion constant (centimeters^2/second)

μ = mobility (average carrier drift velocity per unit applied electric field)

k = Boltzmann's Constant

T = absolute temperature (Kelvin)

At 300 K (near room temperature) $kT/e = .026$ V; thus

$$D = .026\,\mu \text{ (at 300 K)} \qquad \text{(II-13)}$$

The hole and electron mobilities vary both with impurity densities (see Figure II-7) and temperature (see Figure II-8). For the present example the hole mobility at 300 K in high resistivity silicon is about 500 cm^2/V-s and therefore

$$f_T = \frac{1300}{w^2} \text{ megahertz} \qquad \text{(II-14)}$$

where w is I region thickness in microns.

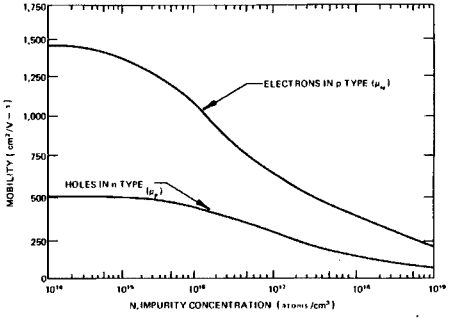

Figure II-7 Hole and Electron Mobilities (at 300 K in silicon) vs. Impurity Density (After A.B. Phillips [1])

Thus, even for a very thin base PIN diode having only a 2.5μ (0.1 mil) I region, f_T = 200 MHz. A graph showing how f_T varies with w is shown in Figure II-9. In practice, PIN diodes used for microwave switching have I region widths of 25-250 μm (1-10 mils) *and accordingly the low frequency I-V characteristic given in Equation (I-1) is useless for evaluating microwave resistance.*

I Region Charge and Carrier Lifetime

However, all of the concepts introduced so far to describe low frequency behavior are easily applied to determine the microwave resistance. We shall evaluate I region charge and use it to gauge resistance. From Figure II-9 it is evident that once charge, consisting of holes and electrons, has been injected into the I region under forward bias, *it cannot be removed in the brief duration of a half cycle of RF frequency* if that RF frequency is above a few hundred megahertz, even for the thinnest I region (or base width) diodes.

The *charge control model* for the PIN diode allows RF performance to be related to the net steady state hole and electron

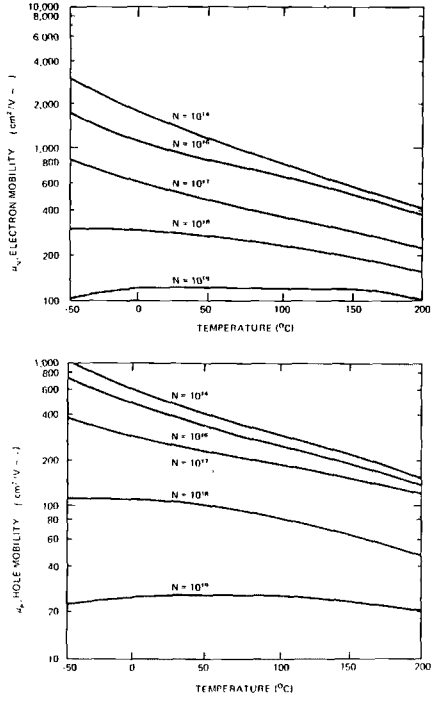

Figure II-8 Hole and Electron Mobilities vs. Temperature for Various Impurity Densities in Section (After A.B. Phillips [1])

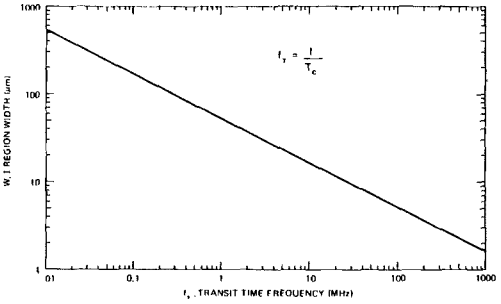

Figure II-9 I Region Width vs. Transit Time Frequency for Silicon PIN Diodes at Room Temperature

charges, Q_P and Q_N respectively, in the I region. These charges are equal to the product of the (low frequency) bias current and the respective average carrier lifetime, thus

$$Q_P = I_0 \cdot \tau_P \tag{II-15}$$

$$Q_N = I_0 \cdot \tau_N \tag{II-16}$$

That is, after the turn on transient during which the I region charge density is established, the bias current serves as a replenishment source for holes and electrons which have recombined. Referring to Figure II-10, the bias current at the P/I interface consists almost entirely of holes being injected into the I region. At the I/N interface the same bias current consists mainly of electron injection into the I region.

The longer the lifetime, the less bias current required to maintain a given charge density and, accordingly, a given microwave conductivity. Before proceeding further it is important to note that *long lifetime does not necessarily imply slow switching speed.* A properly designed driver can remove I region charge, and thereby reverse bias the diode, in a period shorter than the lifetime. Rather, long lifetime should be considered a measure of the crystalline perfection within the diode.

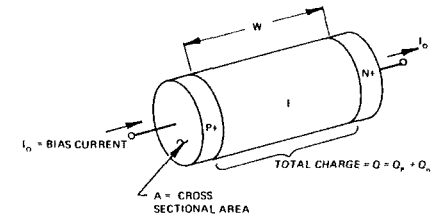

Figure II-10 Cylindrical I Region Model Used to Estimate I Region Resistance of PIN Diode

A pure intrinsic silicon crystal has a calculated carrier lifetime of 3.7 *seconds*. With impurity doping of 10^{15} cm^{-3} this figure drops to 0.11 ms. [1 (p. 80)] In actual diodes the lifetime typically ranges from 0.1 to 10 μs, orders of magnitude less than these theoretically attainable values. To appreciate the reason for this great disparity, it is necessary to review what lifetime represents.

Lifetime is proportional to the *improbability* that an electron and hole will recombine. Imperfections in the regular array of crystal atoms create energy states within the otherwise *disallowed* band gap of silicon. Such intermediate states provide a virtual energy "staircase" by which the recombination proceeds. In a very regular crystalline structure, energy must be given off in the transition of an electron from conduction to valence bands in the form of a 1.1 eV (light emitting) photon; the statistical probability of such an occurrence is low. But with crystalline irregularities, intermediate allowed energy states between these two bands permit a transition in a "staircase" of smaller energy transitions with corresponding low energy phonon (lattice vibrations) emissions, the overall probability of which is higher. Thus lifetime is reduced and recombination is enhanced by the presence of crystalline imperfections and/or impurities.

There are two categories of crystalline irregularities — boundary surfaces and bulk impurities. For a PIN diode the *I* region boundaries consisting of the highly doped P+ and N+ represent rapid recombination surfaces for carriers which diffuse into them. Likewise the peripheral surface boundary of the I region, although not to the same extent as the P+ and N+ regions, provides greater recombination probability than would be present for carriers were the silicon crystal of infinitely extended dimensions. Furthermore, from a bulk point of view, even the structure of an undoped silicon crystal is never ideal. There are stress lines and faults where the probability of electron-hole recombination increases. A doped crystal is all the more susceptible to such imperfections because of the temperature shocks, imperfect atomic fit of doping atoms within the silicon, and related crystal stress producing factors associated with diode manufacture.

This brief discussion of lifetime and its determining factors is qualitative. Even an approximate theoretical treatment of the effective lifetime for a real diode is impractical, although some bulk quantitive analytical treatments of semiconductor crystal lifetime have been made. [3] For the diode maker and user, resort must be made to experimental means by which *average* carrier lifetime can be measured. The conventional method for measuring PIN diode lifetime, τ, consists of injecting a known amount of charge, Q_0, into the I region and measuring the time, τ_S, required to extract it using a "constant" reverse bias current. [4,5] To appreciate this method, consider the equivalent circuit and charge versus time profiles shown in Figure II-11.

A forward bias current, I_F, is established and permitted to flow for a period long compared to the expected lifetime, thus storing a charge, Q_0 equal to $I_F \cdot \tau$ in the diode under test. The current supplies are chosen so that $R_R \ll R_F$. Thus, when the switch, S, closes, the diode current, I_D, reverses direction and reaches a magnitude, I_R-I_F. The stored charge is removed by this current until it is fully depleted. If the discharge period, τ_S, is short compared to the lifetime ($\tau_S \ll \tau$), then negligible recombination occurs during the turnoff and the total stored charge is recovered. In this case, $Q_0 = I_F \cdot \tau = (I_R - I_F)\tau_S$ and the lifetime is found from

$$\tau \approx \tau_S \left(\frac{I_R}{I_F} - 1\right) \quad \text{where } \tau_S \ll \tau \tag{II-17}$$

This same expression gives the approximate switching time, τ_S, of a driver which switches from forward bias, I_F, to reverse bias and has a reverse bias transient current switching capability of $I_R - I_F$.

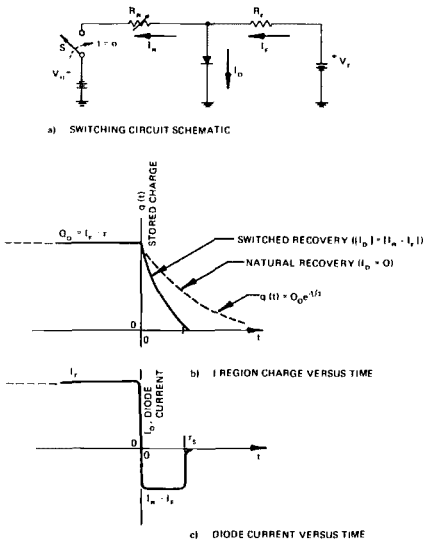

Figure II-11 Lifetime Measuring Method

amperes. Of course, in a practical driver circuit the forward current supply, I_F, would be switched off during reverse bias.

Practically, however, Equation (II-17) is not always directly useable because it may be difficult to switch the diode off in a time short compared with the lifetime. Typical PIN diode lifetimes may range from 0.1-10 μs, requiring extremely fast switches to satisfy the requirements that τ_S be small, say one-tenth, of the expected value of τ. To overcome this problem, a test setup is

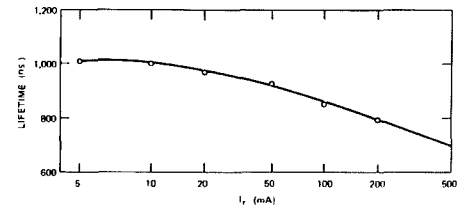

Figure II-12 Typical Variation of PIN Lifetime with Forward Current (After Ciccolella, Johnston, and DeLoach [6 (p. 289)])

made whereby the switching time can be adjusted. In the circuit of Figure II-11, R_R is made variable. The ratio I_R/I_F is adjusted so that $\tau_S = \tau$; the applicable condition is determined by analysis as follows.

If, at t = 0, I_F were turned off, the initial charge, Q_0 would decay at a rate proportional to the product of the instantaneous charge magnitude in the I region and the recombinate rate, 1/r. Actually lifetime is somewhat dependent on the bias current level; a typical variation of PIN lifetime is shown in Figure II-12 [6] for a range of bias currents commonly used. Conventionally this variation of lifetime is ignored, not because it is insignificant, but because its inclusion would not permit the simple analysis which follows. Which is not to say that the analysis isn't useful. Common practice is to apply it, but one should be aware of its limitations.

With the constant lifetime assumption, suppose that the "driver" described in Figure II-11 provides no charge extraction current. Then for $t > 0$, the expression describing the instantaneous rate of charge (dq/dt) of charge in the I region, q, is

$$\frac{dq}{dt} = -\frac{q}{\tau} \quad (t > 0) \tag{II-18}$$

The solution of this differential equation is

$$q = Q_0 e^{-t/\tau} \tag{II-19}$$

This equation shows the "natural recovery" curve in Figure II-11(b) and demonstrates the definition of lifetime as τ, the time constant of charge decay. In time $t = \tau$, q decays to 1/e or about 40% of its initial value. However, to make a practical measurement it is necessary to have a measurable quantity; this requirement is most easily fulfilled by providing a reverse current during recovery. Since the reverse current also removes charge from the I region, its effect must be included in the charge defining equation. Equation (II-18) then becomes

$$\frac{dq}{dt} = \frac{-q}{\tau} + I_D \tag{II-20}$$

This expression is called the *continuity equation* for stored charge; the name underlies the fact that stored charge is neither created nor destroyed instantaneously, but rather has time continuity. This equation is general and applies for charge building with I_D positive, as well as for recovery when the diode bias current direction is reversed and I_D is negative. The solution, which can be verified by substitution into Equation (II-20), is

$$q = Q_0 e^{-t/\tau} + I_D \tau \tag{II-21}$$

Imposing the condition that the stored charge be depleted in time $t = \tau$, as shown graphically in Figure II-11(b), and noting that $Q_0 = I_F \tau$ and that $I_D = -(I_R - I_F)$, Equation (II-21) gives

$$\left| \frac{I_R}{I_F} \right| = e^{-1} + 1 \approx 1.4 \tag{II-22}$$

as the test condition under which $q = 0$ at $t = \tau_S = \tau$, permitting a convenient direct measurement. In practice, I_R and I_F can be monitored by connecting an oscilloscope across a small resistance in series with the diode under test. Switch S is realized using a pulse generator with repetition rate adjusted to permit the application of forward current, I_F, for a time which is long compared to the lifetime, τ, in order that the steady state charge, Q_0 equal to $I_F \tau$, is established before the recovery process is measured. A practical description of lifetime and switching speed measurements is given by McDade and Schiavone [7].

The Charge Control Model and Microwave Currents

We have just seen that, from transit time considerations, the PIN I region conductivity cannot follow a microwave signal because the diffusion of charge carriers isn't rapid enough to traverse the I region within the half period of an RF cycle. Moreover, from the preceding discussion of carrier lifetime it is clear that once charge is injected into the I region it resides there for 0.1-10 μs — the lower limit of which is even long compared to the 0.005 μs half period of, say, a 1 GHz signal. These two facts taken together indicate that the resistance behavior of the PIN at microwave frequencies can be described in terms of the charge present in the I region, q.

To illustrate this point, consider the diode I-V characteristic with superimposed RF excitations, as shown in Figure II-13. The I-V law shown is typical for a high voltage PIN. Under a forward bias current of 100 mA the I region becomes sufficiently conductive that its microwave impedance drops below 1 ohm of resistance (as we describe in the next section). If a microwave current having, say, 50 A peak amplitude (500 times the bias current) is then passed through the diode, the diode is found to remain in the low impedance condition despite the large "negative-going" half cycle of the RF waveform. The reason for this linear operation even under high RF current magnitudes is clear when the total charge movement produced by the RF signal is considered. Assuming a lifetime of 5 μs, typical of a high voltage PIN, the 100 mA bias results in a stored charge of 0.5 μC. However, during the negative-going portion of a 1 GHz sinusoid, the total charge movement is less than 0.025 μC, not even a tenth of the stored charge. This example epitomizes the charge control viewpoint that *it is the total stored charge produced by a bias which determines I region resistance rather than the instantaneous magnitude of an RF current.*

*Ryder** has likened the bias level on a PIN diode to "large signal" and the RF as the "small ac component," with respect to the amount of charge stored or removed from the I region. From the above example, the value of the charge control viewpoint is evident.

*R. Ryder (Bell Telephone Laboratories; Murray Hill, New Jersey) in a talk given at the NEREM Conference in Boston, circa 1970.

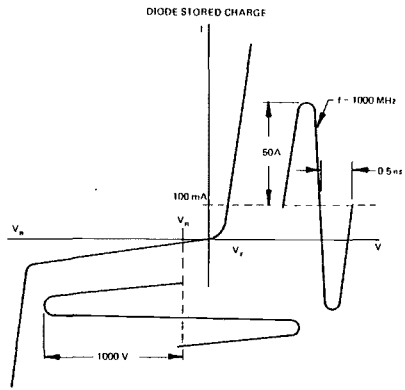

Figure II-13 Example Comparing Charge Stored by Bias to Charge Movement Due to High Level Microwave Signal

Under reverse bias, a relatively small voltage, about -100 V, is sufficient to hold off conduction of the diode under the application of an RF voltage whose peak voltage amplitude is as large as 1,000 V. Again, the brief duration of the half-period of the RF cycle is not sufficient to cause appreciable modulation of the I region of the diode, and the diode appears as a high impedance even with this large voltage magnitude applied.

One might ask why any reverse bias is necessary at all if the diode is nearly non-conducting at zero bias. First, reverse bias fully depletes the I region and its boundaries of charge. Thus, the diode has a higher microwave Q with reverse bias. Second, the role of a reverse bias is to maintain an average field which tends to prevent the accumulation of significant amounts of charge in the I region. The presence of excessive charge in the space, under high RF fields, can produce impact ionization, with a "runaway" current rise and resultant diode destruction. Nevertheless, under large RF excitation, impact ionization effects are often observed, resulting in a *pulse leakage current*, since it occurs only under the combined action of RF and reverse bias excitation. It is necessary that the driver circuit have *sufficiently low impedance* to be capable of providing this pulse leakage current (usually 1-5 mA) in a high power control device without causing an appreciable drop in the bias voltage supplied, if destructive diode conduction in the reverse bias state with high RF applied voltage is to be avoided.

2. Forward Biased I Region Resistance

Having demonstrated the suitability of the charge control approach for determining microwave properties, let us use it to calculate the conductivity and resistance of the I region under forward bias.

Conductivity, σ, is a bulk property equal to the ratio of current density, J, to applied electric field strength, E

$$\sigma = \frac{J}{E} \tag{II-23}$$

But J is the directed average rate of flow of electric charge. In terms of I region holes and electrons

$$\sigma = \frac{J}{E} = e\left(\frac{v_p \cdot p}{E} + \frac{v_N \cdot n}{E}\right) \tag{II-24}$$

Also, by definition, *mobility*, μ, is the average carrier velocity per unit of applied electric field, thus

$$\sigma = e(\mu_P p + \mu_N n) \tag{II-25}$$

where

$e = +1.6 \times 10^{-19}$ coulomb = magnitude of electron's charge

$\mu_{P,N}$ = mobility of holes and electrons respectively

p, n = respective injected hole and electron densities in I region

The formula for the resistance of a cylindrical conductor of electrical conductivity, σ, length W along the current path, and cross sectional area A is [9]

$$R = \frac{W}{\sigma A} \tag{II-26}$$

Using the dimensional notation of Figure II-10, the I region resistance is then

$$R_I = \frac{W}{eA(\mu_P p + \mu_N n)} \tag{II-27}$$

Three main assumptions* have been made in this derivation of R_I:

1) The I region as a whole is electrically neutral.
2) The bias current, I_0, injects holes and electrons which *recombine with each other in the I region*; the limitations of this assumption are discussed later.
3) The carrier lifetime is sufficiently long that both the holes and electrons are uniformly distributed within the I region. Another way of stating this point is that the average hole and electron diffusion lengths, L_P and L_N, are much longer than the I region width, W. This condition is usually valid for well designed PIN diodes and can always be verified by using the relation for diffusion length given below

$$L = \sqrt{D_{AP}\tau} \tag{II-28}$$

where

D_{AP} = ambipolar diffusion constant = $2D_P D_N/(D_P + D_N)$

τ = lifetime within the I region

In silicon, D_{AP} has an effective average value for holes and electrons, the *ambipolar diffusion constant*, of 15.6 cm^2/s [8]. Thus

$$L = 40\sqrt{\tau\ (\text{microseconds})}\ \ (\text{microns})$$
$$L = 1.7\sqrt{\tau\ (\text{microseconds})}\ \ (\text{mils}) \tag{II-29}$$

For example, if the bulk lifetime is 10 μs the diffusion length is about 133 μ (5 mils).*

Under these combined assumptions, it follows that the injected hole and electron densities are equal and uniform

$$p = n \tag{II-30}$$

and, furthermore, since they recombine with one another directly

$$\tau_P = \tau_N \tag{II-31}$$

Then

$$R_I = \frac{W}{2e\,A\,\mu_{AP}\,p} \tag{II-32}$$

where $\mu_{AP} = 2\mu_P\mu_N/(\mu_P + \mu_N)$, 610 cm^2/V-s in silicon [8], is the *ambipolar mobility*, i.e., the effective average of the hole and electron mobilities. But the injected charge is directly proportional to the bias current.

$$Q_P = epAW = I_0\tau \tag{II-33}$$

Combining the last two equations gives

$$R_I = \frac{W^2}{2\mu_{AP}\tau I_0} \tag{II-34}$$

This expression is applied frequently. We note from it that R_I is theoretically independent of I region area, being proportional to the square of I region width and varying inversely with mobility, lifetime, and bias current. However, care must be taken in the application of Equation (II-34) to practical situations. In particular, the following generalizations should be qualified:

1) *Holding all process steps the same except for varying A produces a selection of diodes with different capacitances but the same R_I for a given bias current.* This situation is true only if

*Fletcher, Neville H.: "The High Current Limit for Semiconductor Junction Devices," *Proceedings of the IRE, Vol. 45*, pp. 862-872, June 1957.

*For an analysis of the case where this assumption is not made, see Leenov's paper, Reference 8.

τ remains constant; but generally, τ decreases with a decrease in A, since I region carriers are then nearer to the periphery where recombination can occur more rapidly.

2) *R_I decreases as $(1/I_0)$.* Again, this statement holds true only so long as τ remains constant. However, as I_0 increases, carrier density increases, and the recombination probability increases, decreasing τ. Furthermore, a saturation is reached when p and n increase sufficiently that substantial injection (holes into the N+ region and electrons into the P+ region) becomes significant, in violation of the second assumption used to derive Equation (II-34). Put simply, if there are high densities of electrons and holes in the I region, their chance for recombining increases, decreasing the average lifetime, τ.
3) *Above the transit time frequency, R_I is essentially independent of frequency.* This stipulation is only approximately true for most microwave PIN applications. Skin effect causes both the contact and I region resistances to increase somewhat with frequency.

Despite these limitations, Equation (II-34) is very useful and is typically invoked to estimate I region resistance at microwave frequencies. For example, consider a PIN with a 100 μ (4 mil) I region and a 5 μs lifetime operated with 100 mA bias current.

Using $\mu \approx 610$ cm^2/V-s

$$R_I = \frac{10^{-4}\ \text{centimeter}^2}{(2)(0.1\ \text{ampere})(5 \times 10^{-6}\ \text{second})(610\ \text{centimeters}^2/\text{volt-second})}$$

$$= 0.16\ \text{ohm} \qquad \text{(II-35)}$$

This result is in reasonable agreement with the measured value of 0.3 Ω for a 1.56 mm (61 mil) diameter*, when one considers that the measured value includes resistive contributions of the ohmic contacts as well as those of the P+ and N+ regions. Furthermore, the lifetime at 100 mA is likely to be less than the 5 μs value which is measured at 10 mA – an additional factor contributory to a higher measured resistance than that calculated.

Using this example let us examine the role of skin effect in the forward biased I region. Using the parameters of the above example and solving Equation (II-26) gives $\sigma = 3\ (\Omega\text{-cm})^{-1}$. The skin depth, δ, in a conductor is given by [9]

$$\delta = \frac{1}{\sqrt{\pi f \mu_0 \sigma}} \qquad \text{(II-36)}$$

where f = operating frequency (hertz)

$\mu_0 = 4\pi \times 10^{-9}$ henry/centimeter = free space permeability

σ = conductivity (ohm-centimeters)$^{-1}$

From Equation (II-36), the skin depth for $\sigma = 3\ (\Omega\text{-cm})^{-1}$ at 1 GHz is 0.09 cm, about equal to the diode radius. This diode example has a junction capacitance of about 2 picofarads and would not usually be used at frequencies much above 1 GHz. At higher frequencies a lower capacitance, and hence reduced diameter, would be employed. Thus, it can be seen I region* skin effect usually has but a moderate effect in PIN control devices in the 0.1 to 10 GHz frequency range.

Before leaving the subject of I region conductivity it is interesting to note what level of carrier density, p, was injected into the I region of this sample diode to produce $R_I = 0.16\ \Omega$. An estimate can be made using Equation (II-32) and $\mu \approx 610$ cm^2/V-s, thus

$$p = \frac{W}{2eA\mu R_I} = 1.7 \times 10^{16}/\text{cubic centimeter} \qquad \text{(II-37)}$$

Since there is an approximately equal electron density, n, in the I region, the total free carrier density required to produce $R_I = 0.16\ \Omega$ is 3.4×10^{16}/cm^3. Recalling that the atom density is about 10^{23}/cm^3, this figure represents *less than one carrier per million atoms.* It is therefore easy to see why the skin depth, so significant with metallic conductors at microwave frequencies, has only a moderate effect even under "high injection" levels in the I region of the PIN diode.

3. R_R and C_J Reverse Biased Circuit Model

Under reverse bias the I region is depleted of carriers and the PIN appears as an essentially constant capacitance to a microwave signal. The presence of dissipative losses can be taken into account by either a series or parallel resistance element in the equivalent circuit. In a well-made PIN, the I region has sufficiently high resistivity that most of the dissipation under low RF power conditions occurs in the ohmic contacts made to the diode and in the resistances of the P+ and N+ regions. Accordingly, a fixed series resistance, R_R, used to represent these losses can be expected to offer an equivalent circuit model which is applicable over a broader

*See data for the MA-47891 PIN diode in Table III-1, pp. 94-95.

*Skin resistance may be more important in the P and N regions and in the leads attached to them because it affects how the currents enter the I region.

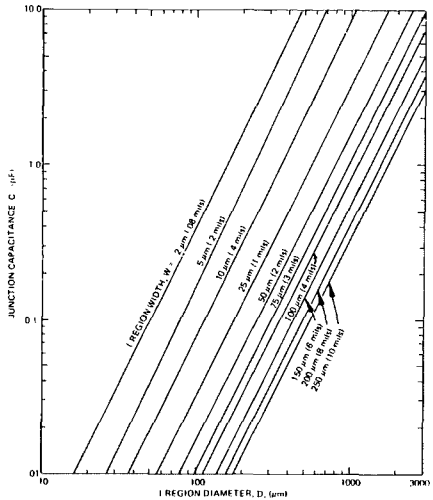
JUNCTION CAPACITANCE C (pF)
I REGION DIAMETER, D, (μm)
I REGION WIDTH, W = 2 μm (.08 mils)
5 μm (.2 mils)
10 μm (.4 mils)
25 μm (1 mils)
50 μm (2 mils)
75 μm (3 mils)
100 μm (4 mils)
150 μm (6 mils)
200 μm (8 mils)
250 μm (10 mils)

Figure II-14 PIN Diode C_J vs. I Region Diameter and Thickness

bandwidth than a parallel conductance. In any event, due to the ratio of diode capacitive reactance to practical RF circuit impedances, the dissipative losses of the PIN under reverse bias are usually much smaller than those under forward bias; thus, the choice of series or parallel R-C equivalent circuit under reverse bias usually can be made according to whichever offers greater computational convenience.

Because of the high relative dielectric constant for silicon (ϵ_R = 11.8), the fringing capacitance (in air) around the I region is relatively small and the capacitance calculated using the parallel plate capacitance formula given below provides a useful estimate of junction capacitance, C_J. Thus

$$C_J \approx \frac{\epsilon_0 \epsilon_R \pi D^2}{4W} \tag{II-38}$$

where $\epsilon_0 = 8.85 \times 10^{-14}$ farad/centimeter = free space permittivity

$\epsilon_R = 11.8$ = relative dielectric constant for silicon

D = junction diameter

W = I region thickness

For many design calculations – estimating thermal capacities, breakdown strength, and RF bandwidth – it is desirable to be able to interrelate the tradeoffs between I region dimensions (W and D) and junction capacitance (C_J). Figure II-14 shows Equation (II-38) graphically for typically available PIN I region widths.

4. Microwave Circuit Measurements and Cutoff Frequency, f_c

Equivalent Circuit Definition and f_{cs}

The microwave equivalent circuit for the unpackaged PIN diode chip to be used in this text is shown in Figure II-15. In most applications the PIN diode is used as a switch; therefore, the less capacitance, the better an "open circuit" it presents with reverse bias. The lower the resistances, R_F and R_R, the smaller the dissipative losses, and, under forward bias, the more the diode resembles a "short circuit." A figure of merit has been defined [10] to relate the PIN's switching effectiveness, termed *switching cutoff frequency*, f_{CS}. The utility of this definition is apparent later in the discussion of performance limitations.

$$f_{CS} = \frac{1}{2\pi C_J \sqrt{R_F R_R}} \tag{II-39}$$

The equivalent circuit parameters are as defined in Figure II-15. Because the additional loss at high power is treated here by a separate equivalent circuit element, G_R, the *definition of f_{CS} as used in this text is limited to microwave power levels below the onset of nonlinear dissipation.* The effect of G_R is discussed in the next section.

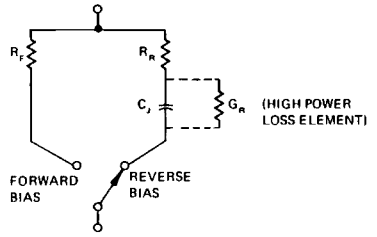

Figure II-15 PIN Diode Chip Equivalent Circuit

In principle, the values for R_F and R_R could be evaluated and f_{CS} could be specified under high power conditions. But it is not usually possible to obtain diodes characterized under high power as this task falls to the circuit designer; for this reason the separation of low and high power characterization is more consistent with actual practice.

Isolation Measurements

It was shown earlier, C_J measurements made at low frequency ($\approx$ 1 MHz) with sufficient reverse bias to deplete the I region provide a useable indication of the microwave capacitive reactance to be expected. However, the *resistances under forward, R_F, and reverse, R_R, bias conditions must always be determined by direct microwave measurements* since they include not only the inherent I region loss effects of the diode but P+ and N+ region as well as contact resistances, none of which is predictable with desirable analytic precision. Since, in most control device circuits, the greater microwave dissipation occurs under forward bias, the determination of R_F usually warrants the greater attention.

Many diode resistance measurement methods have been described. [11, 12] Ultimately the diode loss in the actual circuit of use is what is desired. For determining R_F, in either a test circuit or the actual circuit of use, the terminals where the diode is to be connected are short circuited and the loss of the circuit without diodes (i.e., the *cold circuit loss*) is measured. The additional circuit loss with diodes installed can then be attributed to the diodes themselves and, if the RF currents through the diodes can be estimated, the equivalent circuit parameters can be determined. Of course, by this time the insertion loss of the circuit under test is known and the value of knowledge of the diode equivalent circuit parameters is only of use in future design applications. Nevertheless, such direct evaluation in the circuit of end use is often required especially where diodes are circuit mounted in chip or beam lead configurations, requiring permanent bonding into the circuit to make the adequate ohmic contact necessary for accurate resistance determinations.

The two most common methods used to characterize PIN diodes, outside of the circuit of end use, are the *isolation* and *reflection* (or "slotted line") measurements.

To make an isolation measurement, the diode is used to interrupt a transmission line. When the diode is mounted in shunt with the line (Figure II-16), this method provides a sensitive measurement of the forward resistance, R_F. The isolation produced by a line shunting admittance Y is (the derivation is in Chapter V)

$$\text{Isolation} = \frac{P_A}{P} = \frac{V_A^2/Z_0}{V_L^2/Z_0} = |1 + YZ_0/2|^2 \qquad \text{(II-40)}$$

$$= 1 + GZ_0 + \frac{G^2Z_0^2}{4} + \frac{B^2Z_0^2}{4}$$

where $Y = Z^{-1} = G + jB$

To achieve the maximum test sensitivity, any series inductance introduced when mounting the diode across a transmission line is series resonated by a tunable capacitor. For this reason the measurement is most practical in the 0.5 to 1.0 GHz frequency range. Under these conditions the net series reactance, jX, of the mounted diode is zero and Equation (II-40) reduces to

$$\text{Isolation} = 1 + \frac{Z_0}{R} + \frac{Z_0^2}{4R^2} \qquad \text{(II-41)}$$

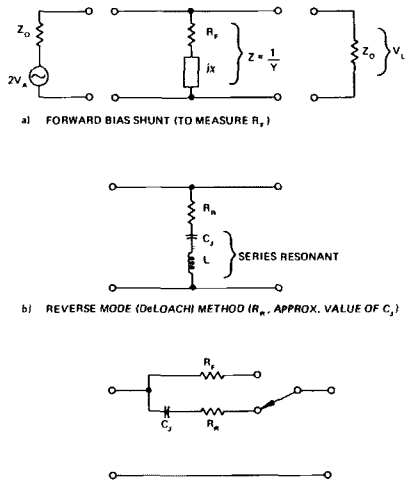

Figure II-16 Equivalent Circuits for Diode Measurements.

Thus, for example, if a series resonated diode having forward resistance of 1 Ω shunts a 50 Ω line, the normalized conductance, GZ_0 equals $Z_0 R_F = 50$. The resulting isolation equals 676, or approximately 28 dB. The resistance limited isolation described by Equation (II-41) is encountered often in both diode measurement and SPST switch design. For convenient reference it is shown graphically in Figure II-17.

There are some fine points to be considered in performing this measurement. First, if the diode is mounted in a package, the

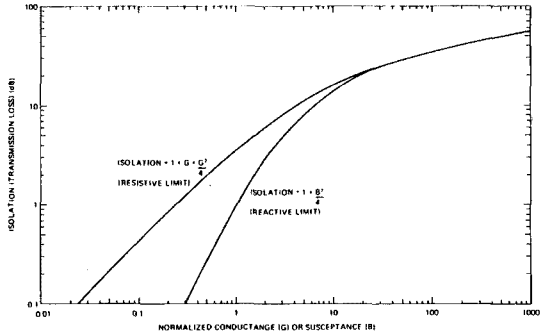

Figure II-17 Isolation of Line Shunting G or B

package capacitance transforms the effective resistance of the diode. This effect is usually negligible in the 0.5-1.0 GHz frequency band. Second, the circuitry used must not have significant leakage paths whereby power can reach the load from the generator by alternate paths such as higher order waveguide modes, fringing electric fields and so forth. This condition is readily tested by measuring isolation with the diode replaced by a short circuit of dimensions similar to the diode. Apart from ensuring that the leakage through the device is within acceptable limits, the isolation value so obtained gives an indication of the circuit *contact resistance. It is common practice to subtract contact resistance when quoting diode resistance.*

An interesting variation of the shunt mounted isolation measurement occurs when C_J series resonates with the mounted inductance of the diode (Figure II-16(b)). Then the diode shorts the transmission line under *reverse bias* and the isolation is a measure of R_R. From the isolation bandwidth an estimate of C_J is possible. This technique is usually used in waveguide at high frequencies, 5-15 GHz, to effect resonance with C_J. Switches built this way are often called *reverse mode*; the measurement technique is called the DeLoach method. [11] The reverse mode switching circuit is

important for duplexer and radar receiver protector designs where isolation in the zero biased diode state is required, as well as in other *fail safe* applications where it is desirable that, should there be a failure of the driver to bias the diode, the high reflection state of the diode switch is obtained.

If the diode is mounted in series with the line (Figure II-16(c)) the high isolation condition gives a measurement of capacitive reactance, X_C, equal to $-(2\pi f C_J)^{-1}$, and hence, C_J. For an impedance $Z = R + jX$ in series with a line of characteristic impedance, $Z_0 = 1/Y_0$, the isolation, by duality, is given by the dual of Equation (II-41)

$$\text{Isolation} = \left|1 + \frac{ZY_0}{2}\right|^2 = 1 + RY_0 + \frac{(RY_0)^2}{4} + \frac{(XY_0)^2}{4} \qquad \text{(II-43)}$$

If $|X_C| > 15\ R_R$, as is almost always the case, the RY_0 terms in Equation (II-43) can be ignored with an error of less than 1%, and the reactance versus isolation can be read directly from the reactance dominated characteristic curve shown in Figure II-17. This method is especially useful for measuring the circuit mounted capacitance of low capacitance devices such as beam lead diodes.

Series mounted diodes require special equivalent circuit treatment. Figure II-18 shows schematically the electric field contours of a capacitor representing a reverse biased diode both within and without a series coaxial line mounting. Measured in free space, all E field lines terminate on the diode terminals directly, and a capacitance, C_0, is measured. When mounted in the coax line, however, some E field lines intercept the outer conductor. The effect is that the effective series capacitance, C, is less than C_0. An additional shunt capacitance, C_2, appears, but in most cases the effect of C_2 on the transmission line is negligble, since it serves to replace the distributed capacitance of the section of center conductor removed to install the diode. However, the fact that the mounted series capacitance, C_1, is less than the capacitance associated with the diode, C_0, means that a higher isolation is obtained in a switching circuit (generally a benefit). Moreover, in a phase shifter circuit a different phase shift than that anticipated will be obtained if this effect is overlooked.

The accuracy of the series measurement can be related to the loss and isolation measurement accuracies. Typically the series isolation

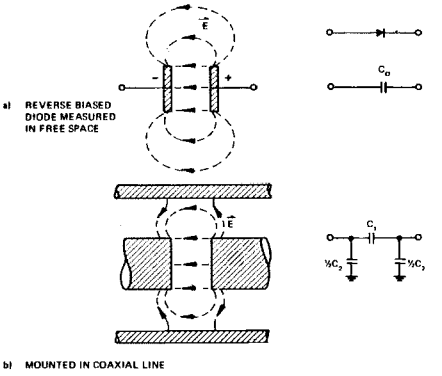

Figure II-18 Change of Effective Series Capacitance with Circuit Mounting

(or loss) measurement can be made to within an accuracy of ±0.1 dB for losses below 3 dB, and ±0.3-0.5 dB for isolation values from 10-40 dB. Thus, R_F can be determined to an accuracy of about ±2%; X_C, to about ±5% of the magnitude of Z_0. For most PIN diodes operated at sufficient forward bias to saturate the I region, $R_F < 1\ \Omega$; this measurement method would require impractically low Z_0 for meaningful measurements. However, for R_F measurements at low bias levels or with beam lead diodes wherein R_F = 2-10 Ω, the measurement is very practical using standard 50 Ω line. For example, a beam lead diode having $R_F = 5\ \Omega$ produces a 10% insertion loss of about 0.5 dB. The same diode, having C_J = 0.03 pF, has a reactance of -j795 Ω at 10 GHz, yielding, in the same test fixture, isolation under reverse bias at 10 GHz of 24 dB.

*Reflection Measurements**

Most of the principles described for isolation measurements are likewise applicable to reflection measurements wherein the diode is used to terminate the line (Figure II-19); the reflection coefficient (Γ equal to $\rho e^{j\phi}$) measurement is used to deduce diode parameters. Other things being equal, the sensitivity of this measurement method is about four times that of the matched load method described previously in the determination of R_F and R_R for a given line impedance and dissipation; therefore, it is used for most standard diode characterizations. Diode reactances under both forward and reverse bias can be determined from the reflection coefficient argument.

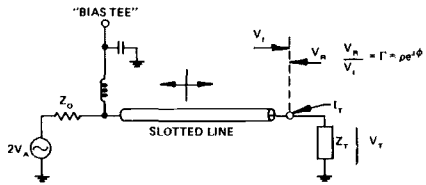

Figure II-19 Reflection Measurement Equivalent Circuit

The added sensitivity arises because, if the magnitude of Γ_L is either high or low compared to Z_0, the current (I_L) or voltage (V_L) at the end of the line is nearly double the value (V_A/Z_0 or V_A, respectively) experienced under matched load ($Z_L = Z_0$) conditions; the relative power absorbed in the diode consequently increases fourfold. For both a load impedance $Z_L = R_L + jX_L$ and a line with Z_0 characteristic impedance, the reflection coefficient at the load position is [13, 14]

$$\Gamma = \rho e^{j\phi} = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{(R_L - Z_0) + jX_L}{(R_L + Z_0) + jX_L} \qquad \text{(II-44(a))}$$

$$\phi = \tan^{-1}\left(\frac{X_L}{R_L - Z_0}\right) - \tan^{-1}\left(\frac{X_L}{R_L + Z_0}\right) \qquad \text{(II-44(b))}$$

*See Appendix J, The Smith Chart, for the development of reflection principles.

$$\rho = \sqrt{\frac{(R_L - Z_0)^2 + X_L^2}{(R_L + Z_0)^2 + X_L^2}} \qquad \text{(II-44(c))}$$

The fractional dissipation in Z_L is

$$\text{Insertion Loss} = 1 - \rho^2 = \frac{4\,R_L Z_0}{(R_L + Z_0)^2 + X_L^2} \qquad \text{(II-45)}$$

Under forward bias, using $Z_0 = 50\ \Omega$, both R_L and X_L are usually much less than Z_0. The fractional power loss is approximately equal to $4R/Z_0$. Under the same approximation, the insertion loss ratio by the series isolation measurement is approximately equal to $1 + R/Z_0$ and the *fractional loss* is approximately R/Z_0, only one fourth that of the reflection measurement. Thus, for example, with $Z_0 = 50\ \Omega$ and $R_F = 1\ \Omega$, the measured loss is about 0.4 dB with the reflection method and 0.1 dB with the isolation method, giving (with ±0.1 dB accuracy) the determination of R_F with ±0.25 Ω and ±1.0 Ω accuracies, respectively. Accordingly, when the diode is mounted in series with the line, the reflection measurement is usually employed for determining R_F.

This method is also used for determining R_R and C_J, but the calculations are less convenient than for R_F because the series reactance, X, cannot be ignored. Furthermore, the impedance transformation effects of a diode package (the package being necessary if the diode is to be conveniently mounted at the end of a slotted line) are not negligible in the reverse biased condition. For routine diode evaluation the reflection coefficient magnitude, ρ, and phase, ϕ, are measured and the exact equations relating diode C_J and R_R are solved using a computer program.* It is common practice to use a coaxial line and obtain a zero impedance reference by short circuiting the line at the leading surface of the diode package (as shown in Figure II-20). Both a phase reference ($\phi = 180°$) and a loss reference ($\rho = 1.0$) are thereby established. The packaged diode impedance, Z_L, is then evaluated by solving Equation (II-46) for Z_L

$$Z_L = R_L + jX_L = Z_0\,\frac{(1+\Gamma)}{(1-\Gamma)} = Z_0\,\frac{(1+\rho e^{j\phi})}{(1-\rho e^{j\phi})} \qquad \text{(II-46)}$$

*Computer programming for circuit evaluation is discussed in Chapter VI.

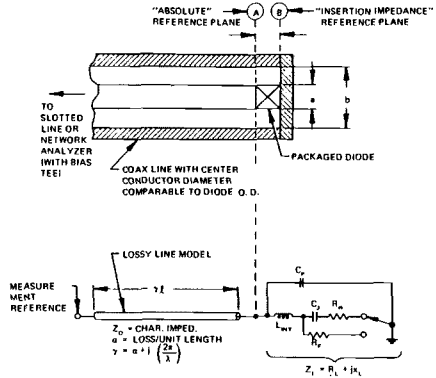

Figure II-20 Schematic and Equivalent Circuit Detail for "Slotted Line" Measurement of Packaged PIN Diode

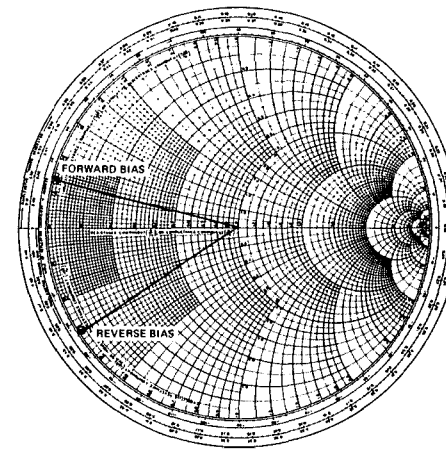

Figure II-21 Reflection Coefficients for Measurement Example

It is illustrative of the measurement method to plot the reflection coefficients obtained under forward and reverse bias on the Smith Chart. For this example, consider a PIN with C_J = 2 pF, $R_R = R_F$ = 0.3 Ω mounted in a package having C_P = 1 pF and L_{INT} = 0.3 nH. At 3 GHz the *chip* impedances are 0.3 Ω and (0.3–j26.5) Ω under forward and reverse bias; they are transformed by the package to (0.37+j6.30) Ω and (0.15–j15) Ω, respectively. When normalized to Z_0 = 50 Ω the corresponding reflection coefficients are (from Equation (II-44)) $\Gamma = 0.986/165.6°$ with forward bias and $\Gamma = 0.976/-145.8°$ with reverse bias. These results are shown graphically in Figure II-21. The proximity of the points to the Smith Chart periphery (ρ = 1.0) underscores the need for careful measurements if R_F and R_R are to be evaluated accurately.

While the application of the principles of this method is straightforward, great care must be exercised if results with useful accuracy are to be obtained. Since a single frequency measurement of Γ produces only two bits of data, ρ and ϕ, it is necessary either to have foreknowledge of the values of package *parasitics* (internal inductance, L_{INT}, and package capacitance, C_P) or to perform the reflection measurement at more than one frequency in order to solve for C_P, C_J, R_R, and R_F. In practice the former method is usually followed. C_P is first determined using an empty diode package; this result for C_P is used with an internally shorted package having a wire or strap lead similar to that to be employed with the diodes to be measured. In this respect, the eventual accuracy of evaluation of C_J and R_R is dependent upon the reproducibility of

C_P and L_{INT} and their relative reactances compared to that of C_J. Furthermore, since the point of measurement and diode reference plane are separated by a line with finite loss, the resulting *lossy line transformation* (see Chapter VI, Equation (VI-2)) must be taken into account when R_F and/or R_R are small ($< 2\%$ of Z_0) as is usually the case. This requirement necessitates a computer program to reduce the data if such measurements are to be made routinely.

Diode Inductance Measurements and Definitions

It should be noted that values measured for diode impedances depend to some extent on the test fixture – especially with inductive reactance, which can *only* be specified in terms of a return path. For example, the inductance per unit length of coaxial line having an outer conductor diameter, b, and an inner conductor diameter, a, is [9]

$$L = \frac{\mu_0}{2\pi} \ln \frac{b}{a} \tag{II-47}$$

and the characteristic impedance Z_0 is [9]

$$Z_0 = \frac{1}{2\pi} \sqrt{\frac{\mu_0}{\epsilon_0}} \ln \frac{b}{a} \tag{II-48}$$

For 50 Ω, the ratio b/a equals 2.3 for air dielectric coax. Suppose a packaged diode having 2.5 mm (0.1 in) length and effective diameter, a of 1.25 mm (0.05 in), is first measured under forward bias in a 50 Ω line having b equal to 15 mm (0.6 in); the inductance is 0.62 nH. If, however, the same measurement is performed using a smaller diameter 50 Ω coaxial line in which b equals 7.5 mm (0.3 in), the inductance is 0.45 nH.

Not only the absolute circuit dimensions but also the reference plane definition affects the inductance determination. For example, the above determination of inductance corresponds to reference plane A selection in Figure II-20. If, however, reference plane B were selected – by replacing with an equivalent length of center conductor to obtain a short circuit measurement reference – *insertion impedance* would be obtained. Insertion impedance is Z_L less the Z_S of the short circuit terminated length of the measurement line, ℓ, neglecting line loss

$$Z_S = jZ_0 \tan\left(\frac{2\pi\ell}{\lambda}\right) \tag{II-49}$$

where λ = wavelength at test frequency.

If, as is usually the case, $20\ell < \lambda$, the value of the tangent term can be replaced by its argument (within 3%). Furthermore, Z_S is an inductive reactance ($j2\pi fL_S$); for a coaxial line

$$\begin{aligned} L_S \text{ (nanohenries)} &\approx 0.0033 \cdot \ell \text{ (millimeters)} \cdot Z_0 \text{ (ohms)} \\ &\approx 0.084 \cdot \ell \text{ (inches)} \cdot Z_0 \text{ (ohms)} \end{aligned} \tag{II-50}$$

For the example cited, ℓ = 2.5 mm, L_S = 0.41 nH, and the diode respective *insertion inductance** values determined from measurements in the two line sizes is 0.21 and 0.04 nH respectively.

These examples highlight the importance, especially for inductance measurements of specifying both the measurement fixture and reference plane selection. Similar reasoning indicates that if the actual circuit of use does not duplicate these conditions – and usually it doesn't – calculations of performance sensitive to inductance will be inaccurate unless the new conditions are taken into account.

C. High RF Power Limits

1. Forward Biased Limits

Under forward bias the PIN diode chip usually has an RF resistance of 1 Ω or less. Failure of the diode in this bias state will occur if the dissipative heating (I^2R_F) is sufficient to cause the diode temperature to rise sufficiently to induce metallurgical changes. For silicon and its dopants, this point is not reached until a temperature of about 1000°C. However, the metal contacts at the silicon boundaries introduce failure mechanisms in the vicinity of 300-400°C, at which temperatures common contact metals form eutectic alloys with silicon. For example, the gold-silicon eutectic occurs at 370°C [16]. Repeated or continuous exposure of silicon to the eutectic temperature in the presence of the corresponding metal can produce conducting filaments of metal-silicon alloy, which eventually "grow" across the I region of a PIN diode, short circuiting it. This structural change of the diode crys-

*Also sometimes called *excess inductance*.

tal is the most common diode failure mechanism with heat, even with reverse breakdown induced failures, described subsequently.

Failure of a diode does not occur instantaneously when an over stress is applied unless the resulting temperature greatly exceeds 300°C, as can occur with filamentry heating produced by avalanche breakdown in the reverse bias condition. This situation is also discussed subsequently. Except for the rapid failure induced by avalanche breakdown, thermally produced failures proceed over a time period related to the ratio of the operating temperature, T, to that which causes near instantaneous burnout. Rather extensive experiments carried out on computer diodes have shown that the mean time to failure can be described by the empirical relationship [15] given by Equation (II-51)

$$t_M(T) = Ae^{+Q/kT} \qquad \text{(II-51)}$$

where $t_M(T)$ = the mean time to failure at operating temperature T

A = a constant

Q = the "activation energy" constant

k = Boltzmann's Constant

T = the average device temperature in Kelvin (= °C + 273)

This expression is called the Arrhenius Law. It can be applied when the variation of operating life with temperature is determined by *only one* failure mechanism – for example, the formation of a particular alloy of the metallization system with the silicon.

To apply this relationship, the failure temperature, T_F, is first determined for the diode type; it depends on the semiconductor material (usually silicon for a PIN) and the metallization system. Next the device is operated at a lower temperature for a period until 50% of the samples under test fail, establishing a data point along the temperature-time graph. Additional data points at different temperatures are determined to allow for averaging of experimental data. This process, called *step-stress temperature testing*, is time-consuming because data points corresponding to hundreds and thousands of operating hours are required if the failure curve is to be established with sufficient accuracy to permit meaningful extrapolation to long life operation – on the order of years.

Care must be exercised that only the common *thermal* failure mode applies throughout the step stress tests. Careful analysis, usually including sectioning of failed diodes, is required to confirm the failure mode of each diode specimen used to establish the failure curve. The resulting temperature-time data plotted on semi-log paper form a straight line, permitting extrapolation for longer periods. Figure II-22 shows a typical plot for a surface-glass passivated; mesa type, high voltage PIN diode used in a phased array application. Notice that with a 200°C junction temperature (often cited as a safe operating limit for semiconductor devices) the anticipated mean life is 1000 hours (or 0.1 years), while for 140°C the anticipated mean life is extended to 1,000,000 hours (or 114 years). Accordingly the role of operating temperature must be given careful consideration if the estimate of anticipated life is to be meaningful.

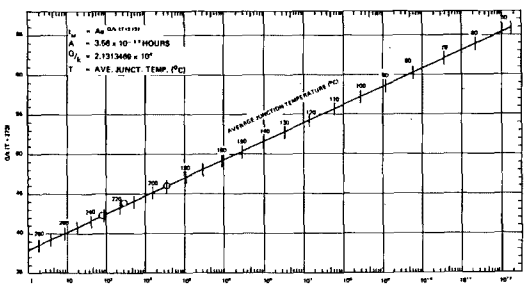

Figure II-22 PIN Life Expectancy vs. Temperature (Courtesy P. Ledger, Microwave Associates, Inc.)

2. Reverse Biased Limits

The reliability criteria apply for reverse biased operation as just discussed for forward bias. The junction temperature is again the result of ambient and RF heating. Unlike the forward biased condition, however, the fractional RF insertion loss does not remain nearly constant once the applied RF voltage has a magnitude which is comparable to either the reverse bias and/or the diode's reverse breakdown voltage. Under these conditions diode dissipation (is nonlinear and increases more rapidly than RF power, producing at times a runaway insertion loss). The onset of this rapidly increasing insertion loss nonlinearity can be used as a practical measurement that the destructive temperature has been reached in the reverse biased state, since diode failure usually occurs if the incident RF power level is increased much beyond this level. Figure II-23 shows a typical insertion loss versus RF power characteristic obtained with a reverse biased diode phase shifter. The mechanisms of reverse biased diode failure under RF voltage stress are not sufficiently evaluated for a definitive theory to be developed, largely because of the difficulty of performing such measurements, with enough samples to have adequate statistical data. Qualitively, two conditions in which I region charge is generated occur and which one predominates depends, as described in Figure II-24, upon the relative magnitudes of the peak RF voltage, V_P; the bias voltage, V_{BIAS}; and the diode breakdown voltage, V_{BD}, as described in Figure II-24.

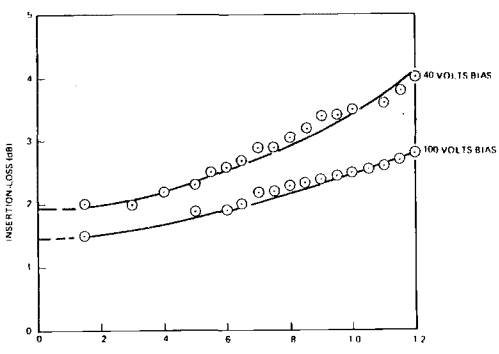

Figure II-23 Insertion Loss vs. Peak Power for a 4 Bit X-Band Phase Shifter Under Reverse Bias in All Bits (Phase Shifter Described in Chapter IX, pp. 470-475)

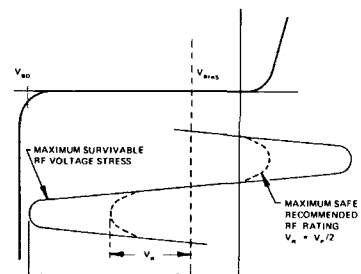

Figure II-24 Operation at High RF Voltage and Reverse Bias

The condition shown in Figure II-24 with voltage, V_P, is representative of typical operation near the failure limit. The RF voltage has a large excursion into the forward direction. Although, as has been shown earlier, the duration of this half cycle is insufficient to result in conduction by the diffusion transit (injection) of P region holes and N region electrons across the I region, *some charge* is introduced into the I region from these boundaries, and not all of it is extracted by the combined action of the reverse bias and

the negative-going half of the RF cycle before the next forward-going RF voltage excursion. However small the magnitude of the injected charge may be, it can increase multiplicatively with each succeeding RF cycle through *impact ionization*; electron-hole pair production results when mobile carriers accelerated by the high RF field strike silicon atoms in the I region lattice with sufficient energy to promote valence band electrons to the conduction band. This cause of increased insertion loss can be identified experimentally by its bias voltage dependence. Increasing the magnitude of reverse bias voltage sweeps such injected charge out of the I region more effectively and thereby extends to a higher applied RF voltage the onset of rapid insertion loss increase, which precedes what, for present purposes, is called the *injection mode* failure mechanism.

The second mechanism causing nonlinear insertion loss is the *direct impact-ionization mode*, occurring when the combined RF + bias voltage exceeds the diode bulk breakdown, i.e, $V_P + V_{BIAS} > V_{BD}$. In this case no partial injection is needed to initiate impact ionization; the requisite electron-hole pairs are obtained directly by high electric field ionization of I region silicon atoms. One might think this mechanism would be eliminated by reducing the bias voltage, since this action would reduce the combined magnitude ($V_{BIAS} + V_P$); but, in most practical cases, where the bias is 10-20% of V_{BD}, reduction of V_{BIAS} would only precipitate the injection-mode failure. An exception, of course, is when the bias is kept at half the breakdown (i.e., $V_{BIAS} = V_{BD}/2$). Then the RF waveform makes no injecting excursion into the forward direction. But for high power switching applications, a driver circuit to accomplish this end requires prohibitively high voltage transistors (500 V or more); the overall expense of the RF control circuit with driver could be more readily reduced by using a larger number of PIN diodes operated with less RF voltage stress.

Practically, the maximum sustainable RF voltage, V_P must be determined by measurement. Taking high power loss data for the diode – RF frequency, pulse length, and duty cycle of intended use – is the most direct and effective technique. In no case can $V_P + V_{BIAS}$ exceed V_{BD}, where V_{BD} is the bulk breakdown voltage of the diode.* The bias voltage is selected to be as large as is possible in a practical driver circuit (usually 10-20% of the diode's reverse bulk breakdown voltage) and the RF power level (from which the corresponding voltage, V_P, can be calculated) is set at the point at which a statistical sample of diodes have been found to undergo rapid loss increase and/or failure. Failures due to either of the two modes described are usually evidenced by a permanent short formed by a conducting filament across the I region.

Most high power switching applications use the PIN diodes in a transmissive circuit with a matched load. Accordingly, failure or removal of the load, transmission line arcing, or any mechanism which affects the load match can result in a voltage reflection and possible RF voltage enhancement at the diode. Neglecting losses in the switching circuit and diodes, this reflection voltage enhancement can double the stress on the diodes. Such a condition, even if encountered only briefly, usually precipitates diode failure. Therefore it is good practice to rate the diode at a stress level $V_R \leqslant V_P/2$ (see Figure II-24) in order for the device to be able to survive such a total reflection. Since power is proportional to the square of voltage, *PIN diode devices should be rated at one-fourth or less of the power level at which, with matched load, they would be expected to undergo near instantaneous failure.* Even if provision has been made to minimize the likelihood of a totally reflecting load, consideration should be given to the following factors before opting a power safety factor of less than 4 to 1:

1) Diode failure is not an exactly reproducible event even with PIN's made by the same process within the same lot. A 2 to 1 variation in burnout is typical for a given process. Thus, a production run of diodes may have a considerably lower (or higher) burnout than experienced with a prototype test lot.
2) Most high power tests are conducted at room temperature while practical devices usually must perform at considerably higher temperature, reducing the power safety margin that is inferred from a room temperature test.
3) High power RF testing is often of short duration, an hour or less, due to the generally limited availability of high power testing facilities. However, semiconductor devices are usually expected to have useful lifetimes of years. Derating, according to Figure II-22, is necessary to accomplish long life.
4) PIN devices operated at or below one-fourth of their burnout power are typically found to be able to survive temporary driver failures wherein the high power RF signals are applied with the diodes at zero bias.

*See Chapter III for bulk breakdown voltage evaluation of practical diodes.

Generally PIN devices to control pulsed high RF power are limited in the reverse biased state by the maximum safe rated RF voltage stress, V_R, as is seen in the circuit discussions to follow. While a device which fails to meet circuit performance expectations may cause some user disappointment, it has been the author's observation that nothing quite equals the state of dissatisfaction resulting when solid-state control devices fail catastrophically due to overrating. No doubt it is for reasons such as this one that it has been industry practice in large phased array systems to design PIN phase shifters to survive operation into a short circuit load of any phase.

Only by carefully rating these devices can the good reliability which has come to be expected, indeed often assumed without question, of solid-state control be sustained. Accordingly, the designer should adopt as a minimum a policy of both designing diode control devices to sustain operation into a short circuit of any phase and testing throughout production to insure that this level, at least statistically, is maintained for the complete population of devices built.

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Questions

1. What is the punchthrough voltage of a PIN diode having a 50μ (2 mil) I region width and I region resistivity of 300 Ω-cm?
2. What is the dielectric relaxation frequency of the PIN diode in Question 1?
3. What is the transit time of the PIN diode in Question 1?
4. If the PIN diode in Question 1 has an average carrier lifetime of $\tau = 2\ \mu s$, what is the microwave resistance of the I region, R_I, when a forward bias of 50 mA is applied?
5. For the conditions in Question 4 what is the value of R_I 1 μs, 10 μs, and 15 μs following the turn off of the forward bias? Neglect reactive effects and assume a constant lifetime of 2 μs, and that the forward bias had been on long enough to establish a steady state charge in the I region before turnoff.
6. If the diode in Question 5 has contact resistance of 0.2 Ω what isolation does it produce when it shunts a 50 Ω line with negligible inductance (SPST switch) with 50 mA bias? What is the isolation 1 μs, 10 μs, and 15 μs after the bias is turned off?

DESIGN CONSIDERATIONS FOR THE DEVELOPMENT OF INTERNALLY MATCHED FETs

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Abstract

This paper describes design considerations for the development of internally matched power GaAs FETs. Both power FET and matching circuit designs are discussed. Examples of single chip and multi-chip designs with power levels of up to 10 Watts in C-band and 2 Watts in Ku-band are presented.

1.0 INTRODUCTION

Over the last few years the challenges offered by high power FET design have been largely overlooked in favor of more glamourous projects on Monolithic Microwave Integrated Circuits (MMICs). Monolithic circuits have received a great deal of research funding and effort, and for some applications, MMICs are clearly the technology of choice, i.e., low cost satellite down converters and low power (.2 Watts) T/R modules for phased array radars; systems where the volume justifies the development costs. However, in many cases where high power is required or the volume required is low, and this is typical of microwave systems, the discrete power FET is the device of choice. For example, high power internally matched FETs are widely used in point to point microwave communications systems where they have replaced TWTAs because of superior reliability. In space, power FETs are currently used for some satellite down link applications and this use will grow as higher power, higher efficiency devices become available.

At MSC, a wide range of devices for these and other applications is under development in the 2-26 GHz range. In this paper, design considerations to optimize output power, efficiency and bandwidth will be discussed and illustrated with examples from current development projects.

2.0 POWER FET DESIGN

To achieve high power capability, a large number of gates must be connected in parallel. This can be accomplished with the simple interdigitated layout of a typical MSC FET shown in Figure 1, with such a layout comes the first problem facing a power FET designer. The FET is a three terminal device, thus any two sets of electrodes can be interconnected directly on the surface of the Gallium Arsenide (in Figure 1, the gate and drain electrode sets are connected) but the third electrode set cannot. It is this fundamental problem that has led to the wide diversity of designs throughout the industry. Some designers have elected to use air bridge or dielectric cross-

overs to interconnect the third electrode, other have used a flip chip approach as shown in Figure 2, but the technique that is now becoming most widely adopted is the use of via hole connectors as shown in Figure 3.

Via hole technology has two significant advantages. It enables the source electrode to be grounded directly through the chip, thus ensuing a minimum parasitic source inductance and it results in an optimum thermal configuration. To form via holes with high yield, the GaAs wafer must be thinned to approximately 30 microns as shown in Figure 3. This minimizes the heat conduction path through the GaAs to the integral gold plated heat sink.

Having solved the source grounding and thermal design problems, the designer is next faced with choices concerning the number of gates to interconnect the individual width and length of these gates. The gate width and length are selected based on the desired frequency of operation. It is desirable to use the maximum gate width possible at a desired frequency to reduce the number of gates required and thus minimize the overall chip size. Because of losses along the gate which increase with frequency, the gate width is limited to approximately 500 microns at 4 GHz and 100 microns at 20 GHz. Similarly, it is desirable to use the minimum gate length consistent with high yield at a given frequency and in most power FET designs, 1.0 micron is chosen for up to 10 GHz operation and 0.5 micron for above 10 GHz.

The total gate width (number of gates x gate width) is chosen to achieve the desired output power based on 0.4 Watts/mm of gate width. However, as the total gate width is increased, the input and output impedances are reduced and the device becomes progressively more difficult to match. For very high power devices, a compromise between the difficulties of matching a large single chip versus matching and combining several smaller chips have to be investigated. For 10% bandwidth applications, it is feasible to design single chip devices with output powers in the 5 Watt range with total gate widths of up to 14mm, but for broad band applications, such as octave band ECM systems, the largest feasible devices are in the 1 Watt range.

Modern process lines for power FETs are highly automated, especially in the photolithography area where cassette to cassette equipment is used for the application and development of photoresists and for mask alignment. The most critical steps in the fabrication process are concerned with the gate formation. At MSC, two different types of FETs have been developed which differ only in the details of the gate cross section. One type is designed to operate at the conventional drain bias of 8-10 Volts, the other is designed to operate at 16 Volts. High voltage operation has advantages in the areas of improved linearity for communications systems and improved

efficiency in phased array radars. At higher voltage the I^2R losses in the feed to the array are significantly reduced and the conversion losses from the typical 28 Volts of airborne and satellite systems are also reduced. Although processing yields with highly automated lines can be extremely high, especially if the definition of the 1.0 micron or 0.5 micron gate is accomplished with direct write e-beam technology, (at MSC a Philips EBPG 4 system, which alone represents an investment of $2M is used for this function), overall yields are low because power FETs must operate at high current densities and voltages near breakdown where their performance is dominated by the quality of the GaAs materials. At MSC the GaAs layers are grown by vaper-phase-epitaxy and their quality and uniformity are carefully monitored using C-V analysis and DLTS (Deep Level Transient Spectroscopy).

3.0 MATCHING CIRCUIT DESIGN

In this section, designs of matching circuits for internally matched FETs are presented. Matching of the input and output impedances of a power FET to 50 ohms requires accurate small and large signal S-parameters and device modeling. The small signal S-parameters are measured using an HP8510 Network Analyzer. A good de-embedding procedure is required to obtain accurate S-parameters. Through-Short-Delay (TSD) is one such method being used to de-embedd the S-parameter at the chip level.

For design of the output matching circuit, it is important to obtain the large signal S-parameters. An automated load-pull technique is used to obtain the large signal output impedance. This technique uses a computer-controlled mechanical double slug coaxial tuner at the output of the FET to match the output impedance of the FET under large signal conditions. Load-pull contours for output power, gain and efficiency are obtained. The large signal output impedance for optimum output power, gain and efficiency is measured using an HP8510 network analyzer. At MSC an automated load-pull system operating in 2-26 GHz band is currently being used for the development of a range of internally matched power FETs.

Touchstone and Supercompact microwave circuit design CAD programs are used to design the input and output impedance matching circuits for the FET. The choice of circuit approach, and its implementation, must be considered while designing the input and output matching networks since the overall dimensions of the matching circuits are limited by the package dimensions. At C- and X-band a 12.9mm wide package is used while at Ku-band a 9.8mm wide package is used. At 20 GHz a .248" wide open carrier is used since a package for this frequency is not available at the present time.

Figure 4 is a Smith Chart representation of the design methodology for an internally matched FET. A two section low pass

filter is used for matching the input and output impedances. Lumped element matching is used in C-band whereas distributed approach is used in Ku and K-band. A combination of lumped and distributed elements are used at X-band. Since the overall size of the matching circuit has to be small to fit the package, a high dielectric constant substrate, such as barium tetratinate with Er-38 is necessary in C-band, whereas the more conventional Alumina substrate material (Er=9.8) is used in X, Ku and K-bands. The thickness of the substrate is also a factor in determining the overall size of the input and output matching circuits. The width of the distributed microstripline is proportional to the thickness of the substrate. Use of thinner substrate reduces the overall dimension. However, loss in the circuit increases as the width of the line is reduced. Five and ten mil thick alumina substrates are used in Ku and K-band, while 5 mil thick Barium Tetratitanate substrate and 10-15 mil alumina substrates are used in C- and X-bands. The choice of substrate thickness depends on the impedance level of the FET. The input and output impedance of the FET fall with increases in output power. To obtain higher output power, larger gate peripheries and multiple chips are used. Thus, a trade-off is made between the thickness of substrate, the size of the overall matching circuit and the losses in the output matching network.

4.0 EXAMPLES OF INTERNALLY MATCHED GaAs POWER FETs

Several internally matched power FETs have been developed at MSC. 3 Watt and 10 Watt internally matched FETs operating over 3.7-4.2 GHz have been developed. Figures 5 and 6 show the variation of output power and third order intermodulation distortion (IMD_3) products as a function of input power for 3 and 10 Watt internally matched FETs, respectively. The gain and efficiency of the 3 Watt FET are 12dB and 40%. The 10 Watt internally matched FET exhibited 9dB gain and 30% efficiency.

Figure 7 shows the output power and efficiency variation as a function of input power for a high voltage internally matched FET. This FET operates at Vds = 16V and exhibited 14 Watt output power with 7.5dB gain and 29% efficiency at 5.3 GHz.

Table 1 shows the results for output power, gain and efficiency for an internally matched FET operating over 14.5-15.35 GHz band. An output power of 1 Watt with 6-7 dB gain and 20-25% efficiency has been obtained.

A 2 watt output power with 4-5 dB gain and 19% efficiency has been obtained over 17-18 GHz. Results for output power, gain, efficiency and return loss over 17-18 GHz are presented in Table 2.

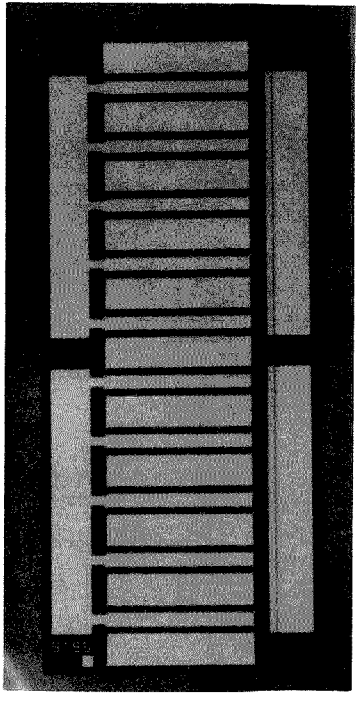
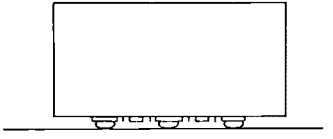


FIG. 1 Photograph of a typical MSC FET



FLIP-CHIP TECHNOLOGY

Fig. 2 Cross-section of a flip-chip FET

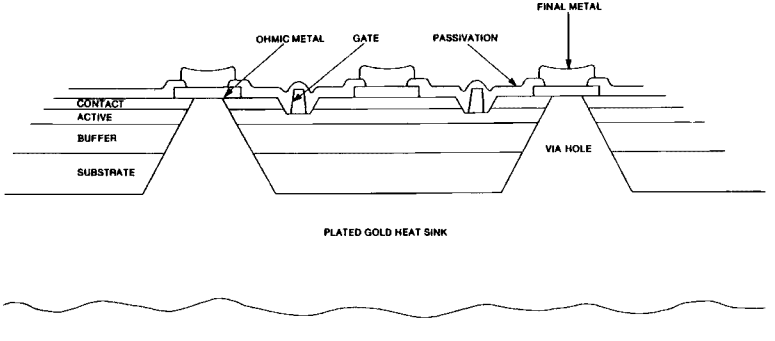


Fig. 3 Cross-section of a via-hole FET

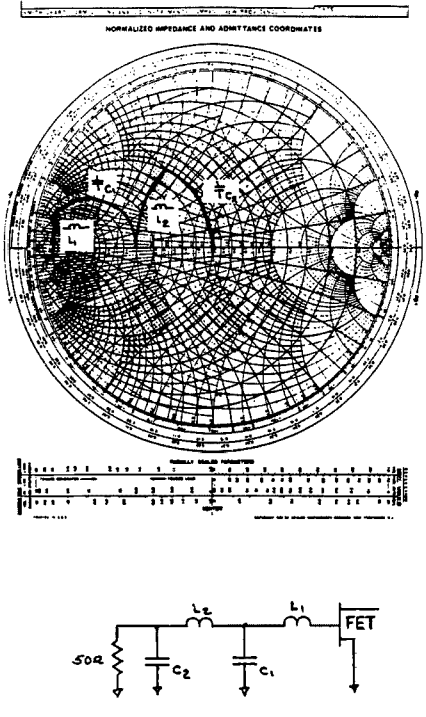


Fig. 4 Smith Chart representation of the design for an internally matched FET

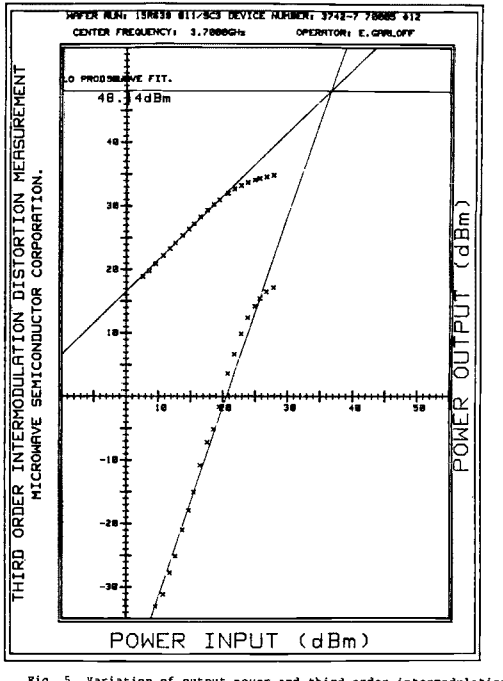


Fig. 5 Variation of output power and third order intermodulation distortion as a function of input power for a 3 Watt internally matched FET at 3.7 GHz

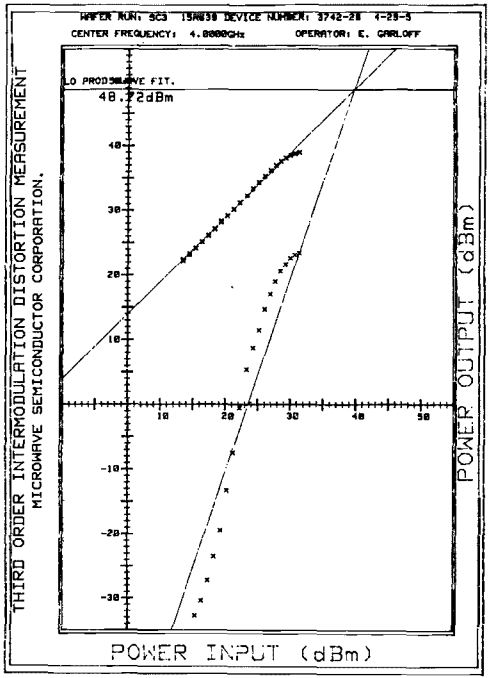


Fig. 6 Variation of output power and third order intermodulation distortion as a function of input power for a 10 W internally matched FET at 4 GHz

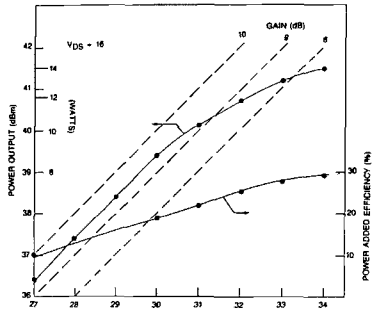


Fig. 7 PERFORMANCE OF HIGH VOLTAGE 28mm MATCHED POWER FET AT 5.3 GHz

TABLE 1. 14.5 - 15.35 GHz 1 WATT INTERNALLY MATCHED FET

Frequency (GHz)	Output Power @ G1dB (dBm)	Gain @ P1dB (dB)	Return Loss (dB)	Efficiency (%)
14.5	31	6	9.8	21
15.0	31.5	7.25	12	25
15.35	31	5.5	6	20

TABLE 2. 17 - 18 GHz 2 WATT INTERNALLY MATCHED FET

Frequency (GHz)	Output Power @ G1dB (dBm)	Gain @ P1dB (dB)	Return Loss (dB)	Efficiency (%)
17.0	33.5	4.7	10.5	19.3
17.5	33.2	4.7	25	18.5
18.0	33.5	4.0	14.6	18.1

LOW NOISE OSCILLATOR PAPER

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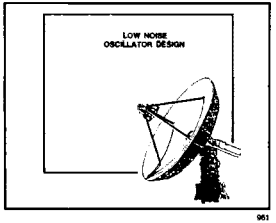

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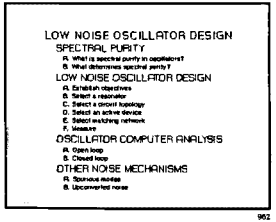

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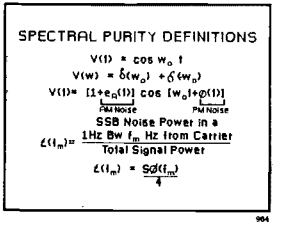
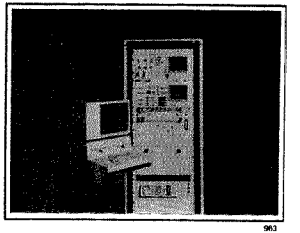

SPECTRAL PURITY DEFINITIONS
V(t) = cos w0 t
V(w) = δ(w0) + δ(w0)
V(t)= [1+eA(t)] cos [w0t+φ(t)]
AM Noise
PM Noise
£(fm)= SSB Noise Power in a 1Hz Bw fm Hz from Carrier / Total Signal Power
£(fm) = Sφ(fm) / 4

964



963

Spectral Purity describes the degree of degradation from a perfect impulse in the frequency domain:

$$V(t) = \cos \omega_0 t$$

$$V(\omega) = \delta(\omega_0) + \delta(-\omega_0)$$

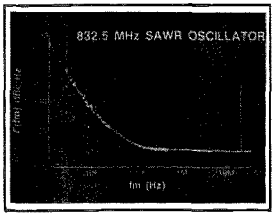
Real signals have some noise associated

$$V(t) = [1 + e_A(t)] \cos [\omega_0 t + \phi(t)]$$

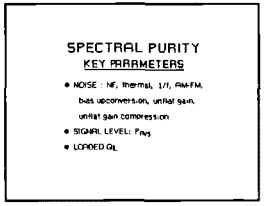
We will focus primarily on phase noise (PM) components. $\mathcal{L}(f_m)$ describes the ratio of SSB power in a 1 Hz B.W. due to phase noise, offset f_m Hz, from the carrier, to the total signal power.

Ref. 2, 14, 15

This is a typical phase noise measurement. This oscillator uses a 832.5 MHz surface acoustic wave resonator as the resonator. How good is this performance? Could it be better? What are the limits to the noise performance of this oscillator? What are the significant contributors to its noise?



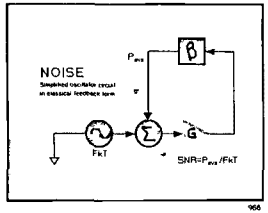
The previous phase noise plot was measured on Hewlett-Packard's 3047 phase noise measurement system. This system has the capability of measuring noise as low as ~−170 dBc. It covers the frequency range 10 MHz to 18 GHz.


SPECTRAL PURITY
KEY PARAMETERS
• NOISE : NF, thermal, 1/f, AM-FM, bias upconversion, unflat gain, unflat gain compression
• SIGNAL LEVEL: P_{avs}
• LOADED QL
985

Key parameters that will be important in our discussion of phase noise in oscillators include noise iteself as evidenced by the noise figure of the active devices and circuits used in the oscillator, 1/f noise of active devices and resonators, AM-FM conversion of noise, upconversion of bias noise, and unflat gain.

Signal levels in the circuit are important. Higher signal levels lead to higher signal to noise ratios and thus better phase noise.

We will see that loaded resonator Q will determine phase noise close to the carrier and that increasing loaded Q will improve phase noise close to the carrier.



We can model an oscillator in the classical feedback form with an amplifier with gain G and feedback β which includes the resonator. For oscillation at $f = f_0$, two conditions must be satisfied:

1. Loop gain is greater than one at f_0.

$$|G\beta| > 1 \text{ at } f = f_0$$

2. Phase shift around the loop = 0

$$\angle G\beta = 0 \text{ at } f = f_0$$

In the interest of preventing spurious oscillations at undesired frequencies, two other conditions should be met:

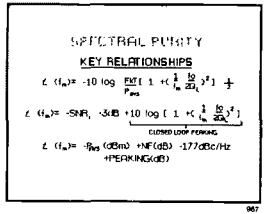
$$|G\beta| < 1 \text{ at } f \neq f_0$$

and

$$\Gamma_{node} < 1 \text{ for all nodes at } f \neq f_0$$

where Γ is the reflection coefficient looking into any node. (Meeting this condition at the collector and base nodes is usually sufficient.)

Signal to noise ratio at the input to the amplifier is P_{avs}/FkT where P_{avs} is the power available at the input of the amplifier and F is the noise figure of the amplifier.



We assume that the signal to noise ratio at the input P_{avs}/FkT causes both amplitude and phase noise in equal amounts. For frequencies far from resonance, f_0, where loop gain $\ll 1$, phase noise relative to the carrier will be

$$f_m = \frac{1}{2}\,\frac{FkT}{P_{avs}}$$

Thus

$$\mathcal{L}(f_m) = -SNR_i - 3\ dB$$

where

$$SNR_i = 10\ \log\ \left(\frac{P_{avs}}{FkT}\right)$$

for $f_m \gg$ loop bandwidth.

Close to the carrier, loop gain peaking will cause amplification of this noise. Let's first understand loaded resonator Q:

$$Q_L = \frac{f_0}{2}\,\frac{\partial \angle(G\beta)}{\partial f}\bigg|_{f=f_0}$$

where

$\frac{\partial \angle(G\beta)}{\partial f}$ = loop gain phase slope.

Loaded Q determines the open loop bandwidth of the feedback loop used to represent the oscillator. Inside the bandwidth,

$$\frac{f_0}{2Q_L},$$

when the loop is closed loop peaking increases phase noise. A first order approximation of phase noise is then

$$L(f_m) = \frac{1}{2}\,\frac{FkT}{P_{avs}}\left[1 + \left(\frac{1}{f_m}\,\frac{f_0}{2Q_L}\right)^2\right]$$

where

$L(f_m)$ = the ratio of SSB noise power due to PM in a 1 Hz bandwidth (centered f_m Hz off the carrier) to total signal power;

F = the noise factor of the active device;

k = Boltzmann's constant; = 1.38×10^{-23} W-s

T = Temperature (in °K ≈ 300°K)

P_{avs} = the power available from the source, resonator, in watts

f_0 = oscillation or carrier frequency

f_m = offset frequency

or

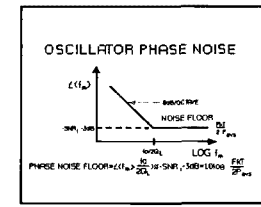
$$\mathcal{L}(f_m) = -10\ \log\left[\frac{1}{2}\,\frac{FkT}{P_{avs}}\left[1 + \left(\frac{1}{f_m}\,\frac{f_0}{2Q_L}\right)^2\right]\right]$$

or

$$\mathcal{L}(f_m) = -3\ dB - SNR_i + 10\ \log\left[1 + \left(\frac{1}{f_m}\,\frac{f_0}{2Q_L}\right)^2\right]$$

If we express P_{avs} in dBm, and knowing that thermal noise in a 1 Hz bandwidth = −174 dBm, then

$\mathcal{L}(f_m) = -P_{avs}$ (dBm) + NF (dB) − 177 dBc/Hz + peaking term (dB).



This slide presents the previous results in graphical form. For large offsets

$$\left(f_m \gg \frac{f_0}{2Q_L}\right),$$

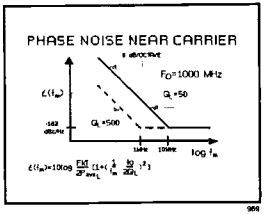
the phase noise floor =

$$\frac{FkT}{2P_{avs}} = -SNR_i - 3\ dB.$$

Inside the offset frequency

$$\frac{f_0}{2Q_L},$$

which is the bandwidth of the open loop circuit of our oscillator model, noise rises 6 dB/octave.



Let's look at an example. If we assume a power level of +10 dBm and NF = 5 dB then the phase noise floor

$$= -177\,\text{dBc/Hz} + \text{NF (dB)} - P_{avs}\,\text{(dB)}$$

$$= -177 + 5 - 10 = -182\,\text{dBc/Hz}$$

$$f_m \gg \frac{f_0}{2Q_L}$$

For phase noise close to the carrier, the equation for shows

$$L(f_m) \approx \frac{1}{2}\,\frac{FkT}{P_{avs}}\left(\frac{1}{f_m}\,\frac{f_0}{2Q_L}\right)^2$$

Thus

$$\mathscr{L}(f_m) \propto \frac{F}{P_{avs}}\,\frac{f_0^2}{Q_L^2} \propto \frac{f_0^2}{SNR_i\,Q_L^2}$$

To minimize phase noise we must maximize signal to noise ratio and loaded Q. Also notice that low phase noise is easier to achieve at low carrier frequencies.

In the example f_0 = 1000 MHz, P_{avs} = +10 dBm, NF = 5 dB, and Q_L = 50.

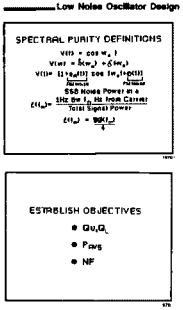
What is $\mathscr{L}$(100 kHz)?

$$\approx \text{phase noise floor + peaking}$$

$$\approx -182\,\text{dBc/Hz} + 20\,\log\left(\frac{f_0}{2f_m\,Q_L}\right)$$

$$\approx -142\,\text{dBc.}$$

If Q_L = 500, this improves 20 dB to −162 dBc/Hz.



Starting with a specific close-in phase noise requirement, $L(f_m)_{required}$, then Q_L can be determined from

$$L\left(f_m \ll \frac{f_0}{2Q_L}\right)_{required} \approx \frac{FkT}{2P_{AVS}}\left(\frac{f_0}{2f_m\,Q_L}\right)^2$$

$$\therefore\ Q_L \text{ required} > \sqrt{\frac{FkT}{2P_{AVS}}}\;\frac{F_0}{2f_m\sqrt{L(f_m)_{required}}}$$

Having Q_L, a resonator may be selected using a rule of thumb that $Q_U \geq 2$ to 5 times Q_L.

The power level, P_{avs}, is typically set by limitations in the resonator (higher power means greater AM-FM, and potential spurious responses, aging, etc.) or by NF or power handling limitations in the active device

$$\text{Phase Noise Floor} = L\left(f_m \gg \frac{f_0}{2Q_L}\right) \approx \frac{FkT}{P_{AVS}}$$

$$\therefore\ P_{avs} \gtrapprox \frac{FkT}{L\left(f_m \gg \dfrac{f_0}{2Q_L}\right)}$$

This relationship may also give a NF requirement

$$F \gtrapprox \frac{P_{AVS}\,L\left(f_m \gg \dfrac{f_0}{2Q_L}\right)}{kT}$$

Once a potential resonator has been selected, it makes sense to verify some of its parameters, notably its unloaded Q (Q_U), 1/f noise, and AM-to-FM conversion. The unloaded Q of a resonator can be measured on a network analyzer by coupling very lightly to the resonator and measuring either the 3 dB bandwidth, phase slope, or the group delay. For this purpose:

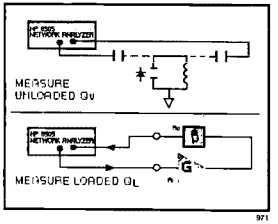
$$Q_U = \frac{f_0}{BW_{3\ dB}}$$

$$Q_U = \frac{f_0}{2}\ \frac{\delta\phi}{\delta f} = \pi f_0\, \tau_{GD}$$

where

$\tau_{GD} = S_{21}$ group delay in seconds

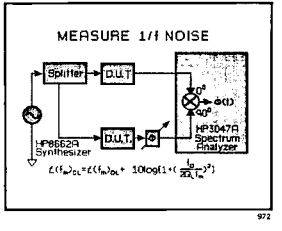
$\tau = Q_U/f_0\pi$

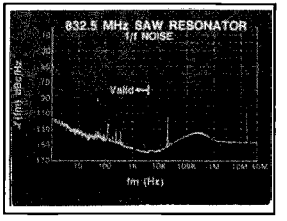


One helpful way to measure Q_U versus frequency is to set the network analyzer in the log frequency mode and draw a 6 dB/octave slope line falling off with frequency. If the group delay rises above the slope line, then Q_U is rising with frequency.

Verifying Q_L in the actual oscillator circuit is also possible, provided that the characteristic impedance Z_0 of the network analyzer is near the operating circuit impedance, or that transformers are used to match the impedances of the test system and the circuit over the frequency range, and power levels are near operating conditions.

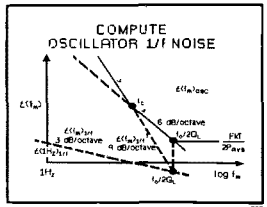
Ref. 12, 25, 26, 27





This is an example of 1/f noise measurement using the technique in the previous slide. These data are indicative of typical 1/f noise seen in SAW resonators: we've seen 5 to 10 dB better and 20 to 30 dB worse.

D. Halford has suggested a "rule of thumb" phase noise intercept of −115 dBc/Hz at a 1 Hz offset. See ref. 16.



It is possible to predict the phase-noise performance of the oscillator circuit (closed loop) by adding the white phase-noise component, FkT/$2P_{avs}$, to the 1/f component, $L(f_m)_{1/f}$, and then modifying both of these by the oscillator closed-loop gain peaking, $[1 + (f_0/f_m 2Q_L)^2]$. The total oscillator phase noise is

$$\mathcal{L}(f_m) = 10 \log \left[1 + \left(\frac{f_0}{f_m 2Q_L}\right)^2\right] \cdot \left[\frac{FkT}{2P_{avs}} + L(f_m)_{1/f}\right].$$

The components of 1/f and white phase noise of the amplifier-resonator combination are artificially separated. However, if we measure the total phase noise, $\mathcal{L}(f_m)_{OL}$, of the series amplifier-resonator open loop (with the correct terminating impedance and power levels), it's possible to predict the oscillator phase noise directly:

$$\mathcal{L}(f_m) = 10 \log \left[1 + \left(\frac{f_0}{2f_m Q_L}\right)^2\right] L(f_m)_{OL}$$

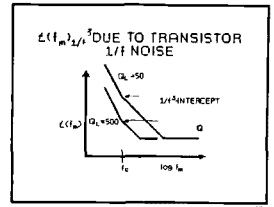
$$\mathcal{L}(f_m) = \mathcal{L}(f_m)_{OL} + 10 \log \left[1 + \left(\frac{f_0}{2f_m Q_L}\right)^2\right]$$

This phase-noise prediction can be shown more easily with a graphical approach. First, plot the phase noise due to white noise components. Then, draw $\mathcal{L}(f_m)_{1/f}$ on the same graph. Next, draw a −9 dB octave line that intersects $\mathcal{L}(f_m)_{1/f}$ at $f_m = f_0/2Q_L$. The intersection of this line with the locus of

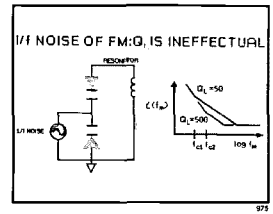
$$\mathcal{L}(f_m) = 10 \log \frac{FkT}{2P_{avs}} \left[1 + \left(\frac{1}{f_m} \frac{f_0}{2Q_L}\right)^2\right]$$

is f_c, the $1/f^3$ noise-corner frequency. The 9 dB/octave line then serves as the predicted value of $\mathcal{L}(f_m < f_c)$.

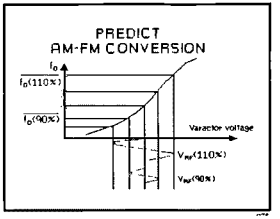
Ref. 41



If 1/f phase noise modulation is in the resonator or active device, then an increase in Q_L will improve the phase-noise performance in the 1/f region. This occurs because the loop peaking effect operates on 1/f noise as well as white noise as can be seen from the previous equations.



However, if the 1/f noise mechanism is frequency modulating the resonator center frequency, then no improvement of Q_L will lower phase noise in the 1/f region. If a noise source is phase modulating the oscillator, then changing the phase slope of the resonator—or changing the Q—will affect the depth of modulation.



In many VCOs, the spectral purity is dominated by AM-to-FM conversion mechanisms, rather than the SNR_1 and Q_L. One method to predict the AM-to-FM conversion in a diode-tuned VCO is by studying the frequency-versus-tuning-voltage characteristic. A change in the rf voltage amplitude on the resonator can affect the average bias on the varactor. A 10-percent change in resonator rf voltage corresponds to 10-percent AM on the carrier. To measure the effects of changing carrier level, one can increase or decrease the rf voltage on the resonator by changing the bias current in the active device. Measure the carrier frequency at 90-percent resonator voltage and compare this with the average carrier frequency at 110-percent resonator voltage. The peak-to-peak frequency shift due to 10-percent AM can then be estimated:

$$\overline{f_0(90\%)} \simeq \frac{f_0(+\text{peak}) - f_0(-\text{peak})}{2}$$

$$\Delta f_{pk}(10\%\ \text{AM}) = \frac{\overline{f_0(110\%)} - \overline{f_0(90\%)}}{2}$$

$$K_v(\text{AM/FM}) = \frac{\Delta f_{pk}(10\%\ \text{AM})}{10\%}\ \text{Hz pk/\% AM}$$

This equation provides a solution in frequency modulation/percent AM. The percent AM, A, should be no less than the collector bias current shot noise fluctuations divided by collector bias × 100 percent:

$$A\%\ \text{AM} = \frac{\sqrt{2}\sqrt{2qI_c}}{I_c} \times 100\% = 200\sqrt{q/I_c}\%$$

where

$\sqrt{2qI_c}$ = the full collector shot noise,

and

q= the charge of an electron = 1.6×10^{-19} Coulomb

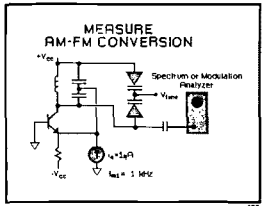
Now we can predict the closed loop phase noise contribution due to AM-FM:

$$\mathcal{L}(f_m)_{AM} = 20 \log \left[\frac{A\ K_v(\text{AM/FM})}{2\ f_m} \right]$$

or total phase noise:

$$\mathcal{L}(f_m) = 10 \log \left\{ \left[1 + \left(\frac{f_0}{2f_mQ_L} \right)^2 \right] \cdot \left[\frac{FkT}{2P_{avs}} + L(f_m)_{1/f} \right] + \left[\frac{A\ K_v(\text{AM/FM})}{2f_m} \right]^2 \right\}$$

Ref. 28, 29



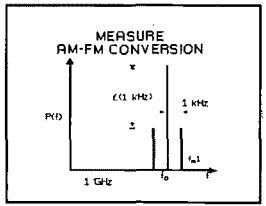
There are several methods for measuring the AM-to-FM conversion coefficient ($K_{vAM\text{-}FM}$). In one case, the resonator must be set up at the appropriate power level with the correct amount of coupling/loading, and connected to a network analyzer. By shifting the power level ±10 percent, and monitoring the center-frequency shift.

$$K_v(\text{AM/FM}) = \frac{\Delta f_{pk}(10\%\ \text{AM})}{10\%}\ \text{Hz pk/\%AM}$$

Another method of measuring AM-to-FM conversion is to adjust the transistor bias current 10%, monitor Δf, and use

$$K_v(\text{AM/FM}) = \frac{\Delta f_{pk}(10\%\ \text{AM})}{10\%}\ \text{Hz pk/\%AM}$$

Typically, a transistor is collector-current cutoff-limiting, so a 10-percent increase in the collector bias current will cause a 10-percent increase in the resonator voltage. The latter approach may cause a change in the active device's phase angle, but this is acceptable, since it's desirable to characterize the sum of all effects contributing to AM-to-FM conversion.



The AM-to-FM conversion can also be tested dynamically. This technique involves injecting a small, low frequency (f_i) current into the transistor's emitter. Adjust f_i until the sidebands around the carrier roll off 6 dB for each octave increase in f_i (which indicates FM):

$$P_{\%AM} = \left(\frac{\text{injected current peak}}{\text{emitter bias current}}\right) \times 100\%$$

$\mathcal{L}(f_i)$ = measured SSB-to-carrier ratio of the injected FM sidebands. From the narrowband FM approximation we have:

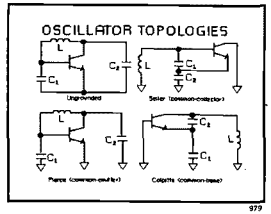
$$\mathcal{L}(f_i) = 20\ \log\left(\frac{\Delta f_{ipk}}{2f_i}\right)$$

$$\Delta f_{ipk} = (2f_i)\ 10^{\mathcal{L}(f_i)/20}$$

Δf_{ipk} = peak frequency deviation indicated by these sidebands

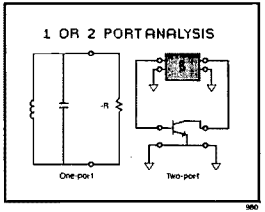
$$\therefore K_v(\text{AM/FM}) = \frac{\Delta f_{ipk}}{P_{\%AM}}\ \text{in Hz peak/\%AM}$$

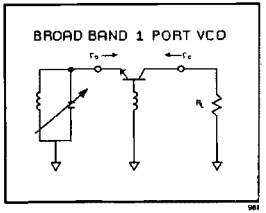
One can also measure this FM modulation directly using an 8901 modulation analyzer.

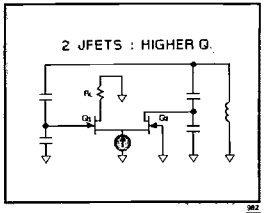


"Many oscillators can be reduced to a Colpitts configuration." The basic layout is an oscillator circuit without a ground terminal. By grounding this circuit at any of its nodes, it can be transformed into any of the other configurations. The preferred topology is one that makes it possible to visualize such things as loop gain, loop phase angle, and stopband stability.

The common-emitter (Pierce) topology is ideal for good out-of-band stability. It yields open-circuit stability at frequencies above about $f_T/3$, and can be kept stable at lower frequencies. Alternatively, the common-base (Colpitts) topology typically has negative real-part impedance at its emitter from about $f_T/5$ to f_{max}, depending on the base-to-ground parasitic inductance. The common-collector configuration, with capacitive loading on its emitter, typically possesses a negative real-part impedance at its base over a significant range of frequencies. Instability is a potential problem whenever there is a negative real part of the impedance at frequencies other than the desired oscillation frequency. The result can be spurious oscillation, squegging, parametric effects, and sharply nonlinear tuning characteristics, especially when a harmonic of the desired frequency crosses through a region of negative resistance. Refs. 9, 10, 4, 5, 6







Oscillator topologies can be designed as one-port or two-port configurations. One-ports (negative-resistance oscillators) have good track records in the gigahertz region. The two-port topology permits analysis and ease of visualization using feedback theory; loop gain and phase slope may be more easily derived (and measured) to predict loaded Q_L and spectral purity.

This one-port configuration is widely used in the gigahertz region with YIG-tuned oscillators and VCOs; multi-octave tuning range is a key advantage.

Despite its good points, however, this configuration has its drawbacks. It does not allow easy definition of loaded Q for the purpose of predicting phase noise, nor does it permit simple modeling of loop gain. This topology is also susceptible to spurious modes, since the conditions for the emitter relection coefficient, $\Gamma_e > 1$, leads to potential instability over a broad range of frequencies. The phase noise for this kind of oscillator can be accurately predicted by a computer method we will discuss shortly.

Refs. 17, 18, 19, 20, 21, 22, 23, 31, 32, 33

The choices are many: bipolar junction transistors, JFETs, SiMOSFETs, GaAs FETs, Gunn/IMPATT diodes, or miniature packaged amplifiers. In all cases, the selection criteria should include low noise figure at the maximum operating junction temperature; low noise figure at higher power in order to get the highest signal-to-noise ratio (SNR) possible; and low noise figure at the source impedance presented to the device. Certain warnings are also in order. Beware of large ripple occurring in small-signal S_{21} gain in the presence of a large signal at f_0; this indicates nonlinear compression. This is not a parameter that the device manufacturer will specify and must be measured on a network analyzer. Also, be wary of limitations in resonators, such as spurious content in YIG resonators ($\geq$ +10 dBm) and aging in SAW and bulk crystal resonators ($\leq$50 μW is typical for most frequency standards).

Of the devices listed above, the bipolar junction transistor is a natural for low-noise design due to its well-characterized and repeatable parameters. The characteristics of the other devices tend to be not quite so predictable. FETs, for example, exhibit significant variations in pinchoff voltage and performance with temperature. A good rule of thumb is to select f_T at least two to three times the operating frequency, and to remember that the noise figure degrades (i_n increases) as f_0 exceeds f_β.

Ref. 7

A JFET is a good choice for achieving low-noise oscillator performance at $f_0 \leq$ UHF. This performance is most likely due to the high input real-part impedance, which allows tight coupliing and little loading of the resonator (high Q_L). Concurrently, a good noise figure can be achieved with a high source impedance because the JFET input noise current (i_n) is so low:

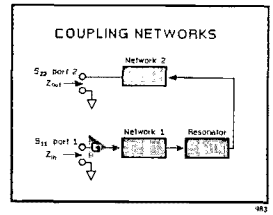
$$r_s \text{ (optimum NF)} = e_n/i_n$$

The end result is high SNR_i or very good phase-noise characteristics.

It has been mentioned that phase noise may be dominated by SNR_i and Q_L (ignoring 1/f noise for the moment). Good SNR_i and Q_L depends on the noise figure of the active device at the operating source impedance, on P_{avs}, and on the Q_L/Q_U degradation due to active device and output loading. The JFET possesses operating characteristics that enable it to achieve high Q_L/Q_U and SNR_i simultaneously.

In a two-port oscillator, there are three contributors to Q_L degradation: the input resistance of the amplifier, the output resistance of the amplifier, *and the load resistance. One way to* improve Q_L/Q_U and SNR_i is to use two devices in an oscillator circuit. This two-device circuit lightly loads the resonator due to the high input and output real parts of the JFET impedance. The load is isolated from the resonator by Q_1, thus removing the third contributor to Q_L degradation.

At low frequencies especially, take advantage of excess device gain to keep impedances large by using feedback. This will help to not load the resonator Q.



The purpose of an oscillator's coupling networks are: to match the input/output impedance of the active device to that of the resonator for optimum P_{avs}, Q_L, and NF; to provide enough phase shift to achieve 0-deg. phase in the angle of the loop-gain transfer function at f_0, where hopefully the loop gain is greater than 1.0 and near the maximum phase slope; and to select the desired operating frequency mode in a multimode oscillator. Some common forms of coupling networks are presented in refs. 12, 9, 10, and 37.

Three coupling network design objectives can also be stated mathematically as

$$|S_{21}|_{\text{loop gain}} > 0 \text{ dB}$$

and

$$\angle S_{21}|_{\text{loop gain}} = 0°$$

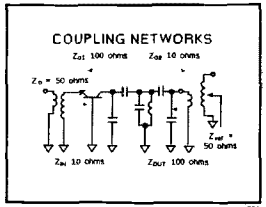
for $f = f_0$ only;

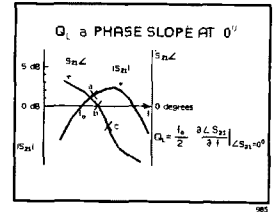
and

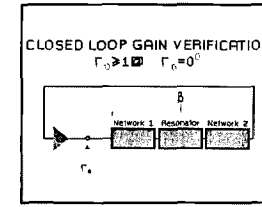
$$|\Gamma_{\text{node}}| < 1.0$$

for $f \neq f_0$ and all nodes.

Ref. 12, 9, 10, 37, 38







The S-parameter treatment is convenient for use with network analysis. The measured S-parameter data can be used in computer modeling and analysis, and for comparing measured and predicted performance.

A coupling network can be tested with the setup shown. In this slide, Z_{in} is the reference impedance for S_{22} at the output port, and Z_{out} is the reference impedance for S_{11} at the input port. The technique is exactly correct if $Z_{01} = Z_{out}|_{Port\ 2}$ and $Z_{02} = Z_{in}|_{Port\ 1}$. Other conditions are that Z_{in} be measured with Port 2 terminated in Z_{in}, while Z_{out} be determined with Port 1 terminated in Z_{out}. These conditions are not that easy to achieve; still, if the loop is broken where the impedances are reasonably well characterized (real), and ideal (computer-simulated) transformers are employed to get different input and output reference impedances, a model develops which provides fairly accurate loop gain/ ·se data.

From the previous model we get

$$|\text{loop gain}| \approx |S_{21}|$$

$$\angle\text{loop gain} \approx \angle S_{21}$$

The results may appear as those shown, where

$$Q_L = (f_0/2)(\partial\phi/\partial f)\,|_{\phi=0^\circ}$$

and

$$\phi(f) = \angle S_{21}(f)$$

It's apparent from this example that oscillation, point b, ($\angle S_{21} = 0°$) will not occur at the maximum phase slope, point c. Consequently, Q_L and the phase noise will be unnecessarily degraded. There is, however, sufficient loop gain (2 dB at point a) for oscillation.

Adjustments to a coupling network make it possible to achieve maximum Q_L, that is, $\angle S_{21} = 0°$ at the maximum phase slope. Coupling to the resonator can also be reduced (so that $|S_{21}| \approx$ +3 dB at $\angle S_{21} = 0°$) in order to increase Q_L. Recall that this action may have deleterious effects on P_{AVS} (the power available from the source in dBm) and noise figure as functions of the source impedance.

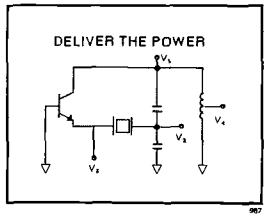
Another test (calculated or measured) for the effectiveness of a coupling network is to close the loop and analyze the reflection coefficient (Γ) at any node. This slide illustrates this concept. Looking at the output of the oscillator, the necessary condition for oscillation is

$$\Gamma_0 > 1\,|_{\angle\Gamma_0 = 0^\circ}$$

where

$$f_0 \approx f\,|_{\angle\Gamma_0 = 0^\circ}$$

Ref. 20



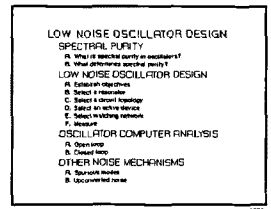
Once there is enough loop gain and the correct phase angle in a design, it's time to consider how to deliver power to the load. Power is typically taken from the resonator, but for the sake of flexibility, it should also be possible to tap signal power at any point in the oscillator loop. Tapping power at V_1, V_2, or V_4 may provide a high signal level to drive limiters and maintain a good noise floor. Node V_4 may have reduced harmonics content due to the lowpass filtering effect of the inductor. Taking power from V_3 may provide a lower noise floor due to some filtering created by the stopband rejection of the resonator crystal.

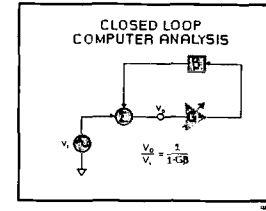
Another power-tapping technique is to reflect a load resistance, r_L, to a desired output node, such that r_L is much greater than the real-part impedance seen looking back into that node at f_0. This can be done with matching networks or transformers. As a consequence, the loop gain (and Q_L) is reduced (less than 3 to 6 dB), and the output power may not be significantly reduced.

Tapping power from the collector can provide out-of-band stability by reducing the real-part impedance as seen by the collector (common-emitter and common-base topologies). This creates heightened rejection of undesired modes.

There are many techniques for matching to a load. One method relies on series-to-parallel transformations, ref. 37.

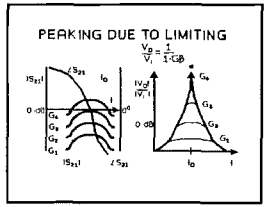
Oscillator Computer Analysis





A computer helps to evaluate oscillator circuit output-noise spectral density (phase noise) and signal power in a closed loop format by using linear, frequency-domain analysis techniques. This approach is really just an extension of classical feedback control theory. An oscillator is a feedback amplifier whose poles of closed-loop gain transfer function have moved into the right half-plane. Feedback amplifiers may be analyzed for noise and transfer function for any degree of peaking as long as the poles remain in the left half-plane (resulting in no oscillation). If an oscillator is analyzed with its loop gain adjusted for poles very near the $j\omega$ axis, the output noise spectral density will be essentially the same as if the poles were exactly on the $j\omega$ axis (resulting in oscillation).

Since this method accurately predicts and uses actual operating power levels, then P_{AVS} does not have to be known apriori. The computer easily handles the changing NF as a function of rapidly changing source impedance near resonance since we are using actual noise generators in our modeling (not an assumed NF).



These figures demonstrate in more detail the process which allows linear-frequency-domain computer analysis to predict closed loop phase noise. If we focus on f_0 where $\angle S_{21} = 0°$ and just modify $|S_{21}|$, then the closed loop gain becomes:

$$\frac{V_0}{V_i}(f_0) = \frac{1}{1 - G\beta} = \frac{1}{1 - |S_{21}|}$$

and we see as $|S_{21}| \rightarrow 1.0$ then

$$\frac{V_0}{V_i}(f_0) \rightarrow \infty$$

goes to infinity. Note the shape of the closed loop gain peaking at the +3 dB corner,

$$f_m = \frac{f_0}{2Q_L},$$

changes very little whether the peak is 40 dB or 90 dB or ∞. Very little is gained by focusing on very close in phase noise

$$\left(fm \ll \frac{f_0}{2Q_L}\right)$$

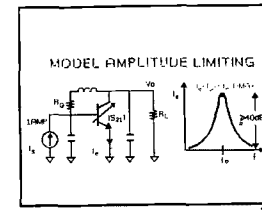
because the shape will remain a constant 6 dB/octave unless we are investigating the effects of crossing high Q spurious modes.

A basic modeling procedure for predicting parameters like phase noise, P_{OUT}, or node voltages and branch currents follows eight steps:

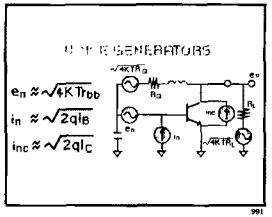
- choose a limiting mechanism (e.g., collector current) for modeling the oscillator. Typically, adjust $|S_{21}|$ of the active device to model the collector current cutoff limiting.
- inject a current source into any node.
- adjust the gain $|S_{21}|$ to model the limiting mechanism so that the closed-loop gain peaking is greater than 40 dB.
- monitor the emitter current at resonance during the computer analysis and scale the computer-analyzed value to the limiting current actually found or predicted in the circuit.
- scale all node voltages and branch currents by this factor. This provides output voltage, resonator voltage, and any other branch current or node voltages during oscillation.
- remove the current source and add all appropriate noise voltage and current sources.
- plot the spectral density of the output noise.
- review the ratio of the output voltage to the output noise (in a 1 Hz bandwidth) gives the predicted SNR_i, hence the phase noise:

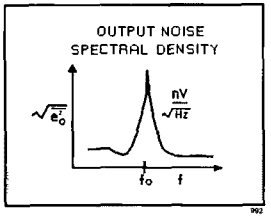
$$\mathcal{L}(f_m) = -SNR_0(f_m) - 3\,\text{dB} \text{ (for PM only)}$$

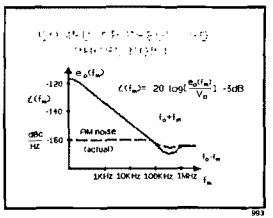
Ref. 11



This transistor oscillator is biased for collector-current cutoff-limiting (no saturation) operation. Experience teaches us that when the transistor goes into compression then $|S_{21}|$ decreases and $\angle S_{21}$ remains approximately the same. As a result, the loop gain variation with level can be modeled through $|S_{21}|$ adjustments alone. A more sophisticated model might use full-blown large-signal S-parameters and adjust S_{11}, S_{12}, S_{21}, and S_{22} accordingly (this has not been found necessary to achieve accuracies within 1 to 2 dB).







The next step in this example is to adjust $|S_{21}|$ until there is at least 40 dB peaking in output due to I_S. The exact amount of peaking is not critical, so long as

$$20 \log \frac{I_e(f_0)}{I_e(f \gg f_0)} \geq 40 \text{ dB}$$

Following this, monitor the emitter current and scale peak value of $i_e(f)$ to the actual emitter bias current, I_E

$$\text{scale} = I_E/[I_e(f)_{max}]$$

With this completed, all node voltages and branch current of interest can be predicted with

$$V_0 = \text{scale} \times V_0(f_0)_{max} = \text{output voltage}$$

$$\left.\begin{aligned} V_N &= \text{scale} \times V_N(f_0) \\ I_B &= \text{scale} \times I_B(f_0) \end{aligned}\right\} \text{ any node or branch}$$

The next step is to remove I_S, introduce all noise generators, and plot the spectral density of the output noise voltage. The computer can automatically generate appropriate noise for all lossy elements.

The use of noise current i_{nc} accounts for that component of i_n which increase as f approaches f_T ($f \gg f_\beta$).

Ref. 7, 8

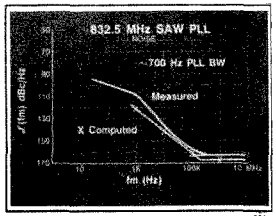
Output phase noise $\mathcal{L}(f_m)$ is simply the ratio of output noise, $e_0(f = f_0 \pm f_m)$, to the output signal voltage, V_0, subtracting 3 dB for the desired phase modulation components only:

$$e_0(f_m) = e_0(f = f_0 \pm f_m)$$

$$\mathcal{L}(f_m) = 20 \log [e_0(f_m)/V_0] - 3 \text{ dB}$$

Unfortunately, this procedure gives no indication of AM noise performance. However, experience has shown that the AM noise is often within 3 to 6 dB of the phase noise floor for

$$f_m \ll \frac{f_0}{2Q_L}$$



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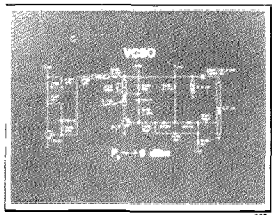

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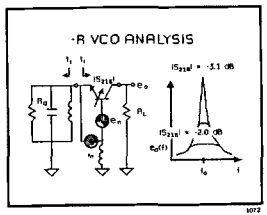

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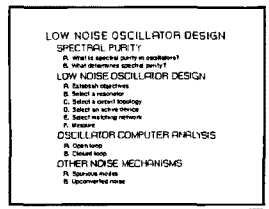


1073

These two figures show the computer model and a comparison of predicted results versus *measured data*. The *computer model* was even more detailed, including parasitic reactances and e_i and i_n. Small signal S-parameter data were used to model the transistors.

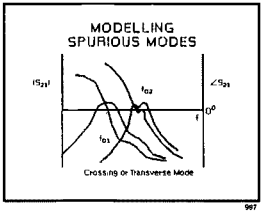
The discrepancy below 10 kHz is due to SAWR 1/f noise and PLL residual noise. The discrepancy above 100 kHz is due to noise contributions of 4 buffer-limiter stages which were not modeled; *measurements in* phase noise floor with the buffers removed indicate ≈ -165 dBc/Hz (computer suggests -167 dBc/Hz).

The advantages are that we have a precise and controllable experiment with which to better understand the "whys" behind the oscillator performance and predict worse case conditions.

One-port or negative resistance type oscillators may be handled similarly. The procedure involves modeling the oscillator in the manner applied to two-port oscillators, adding in all noise generators, and adjusting $-R$ or $|S_{21b}|$.

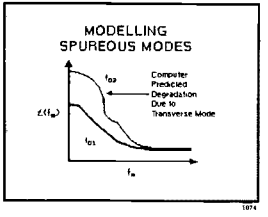
The adjustment of $|S_{21b}|$ to achieve better than 40 dB peaking can be automated if an analysis program has optimization capability. The technique requires searching for a peak near resonance and optimizing $|S_{21b}|$ for maximum peaking. It should be kept in mind that f_0 changes slightly with $|S_{21b}|$.

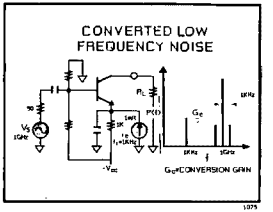
S_{21b} = common base S_{21}



Computer analysis also allows modeling spurious modes (such as transverse, crossing, and tracking modes) in a resonator (model or use measured S-parameter data). The technique consists of repeating the phase noise analysis either near (f_{01}) or coincident (f_{02}) with the undesired mode. In this way, it's possible to see the blooming effect on phase noise due to degradation in phase slope for a coincident mode, or phase noise peaking in the noise floor away from the carrier due to an adjacent mode that comes within 3 to 6 dB of the loop gain of the desired mode.

These analyses were computed from a SAWR oscillator using S-parameter data of the SAWR which has a transverse mode approximately 200 ppm above the desired mode.





A more complicated noise degradation mechanism is low-frequency noise upconverted around the carrier. Low frequency noise contributors (1/f base current noise and e_n or i_n) may cause excess emitter current noise in the audio frequency range if no attention is paid to low frequency source impedance and feedback effects. When the active device is near compression, the upconversion gain for i_e up around the carrier can be as low as −3 to −9 dB. We can measure this by injecting a low level current i_e into the emitter:

Audio upconversion gain, G_C, is

$$G_C = 20 \log \frac{i_e(1\ \text{GHz} + 1\ \text{kHz})}{i_e(1\ \text{kHz})}$$

The phase noise in amplifiers due to low frequency noise $i_{ne}(f_m)$ is then

$$\mathcal{L}(f_m) = 20 \log \frac{i_{ne}(f_m)}{I_e(f_0)}$$

$$-3 \text{ dB} + \text{upconversion gain}$$

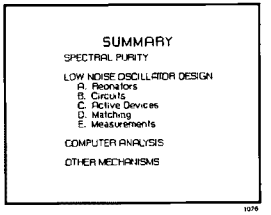
and in the oscillator add the peaking

$$\mathcal{L}(f_m) = 20 \log \frac{i_{ne}(f_m)}{I_e(f_0)}$$

$$-3 \text{ dB} + G_C + 10 \log\left[1 + \left(\frac{f_0}{2Q_L f_m}\right)^2\right]$$

To prevent these problems analyze via computer the emitter current noise spectral density of the oscillator and all buffer chains from DC to beyond f_0. Typically, the noise floor due to this mechanism should be 10 dB lower than the specification limit of that contributed by the oscillator.

There appears to be at least two kinds of 1/f noise in transistors: (1) upconverted 1/f component of base current noise; (2) 1/f phase modulation of the RF signal through the transistor. The reason these components seem separate and distinct is that component (1) should be level dependent since it is upconverted by a nonlinear mixing process. Our measurements show that the 1/f PM of active devices remain virtually constant over a significant range of RF power (from limiting to well inside the linear active region [small signal]). Also measuring the 1/f base current noise and the upconversion coefficient we find that the actual residual 1/f phase noise of the amplifier is 20 to 30 dB greater than hat predicted by upconversion.



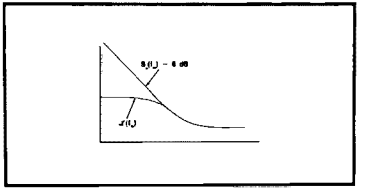
In summary some of the causes of phase noise in oscillators and what to do about them were discussed. The effects of resonator Q, resonator and device 1/f noise, and AM-FM conversion on phase noise were discussed. Oscillator topologies and active devices were looked at. Coupling to resonators and coupling to loads and their effects on noise were examined. Methods of measuring and computer modeling the causes of noise in oscillators were discussed. And lastly, mention was made of other mechanisms that can cause noise.

Appendix 1

$\mathcal{L}(f_m) = 20 \log \frac{\Delta\phi}{2}$ narrowband FM approximation

$$\left.\begin{aligned} L(f_m) &= \frac{S_\phi(f_m)}{2} \\ \mathcal{L}(f_m) &= S_\phi(f_m) - 3 \text{ dB} \end{aligned}\right\} \text{ for } \Delta\phi_{rms} \ll 1$$

In this article we have assumed $\mathcal{L}(f_m) = S_\phi(f_m) - 3$ dB everywhere for simplicity. Actually as we approach the carrier $\mathcal{L}(f_m)$ flattens out:



Reason: $\mathcal{L}(f_m)$ is the power in 1 Hz band centered f_m Hz off the carrier due to PM divided by total signal power. This is what we would see on a spectrum analyzer with a 1 Hz B.W. if reference level (0 dB) was the total signal power.

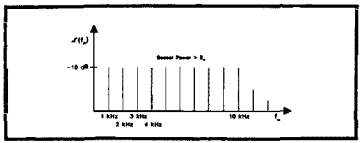
$S_\phi(f_m)$ is the phase spectral density or 20 log $\Delta\phi^2(f_m)$ in the 1 Hz B.W. Here's a simple example which may clarify:

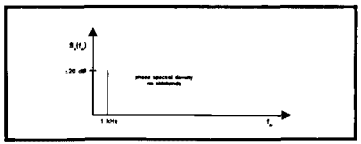
for $\Delta\phi > 1$ radian

Signal: $V(t) = \cos(\omega_C t + 10 \sin 2\pi 10^3 t$ or carrier with $\Delta f = 10$ kHz

fm = 1 kHz; $\beta = 10$ = mod index

Appendix 1





$\phi(t) = 10 \sin 2\pi\ 10^3 t$ no harmonics

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LIST OF SYMBOLS

f = offset frequency

FM = frequency modulation

AM = amplitude modulation

S- = scattering parameters

Q_L = loaded Q

SAW = surface acoustic wave

P_{res} = power available from source (resonator) in Watts

$P_{AVS} = 10 \log P_{res} + 30$ dBm

Po = output power

CE = common emitter

CC = common collector

CB = common base

Γ = reflection coefficient

ϕ = angle of loop gain

LIST OF SYMBOLS

K_v = VCO gain: Hz/Volt

τ_{GD} = group delay

I_E = emitter dc bias current

I_c = collector dc bias current

I_e = emitter AC signal current rms

f_o = frequency of oscillation

i_{nc} = collector noise current in $A_{rms}/\sqrt{Hz}$

i_{ne} = emitter noise current in $A_{rms}/\sqrt{Hz}$

$\mathcal{L}(fm)$ = single sideband power in a 1 Hz bandwidth (due to phase noise) referred to signal power in dBc/Hz (see Appendix II)

SNR_1 = signal to noise (1 Hz BW) referred to input in dB =

$$10 \log \frac{P_{sys}}{FkT}$$

$L(fm)$: $\mathcal{L}(fm) = 10 \log L(fm)$

NF = 10 log F = noise figure in dB

F = noise factor

e_o = output noise voltage in volts rms/$\sqrt{Hz}$

G = active device gain

r_s = source resistance

f_T = current gain-bandwidth

K_v (AM/FM) = VCO gain due to AM-FM in Hz/%AM

$\mathcal{L}(f_m)_{OL}$ = open loop phase noise

HEWLETT PACKARD

Broadband GaAs Monolithic Amplifiers and Their Applications

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Introduction

NEC has recently introduced three new low cost broadband MMICs designed for medium power, low noise, and gain block applications. Each MMIC is a cascadable, multi/octave, 50 ohm device. Typical bandwidths are from 50 MHz to 3GHz with NF as low as 2.7 dB for the UPG100 and high linear power of 20 dBm for the UPG101. The third device is the NEPA1001 which is a general purpose GaAs MMIC which is similar to the UPG100 except with a higher noise figure.

Application of these amplifiers is limited only by the designers imagination. These devices are relatively simple to use, but their wide bandwidths and high fmax require care and good design technique. It is our intent to help the designer who may not be totally familiar with using these devices.

Performance Specifications: 50 to 3000 MHz

		NEPA1001*			UPG100			UPG101		
Item	units	min	typ	max	min	typ	max	min	typ	max
Linear Gain	dB	10/12		15	16			14	16	
Flatness	±dB			1.0/1.5	1.0	1.5		1.0	1.5	
Noise Figure	dB		4/4.3	4.5/5		2.7	3.2			5.5
Power Out	P1dB	7	9		3	6		17	20	
Isolation	dB	35	40		30	40		30	40	
Input R.L.	dB	6	10		7	10		7	10	
Output R.L.	dB	10	16		10	13		10	13	
Idd	mA	40	60	80	30	45	60	70	100	160
Vdd			5			5			8	
Igg	mA		4	5		0.7	1.5		1.1	3.0
Vgg			-5			-5			-5	

* NOTE: These parameters are divided into two frequency bands; .1 - 2 GHz and 2 - 3 GHz.

Fabrication of the NEPA1001

The NEPA1001 is a two stage GaAs MMIC broadband amplifier using FETs with a closely spaced electrode structure. The devices are fabricated by self-alignment technology using Al side-etching techniques to obtain reproducibility of the spacing between the drain to gate and the source to gate electrodes. As a result, these spaces are reduced to .4 micron. Resistance is reduced in both electrodes and results in a cutoff frequency of *18 GHz*. This process is unique in its utilization of ion-implantation. The FET's active layers are formed by using silicon

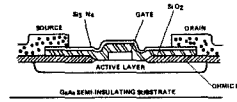


Fig. 1

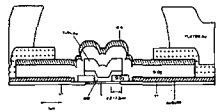


Fig. 1B

ion-implantation into a semi-insulating GaAs substrate. These implanted layers are then annealed in a hydrogen atmosphere. All metalizations on the chip are defined by using dry-etching technology. Combining these fabrication techniques results in a highly reproducible GaAs MMIC.

Fabrication of the UPG100 and UPG101

The UPG100 and UPG101 are also two stage broadband MMIC amplifiers. Fabrication of these devices is slightly different than the NEPA1001. The UPG series amplifiers employ a FET structure which has a tungsten silicide (WSI) *offset gate instead* of the closely spaced electrode structure. Otherwise the same general process are used for both series of amplifers. The tungsten silicide structure was chosen to improve durability of the devices as well as improve yield and manufacturability. The tungsten silicide process uses what is typically known as a T gate. This process allows the deposition of other metals (Ti, Pt, Au) on top of the tungsten silicide Schottky gate. As a result, higher conductivity is possible, providing improved overall performance. Presently, this process lends itself better to MMIC fabrication than the close electrode structure. The close electrode structure features side wall etching to achieve short gate lengths. This process does work well, but is more difficult to control for complex devices. Another advantage of the WSI technology is improved protection against electrostatic discharge.

Circuit Configuration

The configuration for the UPG100 and 101 are nearly identical. The UPG100 is the low noise version and differs mainly in the type of FETs used. The first stage uses a gate width of approximately 1000 microns to improve the input return loss. The second stage uses a device that is about half the gate width of the first stage for improved output return loss. Both devices have gate lengths around .8 micron. One would expect a low noise device for the input which is typically a smaller device. Since smaller FETs exhibit a somewhat higher impedance than larger devices, a larger FET was chosen to simplify the required input matching circuitry.

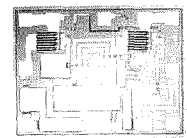


Figure 2

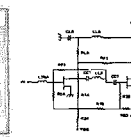


Figure 3

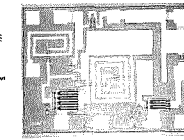


Figure 4

The UPG101 uses 2 larger 1000 micron FETs for both the input and output. The larger output device is the key to the higher output power. Normally, drain currents over 60 mA are very difficult to control using internal bias circuitry. To overcome this problem, an external RFC is required to supply bias to the final stage. Even though the internal drain resistor is bypassed by an external RFC, it still serves two functions. The first is to improve output VSWR and secondly it provides improved circuit stability from high impedance loads. Failure of the RFC will not damage the device. If Vdd is lost to the choke, the drain current will be about half. At this current level the internal resistor can still safely dissipate the power.

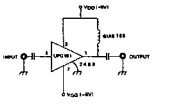


Figure 5

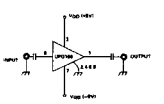


Figure 6

Since the UPG100 has a typical drain current of only 45 mA, internal bias is used and therefore an external choke is not required.

A slightly different configuration is the NEPA1001. As shown below, feedback is achieved from the drain of the first stage. The NEPA1001 is a gain block, but can be used in other applications. A low noise figure was not a design goal for this amplifier. Using this amplifier is similar to using the UPG100 in that an external RFC choke on the output is not required.

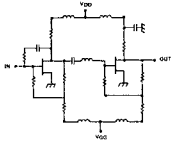


Figure 7

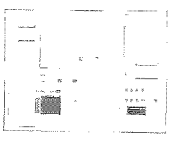


Figure 8

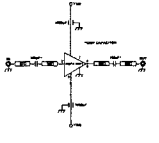


Figure 9

Unfortunately, nature's limitation to the amount of capacitance which can be achieved on GaAs necessitates external blocking capacitors. External blocking capacitors should be of good quality with low ESR and minimal parasitics.

One should consider these capacitors as a series RLC network and keep in mind that their physical size could be too large at 3 GHz. Capacitors other than chip capacitors are not recommended. Leaded capacitors will have too much parasitic reactance. This will either degrade the overall performance of the amplifier or result in unexpected oscillations.

The low frequency performance is also limited by the available capacitance. The internal stages inside these amplifiers are not DC coupled. They all have a blocking capacitor to provide DC isolation in between the stages. This capacitor only serves to block DC. Peaking is provided by the inductor in between the two blocking capacitors. The other critical reactance is Cgs of the following stage. Together L and Cgs achieve a dominant pole slightly beyond 3 GHz. Unfortunately the inductor takes a lot of room also; thus complete peaking is not achieved. Typcial values for the blocking capacitors and peaking inductor are listed below.

	NEPA1001	UPG100	UPG1001
C1:	20 pf	25 pf	25 pf
L1:	3.2 nh	3.2 nh	3.2 nh
C2:	-	8 pf	10 pf

The internal blocking capacitors are the limit of the low frequency response of around 50 MHz. When using caspacitors in MMICs, the low frequency limit is a difficult problem due to the amount of space these elements require.

Digitizing the Amplifiers

These amplifiers will not perform as well as DC coupled amplifiers for digital data. This type of amplifier will distort a digital waveform. Distortions can be seen as poorly defined peaks and valleys in a 1.2 gigabit NRZ stream. Typical bandwidths required to overcome this problem are approximately 100 KHz to 1.6 GHz and up. The limitation lies mainly in the low frequency limit of the amplifier. The upper limit defines the maximum data rate the amplifier can reproduce. At this time NEC is developing a new AGC amplifer which will be suitable for high speed digital data.

Application of the UPG100 and the NEPA1001

Simplicity is always desired in any circuit. These devices require only a few external components. As with any RF circuit, good grounding technique (up to and including microwave frequencies) is of primary concern. Ground loops are traps which have left even the best of designers in a frenzy. Make sure that the ground point is really a ground and not some reactance to ground. Using a few extra plated through-holes may be expensive for board processing, but will prove to be of great value in achieving good performance. These amplifiers have considerable gain well beyond 3 GHz. The user may only intend to use the device to 2 GHz, but the grounding should be sound beyond 3 GHz. A simple test for ground loops is to note S21 of the device. If steep and abrupt responses or oscillations occur, assume grounding problems exist. We have tested quite a number of these devices and found that the response is somewhat smooth. By touching the ground plane one should not expect any changes in the response. If any changes occur, most likely there's a grounding problem. The solution to this is usually simple for a new circuit; either add more plated through-holes or relocate them. With old circuits, one can add

self-tapping screws that either add more grounding points or knock out the hot spots. Keep in mind that RF currents flow on the outside of the conductors. Transitions can be tricky. Try to choose a ground as close as possible to common to both the ground of the device and the ground of the circuit. Critical ground pointsin this case will be at the connectors and directly below the grounds of the amplifier or bypass capacitors. Having an extended path will introduce an additional reactance in series to the ground circuit. In active devices, this usually results in negative resistance. Under the right conditions, oscillations could result. Below are two circuits, one which we found acceptable, and one which was unacceptable.

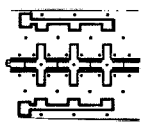


Figure 10 - GOOD

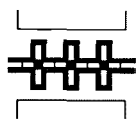


Figure 10A - BAD

Single Stage Operation - NEPA1001

The NEPA1001 is available in two types of packages. The AA package is a can type, and the FA is a hermetically sealed ceramic flat pack. The flat pack is straight forward and is a surface-mountable amplifier on microstrip. Two opposing leads are used to supply +Vdd and -Vgg. Orthogonal to those leads are another set of opposing leads which are the input and outputs. The back side of the package is the ground.

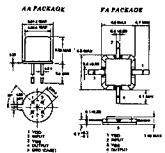


Fig. 11

Mounting of the FA package requires soldering the back side of the device. This can be accomplished in many ways and will most likely vary from one application to another. We tried two methods. One was using a device that was heat sunk to a brass block and the other was to cut a hole in the PC board to pick up the ground from the back side of the board.

The FA package was mounted on a brass block by first mounting the circuit with precut holes for the MMICs on to that block. Next the device and its location was pretinned with 93 degree low temperature solder. This solder was chosen mainly because it was available within our lab, and could have been substituted for a higher temperature. The only constraint was to choose a solder that would not require the back side of the MMIC to exceed about 230 degrees C. since the chip is die-attached by eutitic Au-Sn solder. Then the device was carefully dropped into place after the solder started to wet by applying a light pressure by hand through the eraser of a pencil. When the block cooled below the liquid phase of the solder, we carefully removed the pressure. The device has be firmly in place. Finally the last step was to solder the leads. Maximum temperature for this operation is 260 degrees C for no more than 10 seconds.

Our second approach was considerably easier, but has the disadvantage of poor thermal dissipation. This method should not be used for the previously mentioned UPG amplifiers. We started by cutting a hole for the device into the PC board. The device was then dropped into place with its leads flush with the top side of the board. The thickness of the board was chosen so that the back side of the device would be flush with the ground plane. Lastly, the back side of the device was soldered to the circuit board ground plane by regular 60/40 solder.

Mounting of the canned version or AA package is like that of a general purpose transistor. It is important to note that the case is the amplifier ground. This amplifier is also configurable for self biasing.

Self-Biasing the NEPA1001

NEC has suggested the following method for self-biasing. Since we must self bias two voltages (Vdd and -Vgg), a total of 10 volts is required. The ground must be RF ground regardless of its DC voltage level. This is accomplished by bypassing RF to ground through at least three 1000 pf chip capacitors. Single positive supply operation is realized by pulling up the potential of the ground against the Vgg terminal.

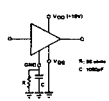


Figure 12

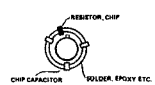


Figure 13

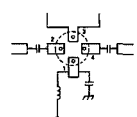


Figure 14

Negative self-biasing is also possible with the NEPA1001 by pulling up the ground terminal against the Vgg terminal (-10 volts).

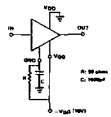


Figure 15

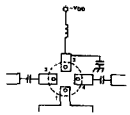


Figure 16

The required resistor for achieving self-biasing can be found by simply applying Ohm's law (remember we want to drop 5 volts):

$$R = \frac{5 \text{ volts}}{Idd}$$

In both cases a resistor value of 90 ohms is required for an Idd = 55 mA.

Self-Biasing the UPG100

Treatment of the UPG100 is schematically the same as the NEPA1001. Packaging is quite different from the NEPA1001 and requires a similar but slightly different approach. The UPG100 is an 8-pin flat pack. Input and output pins are opposite to each other. Orthogonal to those pins are 3 opposing sets of leads. In the center of each set of 3 leads are the bias supply lines (Vgg and Vdd). The outer leads are the grounds. By applying the same techniques for choosing the bias resistor for the NEPA1001, one can pull up or down the voltage for either positive or negative supplies. One should also ground all four corner leads with chip capacitors of 1000 pf or larger.

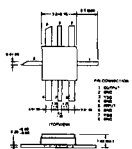


Figure 17

Remember that the bottom of this amplifier is not at ground potential relative to the circuit Either provide a pad for all 4 leads and the back side, or prevent the DC ground of the device from coming in contact with the circuit ground. Below is the "H" shaped ground pad that we used to isolate the circuit ground from the amplifier ground. Chip capacitors were located, after the device was installed, at each leg of the "H" pad to the circuit ground.

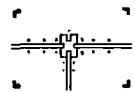
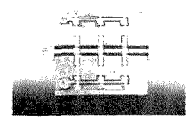


Figure 18

Cascading

Cascading these devices requires good grounding as well as good decoupling between stages. High gain in excess of 40 dB· requires care. Below is an example of a typical circuit



Chokes are recommended but not necessarily required. In this case we choose not to use the chokes in order to see how sensitive the bias line was for high gain amplifiers. This resulted in a three stage amplifier that showed no signs of bias instability. If one were to use chokes, a few turns on a ferrite core would most likely suffice. Capacitive decoupling is important. We used at least one 1000 pf chip capacitor on each bias supply as close as possible to the device. Chip capacitors were also located periodically along the main bus and where each of the bias lines converged. Flatness was very dependent on the coupling capacitors in between the stages. Our data sheet recommends 100 pf chip capacitors. We have found that many of these capacitors will exhibit intolerable reactances. First we tried 100 pf chip caps. The response showed shallow glitches (figure 19a-1). Next we tried 1000 pf (figure 19a-2). This removed the previous glitches. Since the 1000 pf capacitor improved the high end of the amplifier a lower capacitance was chosen. Finally a 500 pf capacitor was chosen (figure 19a-3) and resulted in a similar response to the previous 1000 pf chip capacitor. Clearly the parasitic reactance of the capacitors was interacting with the amplifiers. This was concluded since the effect of the amount of capacitance was opposite to the expected response.

Input and output load pulling has shown this configuration to be unconditionally stable. This should be expected since these amplifiers exhibit a stability factor (K) of about 3, at 3.6 GHz, and greater than 20 at 100 MHz. Shown below is the performance of the previous discussion and NEC published data of three cascaded NEPA1001 amplifiers.

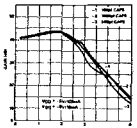


Figure 19a
(CEL)

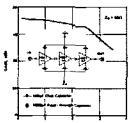


Figure 19b
(NEC)

Application of the UPG101

Much of the same precautions for handling and circuit layout apply to the UPG101 as they do to the NEPA1001 and UPG100. The package of the UPG101 is identical to the UPG100. The UPG101 requires only one additional bias point. Remember that this device is a medium power amplifier and that the drain current must be applied through an external RF choke. Most any conventional high frequency choke will work. The only precaution is that the choke must look for high impedance across the entire band.

In many cases, transformers or chokes will resonate when the wire becomes a magical length of 1/4 wave length. One approach that offers extremely good performance is to wind a 30 turn, 30 guage wire conical choke (Height = .375 mils, angle from longitudinal axis = 30 degrees) loaded with an absorbing material such as Ecosorbe MF-114. Another approach is to wind about 20 turns onto a high frequency torroid core. NEC suggests winding about 20 turns of 38 guage wire on a 1/4 watt resistor. This method works reasonably well and has the advantage of being inexpensive as well as mechanically stable. The disadvantage is that one can expect about 1 dB loss with this approach and will yield about a 11 dB return loss of the bias tee alone. The cone and the torroid provided about 20 dB return loss up to about 5 GHz with an insertion loss of about .7 dB.

It would be a good idea to check the choke by simply connecting the choke across the transmission line to ground. The design goal of such a choke should be the removal of all self resonances far enough away from the passband of the amplifier.

Self Bias of the UPG101

Self biasing the UPG101 is difficult. The high drain current would require a large resistor which may contribute large reactance for microwave work. Should a user need or attempt to use this configuratrion, CEL would like to hear your comments.

Handling the UPG and NEPA Series

Remember, active GaAs FETs are components of these devices. Static discharge and biasing precautions are a must. Also, remember that when powering-up, never apply the drain voltage before the gate voltage. The smaller signal devices, UPG100 and NEPA1001, are current-limited by a drain resistor. Limiting drain current makes the devices more forgiving to biasing errors. No doubt that the UPG101 will be less likely to take a "joke". One must take the same precautions when biasing the UPG101 as when powering any power GaAs FET device.

Conclusion

CEL is excited with NEC's development of these new MMIC's. These devices perform well and have lived up to all our expectations. NEC and CEL would like to invite the user to try these devices for whatever application they may have.

CEL is extremely well staffed with experienced sales persons and supported by a knowledgeable applications engineering group. It is the intention of CEL, together with NEC, to support the user for the successful utilization of all of our products. Should any questions arise concerning these MMIC's or other semiconductor products, please feel free to contact: Applications Engineering, California Eastern Laboratories, 3260 Jay Street, Santa Clara, CA 95054. Telephone: (408)988-3500

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SOLID STATE HF TRANSMITTER FOR OVER-THE-HORIZON (OTH) RADAR

Fuat Agi, Vice President Engineering, M/A-COM MPD
Donald J. Woft, Sr. Vice President, M/A-COM, Inc.

Today there is an ever-increasing number of radar systems, both for new equipments and for improvement upgrades, which utilize solid state (SS) high power amplifiers for the transmitter. SS offers major advantages of high reliability and availability, graceful degradation, low MTTR, logistics and low life cycle cost. A well-designed SS system need never have a system outage due to the loss of the modules since the amplifier is distributed and fails gracefully. Amplifier (modules) building blocks which have failure rates measured in years, have replacement times measured in minutes thus the availability of the system is essentially 100% (approximately 1.0). Repair is often possible on-site with skill levels readily available by service personnel.

To exemplify the advancing state-of-the-art in radar SS transmitters, this paper will describe in some detail HF solid state 200 kW CW transmitter which is applicable in an over-the-horizon radar application.

200KW SS TRANSMITTER

Over-the-Horizon (OTH) Radars are currently planned in several countries for long-range (over 1000 miles) surveillance. These modern OTH systems typically utilize transmitters with 200 kW (CW) or more of power delivered to an array of 10-20 antenna radiators, see Figure 1. Thus, depending on the antenna tapering, the power output to each antenna element is between 5 and 40 kW. These systems utilize the ionosphere to reflect HF energy back to earth, range being a function of the ionosphere characteristics at the time, and the radar operating frequency. A 20 kW solid state transmitter developed for this application is shown in Figure 2. The performance is shown in Table 1 and a block diagram of the 20 kW shelter housing configuration is shown in Figure 3.

TABLE 1.

Frequency Band, Instantaneous	5-28 MHz
(Typical) Power Output, Total	200 kW CW
Antenna Taper	As required in 5, 10, 20 kW increments
Housing	Shelters of 20 kW each
Load VSWR	2:1 Max.
Cooling	Air
Dark Noise	-150 dBm/Hz
Near Carrier Noise	-93 dBc/Hz (2 Hz FM carrier)
Band Switching Time	0.3 sec.
Harmonics	-70 dBc
Phase Linearity	1 degree max. per 100 kHz band

In this way each shelter contains 20 kW of power which can be configured to delivery either 20 kW, 2 times 10 kW or 4 times 5 kW as required by the antenna system. The total system power requirements (over 200 kilowatts) is achieved with an appropriate number of shelters delivering power to the antenna array elements. As can be seen, a basic building block of the 20 kW unit is a 5 kW amplifier housed in each bay; the center bay contains the appropriate combiner, in the case shown in Figure 2 a 4:1 unit to 20

kilowatts. Similarly the 5 kW amplifier is made up of individual power amplifier modules each of which provides 220 watts of output power from a push-pull configuration. Figure 4 is a detailed block diagram of the 5 kW amplifier. The transistors are derated to an average junction temperature of 120 degrees C (150 degrees C worst case) thus assuring excellent reliability. Figure 5 shows the power response of a typical 5 kW and 20 kW amplifier. Each 5 kW amplifier has its own dedicated power supply which has over-capability via redundant modules; thus providing for high reliability/availability on this critical component. BITE is provided to all power levels from the 220 W modules through the full 20 kW level and further includes a full complement of BITE functions. Maintenance is possible to the individual module (225 W) level. This transmitter is now in production at M/A-COM MPD.

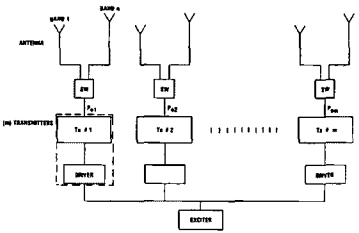
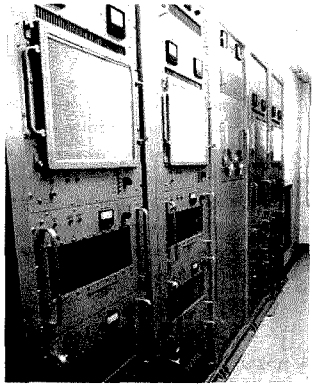


Figure 1. Typical Antenna/Transmitter Array Configuration over the Horizon Radar.

Figure 2.



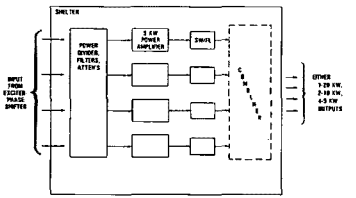

SHELTER
POWER DIVIDER, FILTERS, ATTEN'S
1 KW POWER AMPLIFIER
SWCH
C O M B I N E R
INPUT FROM EXCITER PHASE SHIFTER
OTHER 1-20 KW, 2-10 KW, 4-5 KW OUTPUTS

Figure 3. 20 K Watt Solid-State Transmitter Shelter Architecture.

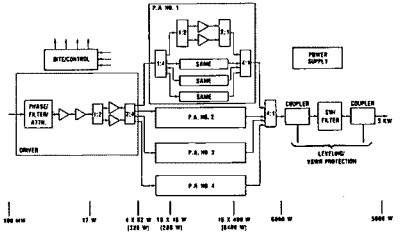


Figure 4. 5 Kilowatt Amplifier Subsystem.

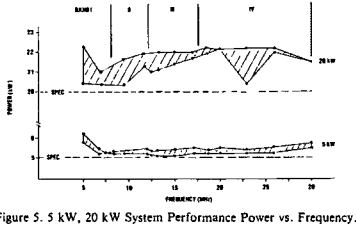


Figure 5. 5 kW, 20 kW System Performance Power vs. Frequency.

AN HF HIGH DYNAMIC RANGE AMPLIFIER USING FEEDFORWARD TECHNIQUES

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ABSTRACT

Feedforward is a distortion cancellation technique in which a sample of the distortion generated in an amplifier is coupled off, isolated, amplified, and recombined 180 degrees out of phase to cancel the remaining distortion in the output signal. This paper describes how feedforward was successfully applied to a three decade bandwidth amplifier (100 kHz to 100 MHz) to achieve a second-order output intercept point greater that +100 dBm, a third order output intercept point greater than +55 dBm, and a noise figure less than 7 dB.

FEEDFORWARD THEORY

A feedforward block diagram is shown in Figure 1. The main signal path is through the main amplifier and delay line 2 to the output. The distortion generated in the main amplifier is the source of the signal degradation and is the distortion which is cancelled by the feedforward circuit.

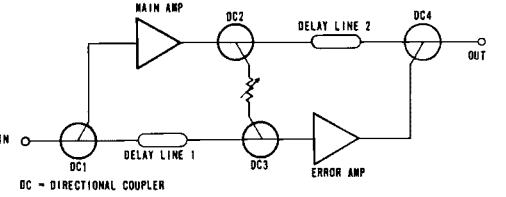

Fig. 1 - Feedforward Block Diagram

Feedforward utilizes a two loop system to accomplish the distortion cancellation. "Loop 1" shown in Figure 2A, can be recognized as the first half of the feedforward block diagram of Figure 1. "Loop 2," shown in Figure 2B, is the second half. Directional couplers are used to sample and recombine the signal and distortion to achieve the desired results.

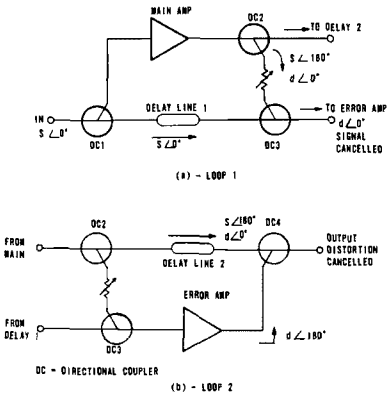

Fig. 2 – Feedforward Loops

To cancel the distortion generated in the main amplifier, it is necessary to isolate the distortion. This is the function of Loop 1 of the feedforward circuit. At the input, the clean signal is coupled off following one path through the main amplifier and the other path through delay line 1. At the output of the main amplifier, a sample of the distorted signal is coupled down to DC3 where it is recombined 180 degrees out of phase with the clean signal from delay line 1. By proper choice of circuit gain and attenuation elements in both paths, the two signals will have equal amplitudes and when combined 180 degrees out of phase the signals will cancel, thereby isolating the distortion. Maximum signal cancellation is desirable not only to obtain a "clean" distortion sample, but also to minimize the input level to the error amplifier so that it does not generate distortion. In addition to strict level control and phase requirements, the time delay of both paths must be equal for cancellation to occur. The delay line is designed to obtain this match.

The distortion cancellation is a function of Loop 2. Here, the isolated distortion at the output of DC3 is amplified by the error amplifier and coupled to the output to recombine with the distorted signal from the main path of the feedforward circuit. As with the cancellation requirements of Loop 1, the distortion from both paths must have good amplitude and delay match, and must be 180 degrees out of phase. Note that the distortion contributed by the error amplifier is insignificant due to the low signal level and so is not a concern.

DESIGN CONSIDERATIONS

AMPLITUDE

To obtain the amplitude match required from both paths of Loop 1 and Loop 2, the losses of the directional couplers and gain of the amplifiers are calculated.

For Loop 1, equal levels from both paths occur at the output of DC3 when the following equation is satisfied. (All gains and losses in dB)

$$S - D1 + G1 - D2 - D3 = S - L1 - DL1 - L3$$

where L# = absolute loss of thru path of DC#

D# = absolute loss of coupled port of DC#

DL1 = absolute loss of delay line 1

G1 = gain of main amplifier

Rearranged, this equation is one of three required for feedforward circuit design:

For signal cancellation:

$$G1 = D1 + D2 + D3 - L1 - L3 - DL1 \qquad 1$$

For Loop 2, the equation for amplitude match is

$$S - L2 - DL2 - L4 = S - D2 - D3 + G2 - D4$$

where L# = absolute loss of thru path of DC#

D# = absolute loss of coupled port of DC#

DL2 = absolute loss of delay line 2

G2 = gain of error amplifier

Rearranging gives the second equation required for feedforward design:

For distortion cancellation:

$$G2 = D2 + D3 + D4 - L2 - L4 - DL2 \qquad 2$$

An additional consideration is the desired gain of the feedforward circuit.

For gain requirements:

$$GAIN = G1 - D1 - L2 - L4 - DL2 \qquad 3$$

The solution to these equations is simplified by several design considerations. For minimum noise figure, DC1 and DC3 should have minimal thru path losses. Minimal loss in the thru paths of DC2 and DC4 is necessary for the highest intercept point. To simplify circuit design, G1 can be set equal to G2 which forces DC1 = DC4 and DC2 = DC3.

PHASE

The phase of the signals can be controlled by choosing appropriate paths through the directional couplers. The circuit diagram of a directional coupler is shown in Figure 3. When a signal enters port 1, the output at port 2 is 180 degrees out of phase with the input, whereas if the signal enters port 3, the output at port 4 is in-phase with the input. By directing the signal in the feedforward circuit through the appropriate port, the required phase is obtained.

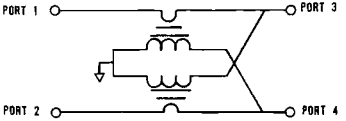

Fig. 3 - Directional Coupler

DELAY

Once the gain of the main and error amplifiers and the coupling coefficients of the directional couplers are chosen, the delay of the main amplifier path of Loop 1 is measured and matched by designing delay line 1 accordingly. Efforts should be made to minimize the delay variation versus frequency of the main amplifier path to simplify the delay line design. Similarly, delay line 2 should be designed to match the delay of the delay line path to the error amplifier path of Loop 2.

CANCELLATION REQUIREMENTS

Figure 4 shows the amplitude and phase match requirements to obtain the desired amount of cancellation. As the chart indicates, 20 dB of cancellation can be obtained with 1 degree of phase match and about 0.9 dB amplitude match. The circuit should have a gain adjustment to adjust the amplitude for a good match and a phase adjustment in the delay lines to attain the delay match. Equalizers and temperature compensation networks are sometimes necessary to obtain more stringent amplitude and phase match requirements.

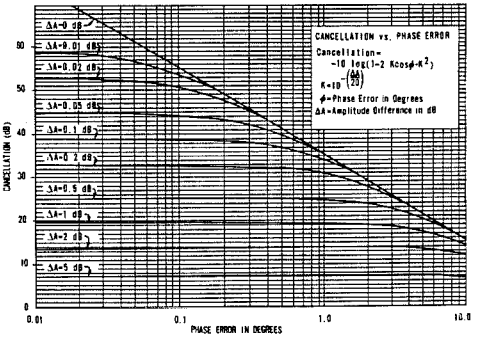

Fig. 4 - Cancellation Requirements

FEEDFORWARD ARCHITECTURE

Other feedforward configurations are possible and should be chosen according to design requirements. Figure 5 shows a configuration commonly used for power amplifiers and is attractive because it requires less gain in the main amplifier than that of Figure 1. The disadvantage of the circuit in Figure 5 is that it has a much higher noise figure. This is due to the fact that feedforward not only cancels the distortion contributed from the main amplifier, but also cancels its noise contribution. This leaves only the error amplifier as the noise source. Since the noise contributed by the error amplifier is the sum of its noise figure and the losses incurred before it, the higher input losses of DC1 in Figure 5 will result in a much higher noise figure.

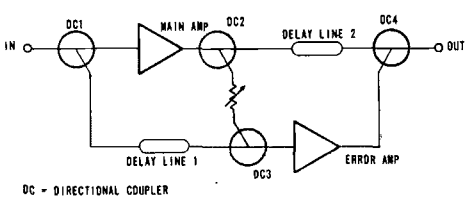

Fig. 5 - Feedforward Power Configuration

HF HIGH DYNAMIC RANGE AMPLIFIER DESIGN

This project was initiated in an effort to design a high performance amplifier suitable for HF multicoupler applications. An HF multicoupler is used at receiver sites to provide multiple outputs from a single receiving antenna and consists of an amplifier driving an n-way splitter. Because of the high concentration of both desired and undesired signals in the antenna environment, a high performance amplifier is required. It must not add excessive noise to weak desired signals nor produce intermodulation products from strong signals. The demands placed on such an amplifier are severe.

Preliminary specifications were established based on these demands and what was considered theoretically possible. A gain of around 11 dB was determined to be necessary to offset the loss of an 8-way split. The goals set for the second and third order output intercept points (OIP2 and OIP3, respectively) were based on the performance of a typical 1 watt bipolar transistor and the estimated distortion cancellation capabilities of push-pull and feedforward techniques. In particular, it was estimated that the OIP2 could be improved 20 dB from push-pull and 20 dB from feedforward and the OIP3 could be improved 3 dB from push-pull and 10 dB from feedforward. From this, the goal of +100 dBm for OIP2

and +57 dBm for OIP3 was established. The noise figure was estimated to be 7 dB: 5 dB from the error amplifier and 2 dB from input losses. With these preliminary specifications, a circuit was built, tuned and tested as described below.

FEEDFORWARD

The feedforward configuration used in the HF high dynamic range amplifier was a modification of that shown in Figure 1 and is shown in Figure 6. Directional couplers DC2 and DC3 are replaced with a single directional coupler to achieve the desired results with fewer parts. A gain adjustment is placed within each loop for independent control of signal levels. With this design, three 14 dB directional couplers are used with main and error amplifier gains of 26.5 dB. This achieves the necessary cancellation in both loops and the desired gain of 11.5 dB.

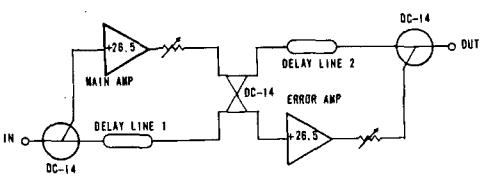

Fig. 6 - Feedforward Circuit

PUSH-PULL

Feedforward is used to cancel distortion generated in the main amplifier by 20 dB and more. However, second order output intercept points greater than +100 dBm and third order output intercept points greater than +57 dBm require a high performance main amplifier. A push-pull arrangement shown in Figure 7 is used to obtain an additional 20 dB of cancellation of the second order intermodulation product and an additional 6 dB of reduction of the third order intermodulation product. Flatness and phase linearity is improved by using 3 dB directional couplers instead of push-pull transformers. In addition, noise figure and intermodulation products are minimized by biasing amps 1 and 2 with Ic = 50 mA and amps 3 and 4 with Ic = 100 mA at +15 V. This design is used for both the main and error amplifiers bringing the total power consumption to 9 watts.

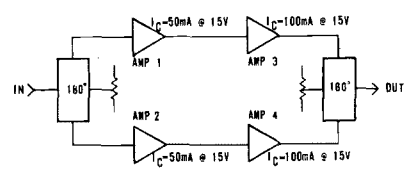

Fig. 7 - Push-Pull Arrangement for Main and Error Amplifiers

RESISTIVE FEEDBACK

The amplifiers in the push-pull arrangement use Motorola's MRF587 1 watt bipolar transistors in a resistive feedback network. Negative feedback techniques are beneficial because they produce flatter gain, lower distortion, better impedance match, and temperature stability. Although resistive feedback results in a higher noise figure (5 dB versus 1.5 dB) and a lower intercept point (by 1-2 dB) than a lossless or coupler feedback network, this compromise was accepted in return for the extended bandwidth that it provided. The resistive feedback amplifier circuits are designed based on a desired gain of +14 dB per stage to bring the total gain in the push-pull arrangement to 26.5 dB. Gain flatness of the push-pull configuration with resistive feedback amplifiers is ±0.1 dB from 100 kHz to 100 MHz with a return loss greater than 20 dB.

TUNING PROCEDURE

Loop 1 and Loop 2 are designed independently and fine-tuned after *integrating* into the final feedforward circuit. The final circuit is tested using resistive coupler test points as shown in Figure 8.

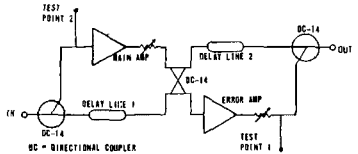

Fig. 8 - Feedforward with Test Points

Tuning the feedforward circuit is performed by using a test signal to simulate the signal that is to be cancelled in Loop 1 and to simulate the distortion that is to be cancelled in Loop 2. Cancellation of each loop is measured separately and requires a reference. For Loop 1, a reference is set up by disconnecting the main amplifier and sweeping from the input through the delay line 1 path to test point 1. Then, with the main amplifier in the circuit, the cancellation is measured by sweeping across Loop 1 from the input to test point 1. Amplitude and delay adjustments should be made to improve the match for maximum cancellation. Similarly, the cancellation of Loop 2 is measured by disconnecting the error amplifier and injecting a test signal into test point 2 through the delay line 2 path to the output to obtain the reference. Then, with the error amplifier in the circuit, the response of Loop 2 from test point 2 to the output is measured and tuned for maximum cancellation.

RESULTS

Test results of the specified HF high dynamic range amplifier indicate success in attaining the specifications set forth. Figure 9 shows the cancellation curves of Loop 1 and Loop 2. As can be seen, better than 30 dB of cancellation of both signal and distortion was attained across most of the three decade bandwidth from 100 kHz to 100 MHz. The gain and return loss curves, shown in Figure 10, indicate a flat response with 11.5 $\pm$0.5 dB of gain and return loss better than 18 dB across most of the band. Figure 11 is a plot of the calculated intercept points with and without feedforward based on the intermodulation measurements of a two-tone test. The OIP2 was 10 dB higher than the expected +100 dBm due to the 30 dB of cancellation obtained from feedforward rather than the anticipated 20 dB. The OIP3 was better than the expected +57 dBm across most of the band. The noise cancellation effects are presented in Figure 12. With feedforward, the noise figure was below the 7 dB specification.

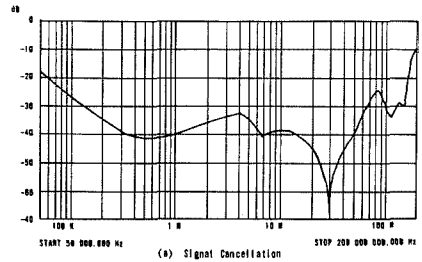

Fig. 9 - Cancellation (Model RF 1960A)

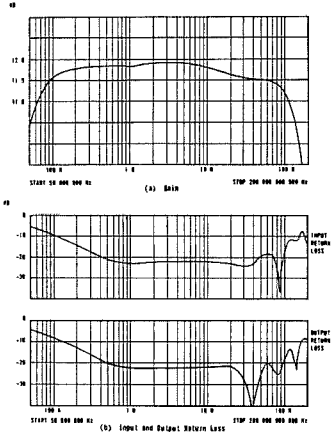

Fig. 10 - Response (Model RF 1960A)

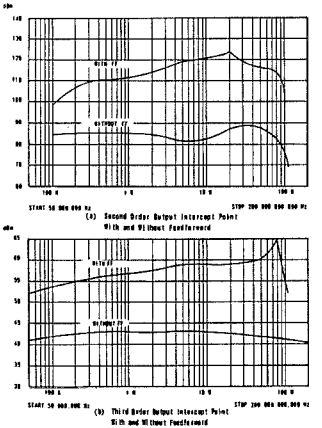
(a) Second Order Output Intercept Point With and Without Feedforward
(b) Third Order Output Intercept Point With and Without Feedforward

Fig. 11 - Output Intercept Points (Model RF 1960A)

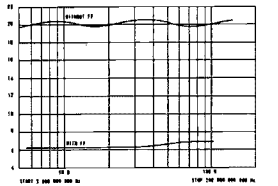

Fig. 12 - Noise Figure With and Without Feedforward

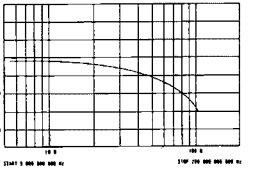

Fig. 13 - 1 dB Compression Point (Model RF 1960A)

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1. H. Seidel, "A Microwave Feed-Forward Experiment," Bell System Technical Journal, Vol. 50 Nov. 1971, pp. 2879-2916.

2. J. Dixon, "A Solid State Amplifier with Feedforward Correction for Linear Single-Sideband Applications," IEEE International Conference on Communications 1986, Ch 2314-3/86/0000-0728.

RESEARCH REPORT

ON

COAXIAL CABLE LEAKAGE

AUGUST 1985

DELTA ELECTRONICS, INC.
5730 GENERAL WASHINGTON DRIVE
ALEXANDRIA, VIRGINIA 22312

Author: Brian E. Shreve.

Contrary to popular belief, coaxial cable exhibits leakage of electromagnetic energy from its shield at greater than negligible levels. This report is a compilation of research initiated to determine the severity of the leakage of coaxial cable in the frequency range 2 to 30 MHz. Several types of cable, experimental and analytical methods, and numerical results are discussed.

Shielding effectiveness of a coaxial cable is the ratio of the magnetic or electric field intensity without the shield to the field intensity with the shield in place. Analytic methods and laboratory experiments yield an approximate value for shielding effectiveness but the actual realized shielding is dependent on numerous factors, some indeterminable quantitatively, such as physical orientation and installation of the cable, and the effect of neighboring objects and connections.[1]

Several methods exist to predict and determine shielding effectiveness of braided shield coaxial cable. The surface transfer impedance concept is very useful for predicting the limits of shielding effectiveness. Treating the gaps between the conductors of the braided shield as radiating aperatures yields a model at the expense of tedious mathematics. Direct measurement methods include a triaxial apparatus to measure the RF voltage and current on the shield as a function of frequency, relative measurements between cables, and absolute measurement of the field in a shielded room using calibrated antennas.

Surface transfer impedance may be thought of as the impedance through the shield of a coaxial cable. For solid metal shields energy is transferred via the diffusion transfer impedance, Z_t. It has been shown that the complex impedance Z_t can be computed for solid shields using the

equation6,8

$$Z_t = \frac{2R_{dc}(t/d)}{\sqrt{\sinh^2(t/d) + \sin^2(t/d)}} \angle 45^\circ - \arctan(\coth(t/d)\tan(t/d)) \quad (1)$$

where:
Z_t = transfer impedance through the shield in ohms/meter
R_{dc} = DC resistivity of the shield in ohms/meter
t = thickness of shield
d = skin depth, or field penetration into the shield in meters
$d = \sqrt{\rho/3.1415fu}$
ρ = dc resistivity of shield in ohms/meter
f = frequency in Hz
u = absolute magnetic permeability of shield material in H/m

At low frequencies the skin depth is so large that the transfer impedance is essentially the dc resistivity of the shield.

The parameters required in Equation 1 are readily found and a numerical solution computed for solid shields. This yields a method by which measurement techniques can be judged.

Surface transfer impedance can be measured directly by causing a known current to flow through the length of the shield and measuring the voltage drop across the shield. Alternately a known voltage can be impressed across the shield and the resulting current flow measured. Accurate measurements depend on a well shielded enclosure for the test sample, accurate instrumentation and methods to measure RF voltage and current, shielding the cables to the measurement instrumentation, careful RF grounding of the test fixture and instrumentation, and care in making connections at the ends of the cable to prevent end effects from dominating the results. Smith[8], DeLorenzo[2], Simons[7], and Salt[6] have documented triaxial testers where the coaxial cable under test forms the the inner two conductors of the triaxial arrangement. The outer conductor of the test apparatus is solid to contain nearly all the energy within the fixture and prevent external fields from tainting the results.

Comparisons between values of the surface transfer impedance calculated using Equation 1 and measured values have been made using solid shield coaxial cable. The good agreement between the values gives confidence in the validity of the direct measurement technique using triaxial testers.2

The discussion of computational methods thus far has been limited to solid shields since the surface transfer impedance equation variables are readily found and solutions simple. These computations can be used to derive minimum radiation limits or maximum shielding effectiveness values for braided shields. Braided shields exhibit the diffusion transfer impedance of Equation 1 with t being equal to the braid wire diameter. Additionally, the gaps between the wires act as an array of electric and magnetic dipoles. Thus inductive (magnetic) coupling and capacitive (electric) coupling allows the fields within the coax to penetrate the shield. Cable eccentricity additionally contributes primarily to the magnetic coupling as detailed by Fowler.[3] Each of the gaps in the braid thus acts as a waveguide to transfer some of the energy from the inside of the cable to the outside. Alternately, the gaps in the braided shield can be thought of as discontinuities in a solid shield which the RF current must flow around thus producing higher field strengths than those generated by the continuous shield. Exhaustive mathematical modeling of the dipole array created by the gaps in the braid has been performed by Ikrath[4] and Vance[9]. Fowler[3] further models the effects of cable eccentricity, intershield resonance in multi-shield cable, and shield termination methods. He further proves that these effects can generate additional coupling on the same order of magnitude as the transfer impedance calculated solely from braid parameters. These models require several physical parameters of the

braid and cable to be determined in order to generate accurate computed results. Such information is not readily available thus this method of determining the shielding effectiveness of coaxial cable was not persued. Moreover, the physical orientation and installation of the cable can greatly affect the parameters of the model such as the spacing between the gaps in the braid, the size of the gaps in the braid, and the angular orientation of the braid wires with respect to the field within the cable.

Smith[8] presents a comparison of computed and measured surface transfer impedance impedance of RG-59/U cable. The impedance is composed of diffusion, inductive, and capacitive transfer impedance components. An error of approximately 50% in the computed values of the transfer impedance components resulted revealing the difficulty of determining the physical parameters of the shield braid to generate an accurate model.

The information needed to make accurate calculations of the surface transfer impedance of a coaxial cable shield is difficult to obtain thus limits were calculated and direct measurements made of shielding effectiveness.

To determine the merits of double shielding, a comparison of single shielded versus double shielded cable was executed. For this comparison, single shield RG-59/U and double shield RG-223/U coaxial cable was used. The test is illustrated in Figure 1. A 50 ohm stripline was constructed to act as a radiating antenna. The stripline, terminated in 50 ohms, was then driven by the RF source in the network analyzer. The coaxial cable under test terminated in its characteristic impedance of 50 ohms was placed on top of the stripline and the energy leaking through the shield measured. Since the field near the stripline is very high and all fields must pass through the shield of the coax, interfering sources are attenuated greatly before reaching the detector, thus more accurate measurements can be made than if the minute energy emanating from the coax shield had been collected by the unshielded stripline. The results indicate an approximate 10 to 14 dB of shielding effectiveness is gained by adding the second shield. The quantity is approximate since some of the measurements were made very near the noise floor of the detection system. These measurements are relative and serve only to allow comparisons between cables. In order to determine the actual shielding effectiveness, field strength measurements must be made.

To carry out field strength measurements on double shield RG-214/U coaxial cable the antenna of Figure 2 was constructed. A receiver/generator was used as an excitation source and detection system. The cable, terminated in 50 ohms, was suspended from the ceiling in the center of the lab and driven by 10 Vrms (2 Watts) from the generator. The antenna was then used to probe the resulting field from all points on a 1 meter radius from the cable to locate and measure the maximum radiation for each test frequency. Figure 3 illustrates the test conditions and the data collected. A possible source of error in this measurement is the fact that the data was collected in an unshielded laboratory inside a steel framed building. Reflections, standing waves, RFI sources within the building and antenna VSWR contribute to the error in the measurements. However, the 100 dB shielding effectiveness derived from the measured field strength is the proper order of magnitude based on conversations with engineers at cable manufacturing facilities.[5]

To minimize sources of error and in an attempt to generate reproducible test conditions, practical field strength measurements were made on RG-214/U cable using the shielded room, calibrated EMI measurement instrumentation, and technical expertise at Honeywell Signal Analysis

Center, Annapolis, Maryland. The test conditions are illustrated in Figure 4. Two 10 feet long pieces of RG-214/U were placed in the shielded room. The cables were connected together with a female to female N-type connector. Power from an RF power amplifier outside the shielded room provided the RF excitation for the test. A dummy load also outside the shielded room was used to terminate the coaxial cable under test. All connections in and out of the room were through bulkhead N-type connectors in the wall of the shielded room. Figure 5 illustrates the emissions measured at a distance of 1 meter from the two 10 feet lengths of RG-214/U at power levels of 10 watts and 100 watts. Theoretically the curves should always be separated by exactly 10 dB. However, the spectrum analyzer detection system plotter did not sample at identical frequencies for each of the power levels introducing differences in the shapes of the curves which are straight line segments between data points. Evidence of this effect is particularly evident in areas of the curves exhibiting high slopes or near maxima and minima of the curves. For example, a data point was plotted at 10 MHz for the 100 watt level but not for the 10 watt level. The slope is so large near 10 MHz that it appears the 10 watt curve does not track the 100 watt curve due to the error introduced by interpolating between data points on a rapidly changing curve. Taking sampling points into account, the areas of the curves with gradual slopes, particularly in the 2 to 5 MHz region, exhibit the 10 dB difference in field strength. Thus, if enough points are sampled to allow a smooth curve to be drawn between the data points without missing the extrema of the curves, emissions for any power level can be predicted. Figure 6 includes a third curve indicating the predicted emission level for a 1 KW signal based on the measured 100 W curve.

In an effort to obtain a numerical value for the surface transfer impedance of RG-214/U cable in order to calculate shielding effectiveness and thus emissions limits, Leonard Visser of the Belden Wire and Cable Research Center was contacted. Mr. Visser is in the process of measuring the surface transfer impedance of the complete line of coaxial cable produced by Belden. When contacted on June 11, 1985 he had not yet measured RG-214/U cable. However, his familiarity with the properties of similar coaxial cable already tested allowed him to estimate the surface transfer impedance to be in the range of 0.1 to 10 millichms per meter over the frequency span of 2 to 30 MHz.[10]

Subsequently, Mr. Visser tested RG-214/U on July 9, 1985. The magnitude of the surface transfer impedance he measured over the frequency range 10 KHz to 500 MHz is illustrated in Figure 7. At 10 KHz the surface transfer impedance is essentially the DC resistivity of the coax shield or 4.6 millichms per meter. The impedance reaches a minimum value (maximum shielding effectiveness) at 2 MHz and then increases with frequency.

Figure 8 illustrates the shielding effectiveness of double shield RG-214/U, single shield, triple shield, composite shield, and standard 0.012 inch thick solid copper shield semi-rigid coax. Shielding efficiencies were calculated from Figure 7 data for RG-214/U; from surface transfer impedance data presented in the Handbook of Wiring, Cabling, and Interconnecting for Electronics for single, triple, and composite shields; and from the surface transfer impedance calculated from Equation 1 for 0.012 inch thick copper. Note that the triaxial composite shield cable consisting of a copper braid over a steel braid over insulation over another copper braid is superior to 0.012" thick solid copper at low frequency. This effect is attributable to the greater net thickness of the shield and reduction of

the surface transfer impedance by the high initial permeability of the ferromagnetic steel braid as analyzed by Salt.[6] The three copper braids shield is superior as well as the net thickness of the three copper braids is also greater than 0.012 inch. At higher frequencies the capacitive component of the transfer impedance dominates and the shielding effectiveness decreases for both the three copper braids and the composite shield while the solid shield shielding effectiveness increases dramatically with the decreasing skin depth at higher frequencies. Also note that the shielding effectiveness of double shield coaxial cable is roughly 12 dB greater than that of the single shield with 90% coverage which agrees with the data derived from the comparative measurements previously discussed.

Figure 9 illustrates the electric field intensity generated by a 1 meter length of each cable carrying 1 KW measured at a distance of 1 meter, calculated from the shielding effectiveness curves of Figure 8 using the near field tangential electric field intensity equation for a current filament:

$$E_t = 30\alpha^2 L I \sin\theta A_t \cos(\nu + \phi_t) \qquad (2)$$

where:

$A_t = [1-(\alpha r)^2 + (\alpha r)^4]/(\alpha r)^3$
L = length of current filament
λ = wavelength
I = current
θ = angle
r = distance from current filament
$\alpha = 2\pi/\lambda$

It is evident from the data presented in Figure 9 that electromagnetic leakage at frequencies less than 10 MHz is not negligible. Approaching the question of leakage from practical viewpoint; the power that can be carried by a 1 meter length of RG-214/U without exceeding the emission limit of Figure 9 in the range 2 to 30 MHz was calculated. Incredibly, the maximum power is less than 500 microwatts.

The results of this research indicate that computational methods are good for establishing limits of shielding effectiveness and thus the level of leakage that can be expected from a coaxial cable. Practical measurements in the actual installation environment are very difficult due to interfering sources of RFI, the dependence of the measurement of the radiated fields on physical orientation of the cable, reflections and absorption of the RF energy from nearby objects and location of the measurement antenna. As shown by Simons[7] there is not good correlation between calculated and measured emissions due to these effects. Even field strength measurements made in shielded rooms are subject to the errors produced by reflections and standing waves present in such chambers. The shielded room also does not adequately simulate the actual installation of the cable.

The results of the predicted leakage calculations and actual measurements of electric field leakage from coaxial cables presented in this report are shocking when compared with the emissions limits imposed by the various standards. At modest power levels below 10 MHz, even certain types of solid shield coax do not provide adequate shielding to hold emissions below mandated limits. Fortunately, coaxial cable manufacturers have become cognizant of the engineer's need to have shielding effectiveness data in order to design equipment and systems to meet electromagnetic emissions standards and are in the process of making the data available to the RF design engineer in the form of surface transfer impedance measurements.

Shielding effectiveness calculations, used with a conservative safety margin, can prevent surprises in the EMI test lab and hold RFI in the equipment operating environment to safe levels.

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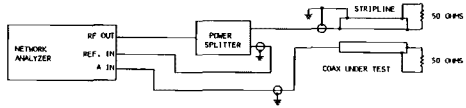


FIGURE 1

COMPARATIVE SHIELDING EFFICIENCY MEASUREMENT

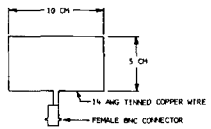
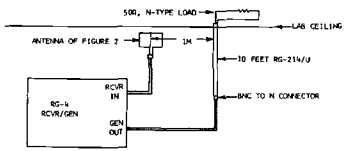


FIGURE 2

ANTENNA FOR FIELD MEASUREMENT



FREQUENCY, MHZ	SHIELDING EFFECTIVENESS, DB
12	103.3
13	101.6
14	100.0
15	99.3
16	93.3
17	89.9
18	81.6
19	88.4

FIGURE 3

RG-214/U LEAKAGE MEASUREMENTS

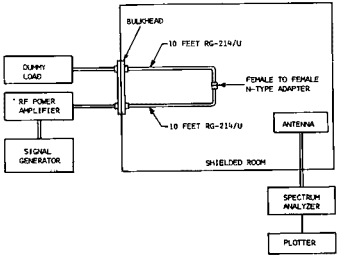
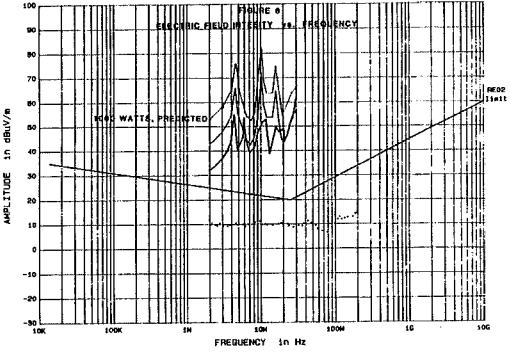
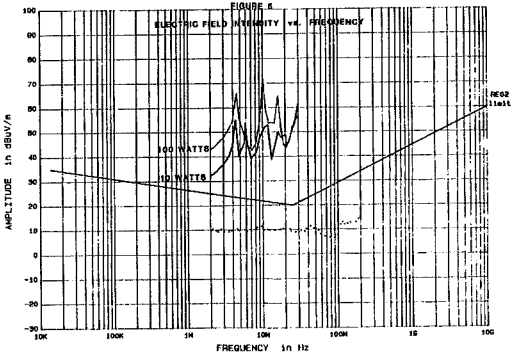
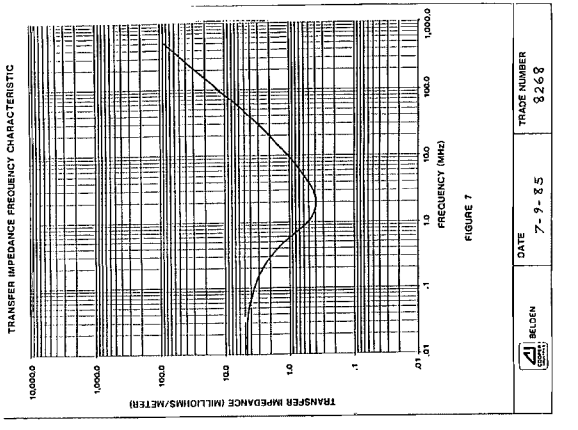


FIGURE 4

SHIELDED ROOM FIELD STRENGTH MEASUREMENTS







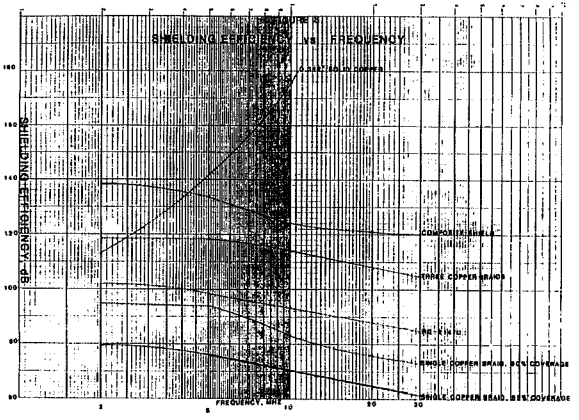


FIGURE 5
SHIELDING EFFICIENCY vs. FREQUENCY
SHIELDING EFFICIENCY, dB
FREQUENCY, kHz
.032" SOLID COPPER
COMPOSITE SHIELD
THREE COPPER BRAIDS
RG-214/U
SINGLE COPPER BRAID, 90% COVERAGE
SINGLE COPPER BRAID, 85% COVERAGE

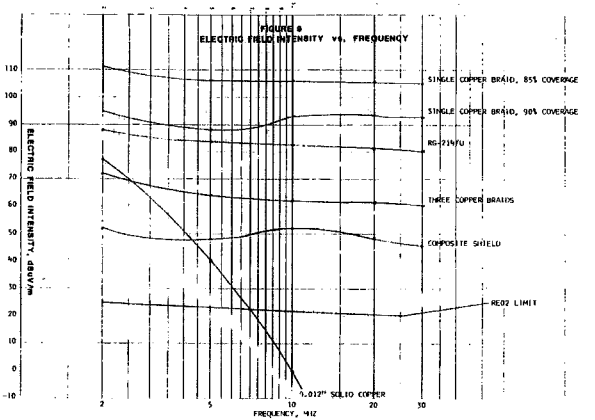


FIGURE 6
ELECTRIC FIELD INTENSITY vs. FREQUENCY
ELECTRIC FIELD INTENSITY, dBuV/m
FREQUENCY, kHz
SINGLE COPPER BRAID, 85% COVERAGE
SINGLE COPPER BRAID, 90% COVERAGE
RG-214/U
THREE COPPER BRAIDS
COMPOSITE SHIELD
RE02 LIMIT
.012" SOLID COPPER

DESIGN AND ANALYSIS OF FOURTH AND FIFTH ORDER INDIRECT SYNTHESIZER LOOPS

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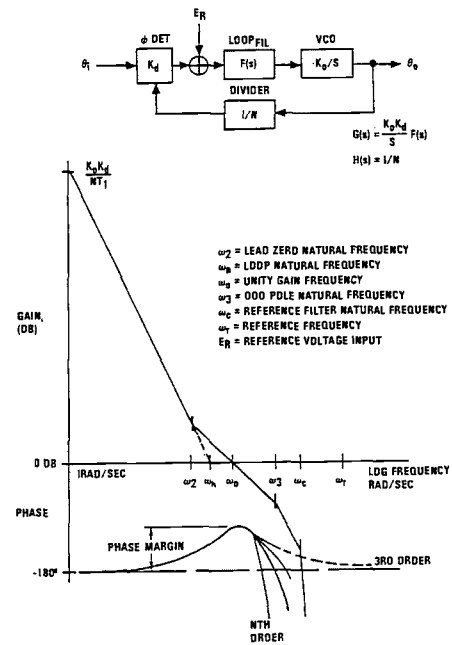
Phase locked loops are applied extensively as indirect frequency synthesizers. Most design techniques draw on the vast array of control system theory, particularly second order systems as described by Gardener[1] and others and the third order system of Przedpelski.[2]

Many applied systems are of higher order due to spurious poles contained in loop components or filtering added to suppress the loop reference frequency sidebands. This paper presents techniques which allow design of systems with four or more poles by compensation of a three pole starting point.

The basic phase locked loop is shown in Figure 1 with a typical BODE plot. Dynamic performance is determined by the design of the loop filter. Oscillator phase noise suppression and transient response are typical design drivers. Two open loop response poles occur due to the VCO at zero frequency and the loop integrator pole, usually modeled at zero frequency. The remaining poles are contained in the loop filter and as spurious poles in other components. Setting values for the loop components to

FIGURE 1. THE BASIC PLL AND ITS BODE PLOTS



produce a desired response is the goal of the design process. Several critical frequencies are defined on the BODE plot. Of the six shown ω_o and ω_r , are usually fixed by tuning step requirements and VCO phase noise suppression or tuning speed requirements. This leaves ω_2, ω_3 and ω_c as variables to set other performance parameters.

SPURIOUS POLES

Spurious poles are those that occur in various components usually not by design, but due to some component limitation. These Poles are not contained in the simple loop model, but do influence actual hardware performance. A typical spurious pole occurs due to the finite gain of real operational amplifiers. Figure 2 shows a loop filter with its spurious pole due to limited high frequency gain. This pole at $10\,\omega_o$ will reduce loop phase margin by 5.7 degrees. Such poles can be included in the loop design using a compensation technique.

REFERENCE SIDEBAND FILTERS

Another difference between model and hardware occurs in the use of multi-pole filters to reduce the reference frequency sidebands. These sidebands are caused by the reference frequency

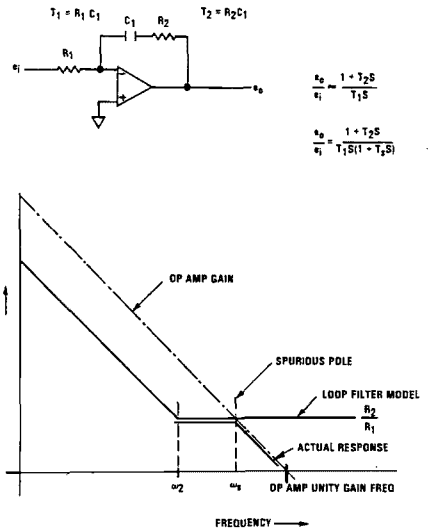


FIGURE 2. LOOP FILTER SPURIOUS POLE GENERATION

output of the phase detector reaching the VCO input. Filters added to reduce the sideband level are often used, but not included in the design equations. This results in a difference between calculated and actual performance due to reduced phase margin and unity gain frequency. The detailed loop model of Figure 3 shows a typical reference filter and fifth order loop configuration.

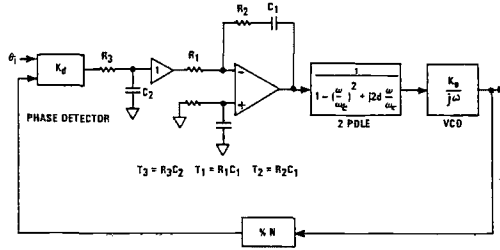


FIGURE 3. DETAILED LOOP MODEL

REFERENCE SIDEBAND LEVEL

The loop reference frequency must be several times greater than the unity gain frequency if linear continuous data analysis is to be valid. With loop gain at ω_r much less than one, the gain from phase detector to VCO output is essentially the forward gain of the loop. With a given static phase error, reference sidebands are evaluated as shown in Figure 4 for phase detectors with logic level outputs.

The input signal at ω_r consists of the fundamental component of the pulsed output of the phase detector. This is 2 times the pulse duty cycle times the peak output voltage. This voltage is filtered by F(s), the loop filter, and applied to the VCO producing phase modulation of K_o/ω_r radians per volt. If this modulation is small, less than six degrees, the sidebands will be 20 log $\Delta\theta/2$ dB below the VCO output. Output pulse width for a given static error

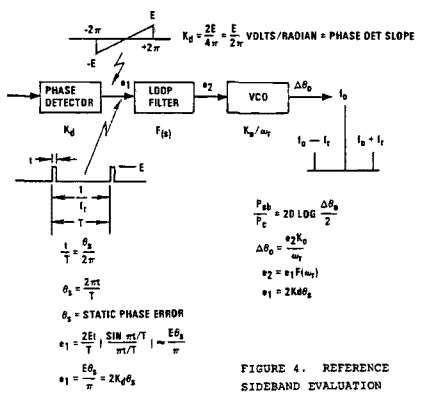


FIGURE 4. REFERENCE SIDEBAND EVALUATION

is dependant on phase detector configuration. The popular phase - frequency detectors such as the Motorola MC4044 produce a pulse width approaching a constant of 10 to 20 nanoseconds at zero phase difference. Given the pulse width and loop filter characteristics, the sideband level can be determined and the filter requirements established. As the unity gain frequency ω_o and reference frequency ω_r become closer the suppression of the sidebands may require complex filter circuits. If the complex filters poles are known, the suppression can be calculated as shown in Figure 5.

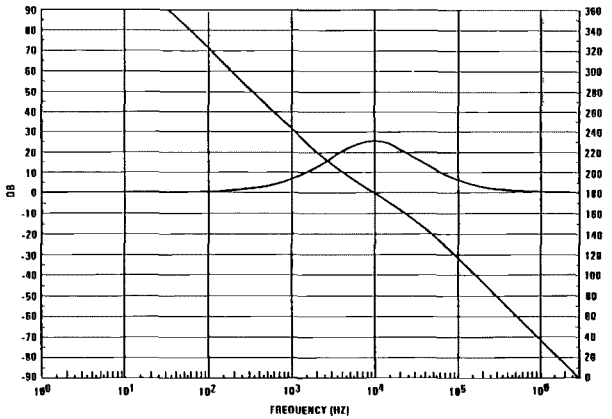
THIRD TO FIFTH ORDER COMPENSATION TECHNIQUE

A third order loop is designed for optimum phase margin by locating unity gain and minimum phase at the same frequency. Figure 6 shows a BODE plot for an optimum loop. This is a good choice for tunable synthesizers since the phase margin has small variation with variable divider ratio N. This optimum can be closely approached for higher order loops by a compensation process. As the additional poles reduce gain and increase phase at the desired ω_o the loop filters T_1 and T_3 can be modified to maintain near optimum conditions. This procedure is quite successful for large separations between ω_o and ω_c, the filter cut frequency, and remains useful, but not optimum as ω_c approaches ω_o.

LOOP ORDER	REFERENCE FREQUENCY GAIN
2ND	$20 \log \frac{\omega_o}{\omega_r}$
3RD	$20 \log \frac{\omega_o}{\omega_r} + 20 \log \frac{\omega_3}{\omega_r}$
4TH	$20 \log \frac{\omega_o}{\omega_r} + 10 \log \left(\frac{1}{\left(1 - \left(\frac{\omega_c}{\omega_r}\right)^2\right)^2 + \left(2d \frac{\omega_c}{\omega_r}\right)^2} \right)$
5TH	$20 \log \frac{\omega_o}{\omega_r} + 20 \log \frac{\omega_3}{\omega_r} + 10 \log \left(\frac{1}{\left(1 - \left(\frac{\omega_c}{\omega_r}\right)^2\right)^2 + \left(2d \frac{\omega_c}{\omega_r}\right)^2} \right)$
NTH N EVEN	$20 \log \frac{\omega_o}{\omega_r} + \sum_{F=3}^{N-2} 10 \log \left(\frac{1}{\left(1 - \left(\frac{\omega_{cF}}{\omega_r}\right)^2\right)^2 + \left(2d_F \frac{\omega_{cF}}{\omega_r}\right)^2} \right)$
NTH N ODD	$20 \log \frac{\omega_o}{\omega_r} + 20 \log \frac{\omega_3}{\omega_r} + \sum_{F=4}^{N-3} 10 \log \left(\frac{1}{\left(1 - \left(\frac{\omega_{cF}}{\omega_r}\right)^2\right)^2 + \left(2d_F \frac{\omega_{cF}}{\omega_r}\right)^2} \right)$

FIGURE 5. REFERENCE FREQUENCY GAIN VERSUS LOOP ORDER

FIGURE 6. BODE PLOT FOR AN OPTIMUM 3rd ORDER LOOP



This procedure maintains constant phase at ω_o by moving T_3 to a value which reduces its phase shift by that of a two pole filter with a given cut-off frequency and damping factor. The loop may be designed from parameters of the third order loop plus two, ω_c and d, for the filter. Any two poles, including two isolated spurious poles can be defined by a natural frequency ω_c and a *damping factor* d.

Figure 7 gives the design equations for third and fifth order loops. An open loop pole zero plot on the S-plane is shown in Figure 8. Here the path of two complex poles moves on constant d radials toward the origin as the ω_3 pole moves toward infinity on the negative real axis. As the real parts of the poles near equality, they become 3 pole filters with familiar names such as Butterworth, Bessel or Chebyshev. These pole locations can be normalized to the ω_3 values as shown in Figure 9. As ω_c is decreased beyond this point ω_3 moves very rapidly, due to its relatively low phase slope at ω_o, and the compensated five pole model finally fails as ω_3 goes to infinity. Now the loop becomes fourth order. This condition can be used to define a near optimum fourth order loop consisting of a second order loop plus a two pole reference filter.

FIGURE 7.

DESIGN EQUATIONS FOR THIRD AND FIFTH ORDER LOOPS

THIRD ORDER

$$T_{33} = \frac{1}{\omega_0}(\text{SEC}\,\phi_m - \text{TAN}\,\phi_m)$$

$$T_{23} = \frac{1}{\omega_0^2 T_{33}}$$

$$T_{13} = \frac{K_0 K_d}{N\omega_0^2}\left(\frac{1+\omega_0^2 T_{23}^2}{1+\omega_0^2 T_{33}^2}\right)^{1/2}$$

FIFTH ORDER

$$T_{35} = \frac{1}{\omega_0}\text{TAN}\left[\text{TAN}^{-1}(\text{SEC}\,\phi_m - \text{TAN}\,\phi_m) - \text{TAN}^{-1}\left(\frac{2d\omega_0/\omega_c}{1-\omega_0^2/\omega_c^2}\right)\right]$$

$$T_{25} = \frac{1}{\omega_0(\text{SEC}\,\phi_m - \text{TAN}\,\phi_m)}$$

$$T_{15} = \frac{K_0 K_d}{N\omega_0^2}\left(\frac{1+\omega_0^2 T_{25}^2}{1+\omega_0^2 T_{35}^2}\right)^{1/2}\left(\frac{1}{\left(1-\frac{\omega_0^2}{\omega_c^2}\right)^2+\left(2d\frac{\omega_0}{\omega_c}\right)^2}\right)^{1/2}$$

T_{nm} = Nth TIME CONSTANT OF AN M POLE LOOP
K_0 = VCO GAIN
K_d = PHASE DETECTOR GAIN
N = DIVIDER RATIO
ω_0 = UNITY GAIN FREQUENCY
ϕ_m = PHASE MARGIN
ω_c = NATURAL FREQUENCY OF TWO POLE REFERENCE FILTER
d = DAMPING FACTOR OF TWO POLE REFERENCE FILTER

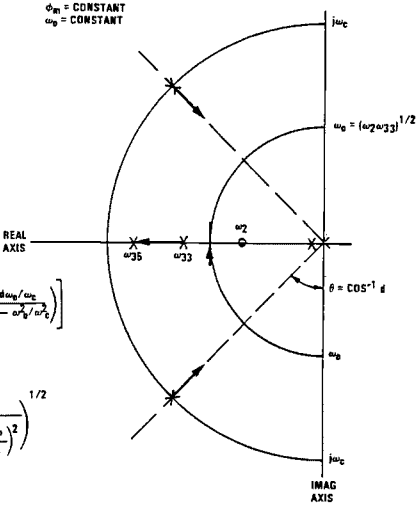


FIGURE 8. OPEN LOOP POLE ADJUSTMENT FOR THE 5th ORDER COMPENSATION WITH CONSTANT d

POLE CONFIG	OPEN LOOP: DAMPING FACTOR	OPEN LOOP: ω_c/ω_3	CLOSED LOOP: ϕ_m	CLOSED LOOP: G_m	CLOSED LOOP: ω_r REJ AT $9\omega_0$
BESSEL	0.75	0.94	40°	11.7 DB	34 DB
			50°	15.1 DB	29 DB
			60°	17.8 DB	25 DB
BUTTERWORTH	0.50	1.0	40°	10.5 DB	37 DB
			50°	12.8 DB	31 DB
			60°	15.4 DB	24.7 DB
CHEB 3 DB	0.16	3.0	40°	16.9 DB	27.4 DB
			60°	18.2 DB	19 DB
			60°	21.1 DB	21.3 DB

ϕ_m = PHASE MARGIN
G_m = GAIN MARGIN

FIGURE 9. 5th ORDER LOOPS WITH SOME COMMON FILTER POLE CONFIGURATIONS

FOURTH ORDER DESIGN TECHNIQUE

A fourth order loop occurs when T_3 goes to zero using the fifth order compensation technique. At this point the two pole filter has the same phase shift as the ω_3 pole in the third order loop.

This condition can be used to derive the filter characteristics for a fourth order loop. Figure 10 shows this process starting with the condition that $T_3 = 0$ and T_2 set at the third order starting point. The resulting design equations show the ratio of filter cutoff frequency to unity gain frequency set by the phase margin and filter damping factor. Figure 11 plots frequency ratio and gain margin as a function of phase margin and damping factor. Relative pole locations for this configuration are shown in Figure 12 with the progression of ω_3 from its third order position at ω_{33} through the fifth order ω_{35} range to infinity, which produces the fourth order loop. Constant phase margin and unity gain frequency are maintained by the design equations.

GAIN MARGIN

Gain margin is the open loop loss at the frequency where open loop phase equals 180°. Second and third order loops have infinite gain margins. Their loop gains can be increased indefinitely

FIGURE 10.

FOURTH ORDER LOOP AS A LIMIT FIFTH ORDER LOOP

1. 5TH $T_3 = T_{35} = \frac{1}{\omega_0} \text{TAN} \left[\text{TAN}^{-1}(\text{SEC } \phi_m - \text{TAN } \phi_m) - \text{TAN}^{-1} \left(\frac{2da}{1 - a^2} \right) \right]$
2. 4TH $T_3 = T_{34} = 0$
3. $\text{SEC } \phi_m - \text{TAN } \phi_m = \frac{2da}{1 - a^2}$
4. LET $\text{SEC } \phi_m - \text{TAN } \phi_m = K$
5. FROM 3

   $K = \frac{2da}{1 - a^2}$
6. SOLVING FOR a

   $a = -\frac{d}{K} \pm \left(\frac{d^2}{K^2} + 1 \right)^{1/2}$

GIVING THE FOLLOWING DESIGN EQUATIONS

$$T_{14} = \frac{K_0 K_d}{N \omega_0^2} \left(\frac{1 + 1/K^2}{(1 - a^2)^2 + (2da)^2} \right)^{1/2}$$

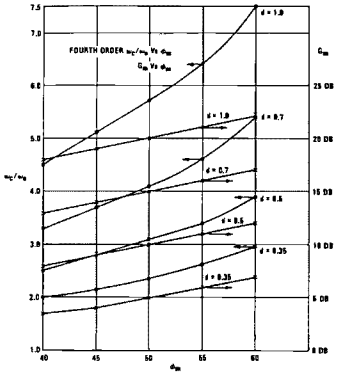
$K = \text{SEC } \phi_m - \text{TAN } \phi_m$

$T_{24} = 1/\omega_0 K$

$$\frac{\omega_c}{\omega_0} = \frac{1}{a} = \frac{1}{\left(\frac{d^2}{K^2} + 1 \right)^{1/2} - \frac{d}{K}}$$

ω_0 = UNITY GAIN FREQUENCY
ϕ_m = PHASE MARGIN
$a = \omega_0 / \omega_c$
ω_c = NATURAL FREQ OF TWO POLE FIL
d = DAMPING FACTOR OF TWO POLE
$T_{n,m}$ = Nth TIME CONSTANT OF AN Mth ORDER LOOP

FIGURE 11.



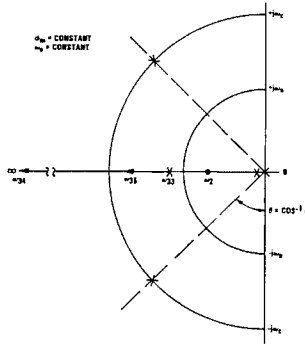


FIGURE 12. OPEN LOOP POLE LOCATIONS FOR THE 4th ORDER LOOP RESULTING FROM $T_{35} = 0$

without instability. Such loops do not occur in real systems due to the spurious poles discussed above. Loops of order greater than three have a finite gain margin. It is readily determined from the BODE plot for a given loop. The compensation technique does not control gain margin nor does it insure stable operation of all fourth and fifth order loops. As the high frequency poles move lower in frequency the 180 degree phase response moves downward and gain margin falls. Underdamped poles (d<1) aggravate this situation by increasing gain with frequency. This effect, shown in Figure 11, produces fourth order loops using d less than .3 with small or negative gain margin (oscillators). Fifth order loops with the pole arrays of Figure 9 have good to excellent gain margins.

MORE POLES

This compensation technique produces excellent results for small loop modifications which occur for high frequency spurious poles. As the complexity of the filter increases or it moves lower in frequency the resulting phase slope will move the phase minimum away from unity gain producing non-optimum loops. Decreasing gain margins will also produce unacceptable loops even when phase margin remains high. To date the process has not been applied beyond the five pole loops discussed here. In the above technique the optimum

loop condition was taken as equal frequency for unity gain and minimum phase. If this is not optimum for a given condition the design process can begin with any reasonable value for ω_2 rather than that of the "optimum" third order loop. One choice might be the 1/f phase noise break point for a particular VCO. Lowering ω_2 will allow more complex filtering at the expense of "optimum" phase conditions.

DESIGN EXAMPLES

The utility of this technique can be tested by application to to some typical loop designs. Figure 6 is the BODE plot of an optimum third order loop with phase margin of 50°. This loop has a unity gain frequency of 10 KHz and a reference frequency of 250 KHz. Reference suppression is 47 dB. (Reference suppression is taken as gain at ω_r and does not account for N.) Figure 13 shows the effect of two spurious op amp poles at 100 KHz. Phase margin is 38 degrees rather than 50. Unity gain frequency is 9.9 KHz and gain margin is 13 dB. Figure 14 is the same loop designed as fifth order with the compensation equations, providing the desired phase margin and unity gain frequency by modification of T_1 and T_3. Its gain margin is 17 dB and reference suppression 57 dB.

FIGURE 13. 3rd ORDER LOOP WITH 2 SPURIOUS POLES

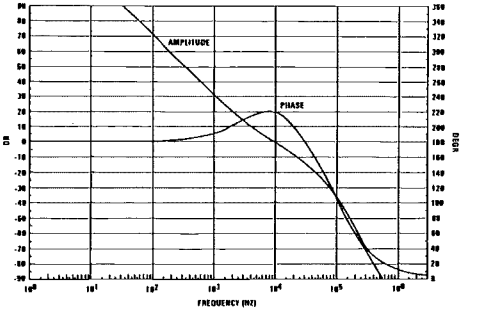


FIGURE 14. 3rd ORDER LOOP COMPENSATED FOR TWO SPURIOUS POLES

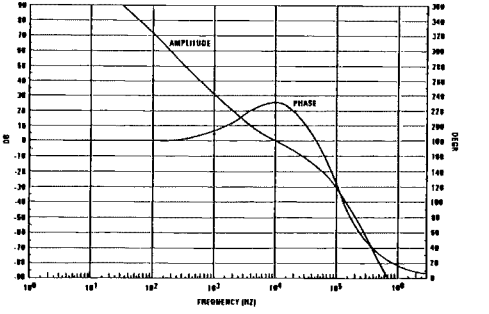


Figure 15 shows the same third order loop with a two pole filter at 75 KHz added to reduce reference sidebands. Note again that the phase margin and unity gain points are as desired, and the gain margin of 16 dB for this loop. Reference suppression is 65 dB.

Figure 16 shows the fourth order loop produced when ω_3 goes to infinity. Again the phase margin and unity gain are as required, the gain margin is 9 dB and the reference suppression 50 dB.

CONCLUSIONS:

A design technique for fourth and fifth order phase-locked loops has been described which accounts for common loop filter elements not found in earlier models. While not strictly optimum in the mathematical sense, the technique yields very useful results and is valuable as a design tool for the equipment design engineer. The technique is readily applied as a computer program which produces circuit component values from performance requirement inputs.[3]

FIGURE 15. 3rd ORDER WITH 75 KHz 2 POLE ADDED

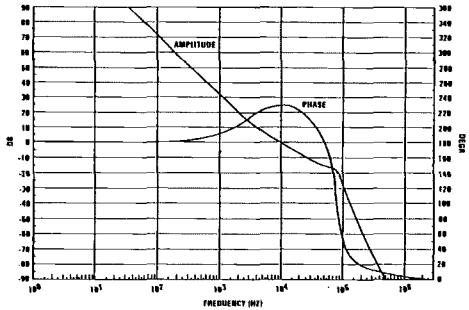
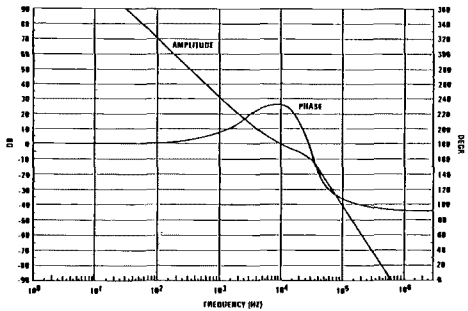


FIGURE 16. 4th ORDER LOOP WITH 31 KHz 2 POLE



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ACKNOWLEDGMENTS

The author thanks Mr. Steve Zamoscianyk for creating the program FAZLOK, which applies the compensation technique, and Mr. Paul Peloquin for extensive use of the program in generating data for this article.

DEVELOPMENT OF A C BAND POWER MODULE FOR THE MORELOS MEXICAN SATELLITE SYSTEM

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ABSTRACT

This article describes the procedures of design and characterization of power modules of 1 Watt, 3 Watt and 5 Watt intended to be used as transmission elements in RF sections of earth stations linked through the Morelos Mexican Satellite System. This article also describes the particular use of the three indicating the number of available channels for each application taking into account the essential parameters of the satellite link. These modules were developed under contract with the National Council of Science and Technology Potentially to be used in rural and private network applications in Mexico.

I. INTRODUCTION

This document deals with the effort made toward the development of high power amplifiers, based in the use of GaAsFET devices and intended to be proposed for use with the Mexican Satellite System.

We start this program by first making several low and medium power prototypes, to generate an efficient methodology for design and characterization of HPA's modules. Our main interest is to develop the technological aspects involved in the design and fabrication of this type of subsystems, based on our previous experience in the low-noise design.

II. DESIGN PHYLOSOPHY

Initially, we must select a circuit topology that allows us to satisfy the operation requirements, taken into account the final application of the amplifier. For this case, we have taken a modular approach in order to evaluate adequately each separated stage and to make any possible correction without interfering with other stages.

We have chosen to design several independents modules prior *to the main HPA prototype, namely, we* design: 1W, 3W and 5W modules, in order to get a better way of selecting the final circuit configuration, based on device availability and technological internal support.

We focused in the 3W module, because in its design and implementation, there are involved both small signal and large signal methods, that could be used in the final design. The following section will be devoted entirely to show the general design methodology, and then we will present some results and possible applications.

III. DETAILS OF 3 WATT AMPLIFIER MODULE

This module is intended to provide 3 Watts of output power at the 1dB gain compression point. In the design of this module, the main objective is to obtain a good trade-off between linearity, dc power consumption and distorsion level.

One of the goals in this design project is to get a strong correlation between computed and measured circuit performance, detecting the possible source of error in its final implementation.

The circuit configuration for this high-gain, high-power amplifier is shown in figure 1 along with the type of GaAsFET devices that will be used in its implementation. This configuration includes one balanced stage in order to increase the power handling capability of the single medium power GaAsFET.

We can see three basic building blocks in this figure, namely, the low-power two-stage block that uses cascade connection of one NE72089 with one NE69489, then there is a medium power block formed with one NE900175 cascade connected with one NE800299, and finally there is a single stage high power block that uses one internally matched GaAsFET device that provides 3.5 Watts at 6.4 GHz.

Also of importance are the 3 dB hybrid couplers that should be used in the balanced block and that will be implemented by using branch line quadrature hybrids on the same substrate used for the amplifier stage.

The basic block for the two-stage designs is shown in figure 2 and it will be used as reference in the description of the design steps that follows.

a) Design of the two-stage low-power block.

In the structure for this block is necessary to calculate the appropriate matching networks MN1, MN2 and MN3 in order to present the reflection coefficients required at the transistor input and output ports, to get maximum gain at this stage.

Due to the signal level at this point the small signal 'S' parameters of the GaAsFET can be used in the design. As a first approach, the manufacturer data sheet are used and the individual FETs are first analyzed to check for stability and available gain in the 5.9-6.4 GHz band. The result of such analysis is shown in tables 1 and 2.

The requeriments imposed to the matching networks are as follows, making reference to the results on tables 1 and 2, and regarding the values of the reflection coefficients for maximum

gain at 6.2 GHz:

1) MN1 must match the 50 Ohms source impedance, to the impedance corresponding to $\Gamma g = (\Gamma in,1)^* = \Gamma ms,1 = 0.73/\underline{150}^*$ (8.3 + j13 Ohms),

2) MN2 must match $\Gamma in,2 = (\Gamma out,1)^* = \Gamma m1,1 = 0.601/\underline{148}$ (13.4 + j13.2 Ohms), to $\Gamma out,2 = (\Gamma in,3)^* = \Gamma ms,2 = 0.803/\underline{134.7}$ (6.2 + j20.6 Ohms),

3) MN3 must transform the impedance corresponding to $\Gamma 1 = (\Gamma out,3)^* = \Gamma m1,2 = 0.887/\underline{70.8}$ (8.9 + j69.6 Ohms), to the 50 Ohms load impedance.

Based on previous results, the circuit topology selected for MN1, MN2 and MN3 is formed by the cascade connection of short lenght transmission lines, whose electrical characteristics as well as the number of elements in the network are determined with the following equations (1):

$$Zc^2 = \frac{R1/Z2^2 - R2/Z1^2}{R2 - R1} \qquad (1)$$

$$\theta c = \tan^{-1} \frac{Zc\,(R2 - R1)}{R2\,X1 + R1\,X2} \qquad (2)$$

where $Z1 = R1 + j\,X1$, $Z2 = R2 + j\,X2$, and θc, are shown schematically in figure 3. Obviously, if Zc^2 is negative the impedance transformation is not possible with only one matching element, so *more elements must be* added. *This can* be acomplished by first transforming to an intermediate impedance (arbitrary) and then using the given equations and repeat this process until the right transformation is found. When this transformation is possible, then:.

$$Ze = Zc\,\frac{Z1 + j\,Zc\tanh(\gamma\ell)}{Zc + j\,Z1\tanh(\gamma\ell)} \qquad (3)$$

where, ℓ is the physical line lenght, $\gamma = \alpha + j\,\beta$ is the propagation constant with α being the attenuation constant andβ the phase constant.

Following this method, the two-stage low power design is shown in table 3 along with the microstrip dimensions for low Er substrate. The physical implementation is shown in figure 4 and its measured response appears in figure 5. This response is in agreement with the NE69489 data sheet that shows an output power of 19 dBm at the 1dB compression point. From this figure we can see that the measured gain is around 3 dB below the calculated one and by making some tuning after construction it was possible to add 2 dB more gain with flat response. The type of tuning elements required to get this improvement suggests that in the fabrication process some errors could arise causing this discrepancy in the performance. This will be discussed later.

b) Design of the two-stage medium power block.

In this block, we use small signal 'S' parameters to calculate the matching networks for linear output power in the first stage, and the load and source impedances for maximum output power are used in the second stage.

For the NE900175 the manufacturer's data are shown in table 4

along with its corresponding stability and gain analysis. To evaluate the NE800299 stability and liner gain capabilities, the 'S' parameters were also used giving the results shown in table 5, while for this same transistor (NE800299) load-pull measurements were made in order to obtain input and output reflection coefficients at the 1 dB gain compression point. This information is shown in table 6.

With a similar approach to that of the low-power case, the matching networks in this design were determined by using the data shown in tables 4 and 5, with the following conditions at the 6.2 GHz point:

1) MN1 is designed to match the 50 Ohms source, to the impedance corresponding to $\Gamma g = (\Gamma in,1)^* = \Gamma ms,1 = 0.917/\underline{160^*}$ (22 + j8.8 Ohms),

2) MN2 has to match the reflection coefficient $\Gamma in,2 = (\Gamma out,1)^* = 0.730/\underline{104^*}$ (12.4 + j37.4 Ohms) to the measured input reflection coefficient $\Gamma meas,1 = 0.731/\underline{-11.2^*}$,

3) MN3 is designed in order to transform from the measured load impedance corresponding to $\Gamma meas,2 = 0.507/\underline{110^*}$ to the 50 Ohms load impedance.

For the cascade connection, the circuit topology and element values, its computed response using an internal small signal circuit analysis program, and their physical dimensions on microstrip transmission lines with high Er substrate appear in table 7.

Two units with similar characteristics are needed to conform the balanced stage, so, 'A' and 'B' medium power modules were constructed and tested individually giving the results shown in figure 6. Discussion of these results will be made in a following section.

c)**Design of the high-power block.**

As mentioned above, in this block we use an internally matched device that requires only, 50 Ohms lines at the input and output ports, to provide 3.5 Watts at 6.4 GHz. With slight tuning adjustment, it can be possible to get an adequate performance across the frequency band. This module is shown in figure 7 and its performance appears in figure 8.

Discussion of results.

We have found in the experimental work, that some deviations between the calculated and measured responses of both the low-power and the medium-power blocks have ocurred. In order to analyze in more detail the possible causes of that discrepancies, in what follows, we take as an example the medium-power design.

The first cause of error, could arise during the characterization of the NE800299 transistor in order to obtain its load and source impedances for maximum output power. We found for one hand, a strong frequency and input power dependence on transistor impedances, and for the other hand, we have taken the reflection coefficients of the transistor at the input and output

connector of the test fixture, and then we tried to compensate the transmission line lenght, and also the SMA connector to microstrip interface, during the Network Analyzer calibration procedure. That could bring out some errors due to the lack of precision in the setting of the reference planes.

We will use in future works to evaluate the large signal impedances of the transistor, by first optimally match the transistor in the test fixture to get maximum output power,then disassemble the test fixture, and measure the complex conjugate input and output impedances of the transistor, in the precise reference planes, by taking out the tansistor mount and measuring the complete input and output matching network that includes bias tee, tuner and connectors, as shown in figure 9. We are starting a program just to determine how well this could be used with certain degree of confidence.

The second problem we face, consists in the errors involved during the photolitographic process. This is best illustrated in Table 8 and 9, where the actual circuit dimensions are compared against the calculated ones. We found that the sources of great errors are in the high impedance elements (narrower line), so, in the matching impedance procedure, could be better to look for low impedance matching lines, or to improve the technological aspects involved.

IV. RESULTS AND APPLICATIONS

Following the methods described in Section III, we designed and built the 5 Watt prototype shown in figure 10, whose performance at 6.2 GHz appears in figure 11.

The solid state power modules described in this article were originally intended for applications in earth stations transmitters using the Morelos Mexican Satellite System. Link calculations between Ensenada, Baja California and Mexico City were performed to define the especific applications of the 1, 3, and 5 Watt modules. Table (A) shows the results of such calculations using the following Satellite Characteristics:

Satellite Characteristics
Channel 9N, Morelos

O_{S^a} - 8953 $\frac{dbw}{m^2}$
Saturation flux density

Satellite location 113.5° W

$\frac{G}{T}$ = 3.1 dB/oK
Satellite figure of Merit

BO = 6 dB
Output Backoff

$EIRP_{Sat}$ = 36.33 dw
Electric isotropic radiated power of Morelos in Ensenada

BI = 11 dB
Input Backoff

T A B L E A

PHPA Watts	GTxdB	GRx dB	G/T RES db/oK	Eb/No dB	RBW
1 Watt	50	40	19.31	5.3	30 MHz
3 Watt	50	40	19.31	6.3	30 MHz
5 Watt	50	40	19.31	10	30 MHz

PHAPA = Solid state power amplifier output;
GRx = Receiving antenna Gain
GTx = Transmitter antenna Gain;
G/TREC = Figure of Merit of receiving antena
Eb/No = Energy bit per noise
RBW = Reference Bandwidth

It can be seen from Table (A) that the 5 Watt power module would provide the best characteristics of a thin route Satellite Communications link. The improvement of the Eb/No for the 1 Watt or 3 Watt module would imply the use of bigger antenna and the reduction of the reference bandwith and hence the transmission rate.

Another possible application of the 5 Watt amplifier would be in tererestrial microwave line-of-sight links as TWTA's replacement.

V. CONCLUSIONS

We have described the methodology for obtaining low-power and medium-power modules, and we have combined them in order to get a 5 Watt module whose possible applications are in satellite communications and also in terrestrial links. We will continue in the technological development of these microwave subsystems, and in this way present additional alternatives for the Mexican Telecommunications System.

ACKNOWLEDGEMENTS

We thank Mr. Humberto Flores from CONTEL SCT and Mr Benjamin Ramirez for their participation in the link calculations of the example described in the paper.

We also thank Mr. Ricardo Chavez for their work on the measurements and circuit fabrication.

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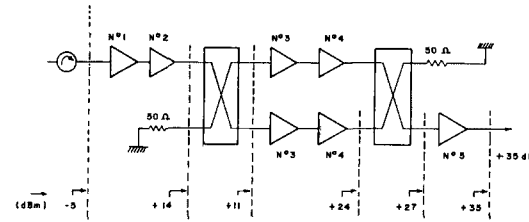


Figure 1. Circuit Configuration

#	TYPE	P_{1dB}	G_{LIN}	V_{DS}	I_{DS}
1	NE72089	+12 dBm	10 dB	3.5V	30mA
2	NE69489	+18 "	10 "	7.0V	45 "
3	NE900175	+23 "	8 "	9.0V	90 "
4	NE800299	+27 "	6 "	9.0V	300 "
5	NEZ-5964-3A	+35 "	8 "	9.0V	1200 "

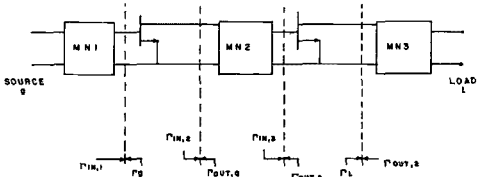


Figure 2. Basic Two-Stage Amplifier

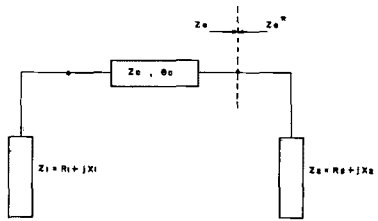


Figure 3. Impedance Transformation with Short length Transmission Line

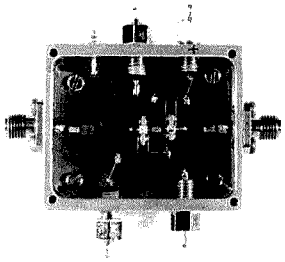


Figure 4. Photograph of Two-Stage Amplifier

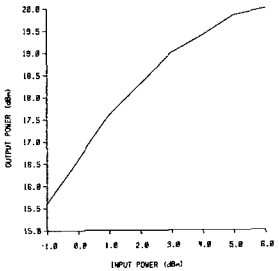


Figure 5. Measured Response of Two-Stage Amplifier at 6.2 GHz

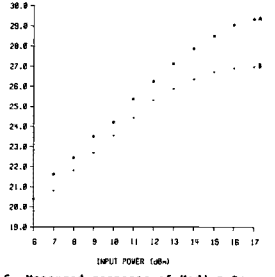
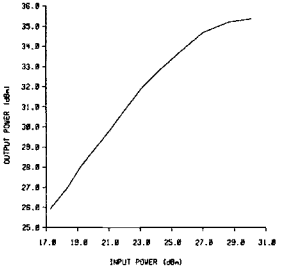


Figure 6. Measured response of Medium-Power Block



8. Measured Response of the High_Power Module

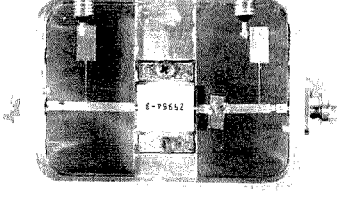


Figure 7. High-Power Block (internally matched) NEZ5964-3

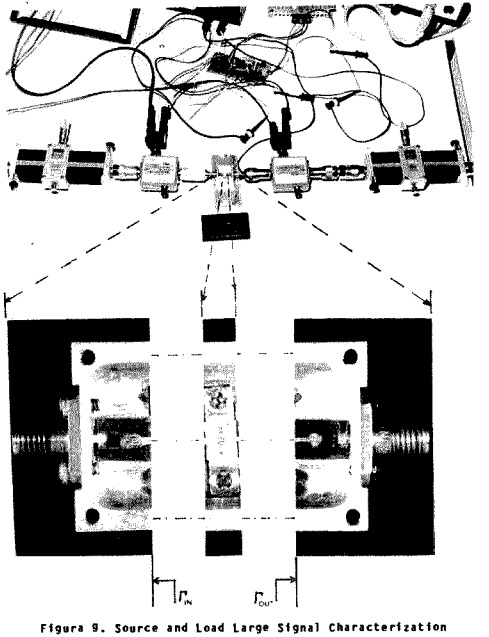


Figura 9. Source and Load Large Signal Characterization

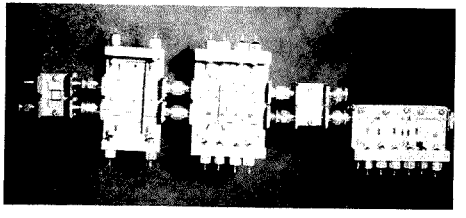


Figura 10. Circuit Topology for the 5 Watt Module

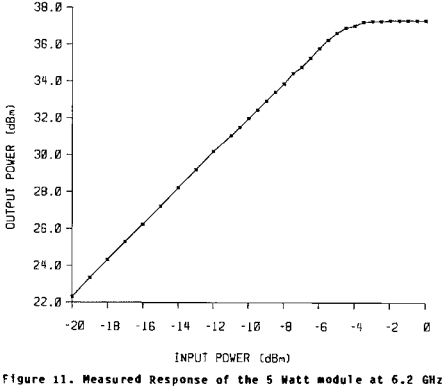


Figure 11. Measured Response of the 5 Watt module at 6.2 GHz

TABLE 1

***** NE7208 GAASFET ANALYSIS *****

S-PARAMETERS IN 50.0 OHM SYSTEM DEVICE GAIN-STABILITY DATA

FREQ	S11		S12		S21		S22		S21	K	DELTA
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	DB	FACT	MAG
5.9	0.608	172.	0.099	-9.	2.410	41.	0.390	-103.	7.6	1.0	0.149
6.0	0.597	-162.	0.100	-10.	2.310	36.	0.390	-117.	7.3	1.2	0.216
6.1	0.595	-151.	0.100	-10.	2.280	33.	0.390	-120.	7.2	1.2	0.252
6.2	0.592	-141.	0.100	-10.	2.270	33.	0.390	-125.	7.1	1.3	0.268
6.3	0.588	-115.	0.100	-10.	2.230	30.	0.390	-130.	7.0	1.4	0.334
6.4	0.584	-102.	0.101	-10.	2.200	29.	0.390	-139.	6.8	1.4	0.345

STABILITY CIRCLE LOCATIONS

FREQ	INPUT PLANE MAG	ANG	RAD	STABLE	OUTPUT PLANE MAG	ANG	RAD	STABLE
5.90	1.706	-166.7	0.69	OUTSIDE	2.866	116.4	1.84	OUTSIDE
6.00	1.815	169.6	0.75	OUTSIDE	3.305	136.1	2.19	OUTSIDE
6.10	1.879	159.6	0.78	OUTSIDE	3.724	142.1	2.57	OUTSIDE
6.20	1.924	150.0	0.81	OUTSIDE	4.002	148.3	2.82	OUTSIDE
6.30	2.128	125.0	0.95	OUTSIDE	6.815	158.2	5.50	OUTSIDE
6.40	2.197	112.1	1.00	OUTSIDE	8.132	167.2	6.78	OUTSIDE

STABLE REGION OUTSIDE OR INSIDE THE STABILITY CIRCLE

REFLECTION COEFFICIENTS FOR MAXIMUM STABLE GAIN

FREQ	INPUT PLANE GAMMA S MAG	ANG	IMPEDANCE OHMS	OUTPUT PLANE GAMMA L MAG	ANG	IMPEDANCE OHMS	GAIN DB
5.90	0.881	-166.7	3.2 +J(-5.8)	0.818	116.4	6.9 +J(30.6)	12.5
6.00	0.784	169.6	6.1 +J(4.5)	0.679	136.1	11.0 +J(19.3)	11.2
6.10	0.749	159.6	7.4 +J(8.8)	0.627	142.1	12.7 +J(16.2)	10.7
6.20	0.730	150.0	8.3 +J(13.0)	0.601	148.3	13.4 +J(13.2)	10.5
6.30	0.663	125.0	12.7 +J(24.7)	0.495	158.2	17.5 +J(8.5)	9.8
6.40	0.645	112.1	15.4 +J(31.4)	0.470	167.2	18.2 +J(4.9)	9.6

*** UNCONDITIONALLY STABLE TRANSISTOR ***
GPMAX= 10.53075DB FREQ = 6.200
CONSTANT OPERATING POWER GAIN CIRCLES

GAIN(DB)	RADII	CENTER.MAG	CENTER.ANG
2.50000	0.87554	0.10820	148.29657
4.50000	0.80376	0.16881	148.29657
6.50000	0.69037	0.26110	148.29657
8.50000	0.50575	0.39861	148.29657
10.50000	0.06207	0.59697	148.29657

TABLE 2

***** NE6948 GAASFET ANALYSIS *****

S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ	S11		S12		S21		S22		S21	K	DELTA
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	DB	FACT	MAG
5.9	0.805	-116.	0.039	24.	1.620	65.	0.820	-70.	4.2	0.9	0.659
6.0	0.800	-117.	0.040	23.	1.610	63.	0.820	-71.	4.1	0.9	0.655
6.1	0.795	-118.	0.041	22.	1.601	61.	0.820	-72.	4.1	0.9	0.650
6.2	0.790	-119.	0.042	22.	1.594	60.	0.819	-73.	4.0	0.9	0.646
6.3	0.785	-120.	0.043	21.	1.587	58.	0.818	-73.	4.0	0.9	0.641
6.4	0.779	-121.	0.044	21.	1.582	57.	0.817	-74.	4.0	0.9	0.637

STABILITY CIRCLE LOCATIONS

	---- INPUT PLANE ---------				*---- OUTPUT PLANE ---------*			
FREQ	MAG	ANG	RAD	STABLE	MAG	ANG	RAD	STABLE
5.90	1.272	126.7	0.30	OUTSIDE	1.244	80.0	0.27	OUTSIDE
6.00	1.282	128.2	0.30	OUTSIDE	1.244	80.8	0.26	OUTSIDE
6.10	1.292	129.7	0.31	OUTSIDE	1.244	81.5	0.26	OUTSIDE
6.20	1.303	131.0	0.32	OUTSIDE	1.246	82.2	0.26	OUTSIDE
6.30	1.315	132.4	0.34	OUTSIDE	1.249	82.9	0.27	OUTSIDE
6.40	1.327	133.7	0.35	OUTSIDE	1.251	83.6	0.27	OUTSIDE

STABLE REGION OUTSIDE OR INSIDE THE STABILITY CIRCLE

REFLECTION COEFFICIENTS FOR MAXIMUM STABLE GAIN

	----- INPUT PLANE ----------			*----- OUTPUT PLANE ----------*			
FREQ	GAMMA	S	IMPEDANCE	GAMMA	L	IMPEDANCE	GAIN
GHZ	MAG	ANG	OHMS	MAG	ANG	OHMS	DB
5.90	0.820	129.7	6.0 +J(23.2)	0.879	68.2	10.2 +J(72.9)	13.8
6.00	0.816	131.4	6.1 +J(22.3)	0.881	69.1	9.7 +J(71.7)	13.6
6.10	0.812	133.1	6.1 +J(21.4)	0.884	70.0	9.3 +J(70.6)	13.4
6.20	0.808	134.7	6.2 +J(20.6)	0.887	70.8	8.9 +J(69.6)	13.3
6.30	0.805	136.4	6.3 +J(19.7)	0.889	71.5	8.5 +J(68.7)	13.1
6.40	0.801	138.0	6.3 +J(18.9)	0.891	72.2	8.2 +J(67.9)	13.0

*** POTENTIALLY UNSTABLE TRANSISTOR ***

MSG= 15.79157DB FREQ = 6.200

CONSTANT OPERATING POWER GAIN CIRCLES

GAIN(DB)	RADII	CENTER.MAG	CENTER.ANG
5.75000	0.66179	0.34009	82.19690
7.75000	0.53835	0.46480	82.19690
9.75000	0.40082	0.60472	82.19690
11.75000	0.26401	0.74651	82.19690
13.75000	0.14742	0.87613	82.19690
15.75000	0.08622	0.98392	82.19690

TABLE 3

DESIGN OF THE LOW-POWER BLOCK

FREQ. LOW : 5.90 GHZ FREQ. CENTRAL : 6.20 GHZ FREQ. UPP : 6.40 GHZ

ATTENUATION : 0.10 DB/LAMBDA NUMBER OF ELEMENTS : 13

ELEMENT #	TYPE	Z(OHMS)	LENGTH (L/LAMBDA)	LENGTH (DEGREES)
1	TL	50.000	0.208	75.000
2	SC	510.000	0.000	0.000
3	TL	50.000	0.125	45.000
4	TL	30.525	0.311	111.960
5	FT	0.000	0.000	0.000
6	TL	68.243	0.046	16.560
7	SC	510.000	0.000	0.000
8	TL	68.243	0.046	16.560
9	FT	0.000	0.000	0.000
10	TL	93.375	0.090	32.400
11	TL	50.000	0.125	45.000
12	SC	510.000	0.000	0.000
13	TL	50.000	0.125	45.000

ELEMENT # 5 IS TRANSISTOR TYPE : NE7208

ELEMENT # 9 IS TRANSISTOR TYPE : NE6948

ANALIX

FREQ (GHZ)	GAIN (DB)	K (NUM)	GROUP DELAY (NSEC)	R.L.(INP) (DB)	R.L.(OUT) (DB)
5.90	17.964	2.235	0.233	5.1442	2.7004
6.00	18.675	1.720	0.284	4.6154	2.6799
6.10	18.594	1.858	0.270	4.8264	2.7233
6.20	18.549	2.041	0.230	5.2207	2.7973
6.30	17.617	2.921	0.279	6.3169	2.9112
6.40	17.050	3.498	0.461	7.1336	3.1357

DUROID 5870 ER = : 2.30 H = : 0.7874 T = : 0.0344

ELEMENT #	TYPE	Z(OHMS)	LENGTH(MM)	WIDTH(MM)
1	TL	50.00	7.318	2.322
2	SC	510.00	1.250	0.000
3	TL	50.00	4.391	2.322
4	TL	30.52	10.689	4.631
5	FT	0.00	2.000	0.000
6	TL	68.24	1.641	1.389
7	SC	510.00	1.250	0.000
8	TL	68.24	1.641	1.389
9	FT	0.00	2.000	0.000
10	TL	93.38	3.264	0.734
11	TL	50.00	4.391	2.322
12	SC	510.00	1.250	0.000
13	TL	50.00	4.391	2.322

TABLE 4

***** NB9001 GAASFET ANALYSIS *****

S-PARAMETERS IN 50.0 OHM SYSTEM DEVICE GAIN-STABILITY DATA

FREQ	S11		S12		S21		S22		S21	K	DELTA
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	DB	FACT	MAG
5.9	0.890	-153.	0.051	-6.	1.328	44.	0.576	-107.	2.5	0.8	0.486
6.0	0.890	-154.	0.050	-7.	1.310	42.	0.580	-108.	2.3	0.9	0.490
6.1	0.889	-155.	0.050	-7.	1.304	41.	0.583	-109.	2.3	0.9	0.492
6.2	0.888	-155.	0.050	-7.	1.298	40.	0.586	-109.	2.3	0.9	0.494
6.3	0.887	-156.	0.050	-7.	1.292	38.	0.589	-110.	2.2	0.9	0.497
6.4	0.886	-156.	0.050	-7.	1.286	37.	0.592	-111.	2.2	0.9	0.499

STABILITY CIRCLE LOCATIONS

FREQ	*---- INPUT PLANE ----*				*---- OUTPUT PLANE ----*			
	MAG	ANG	RAD	STABLE	MAG	ANG	RAD	STABLE
5.90	1.103	156.2	0.12	OUTSIDE	1.635	126.7	0.71	OUTSIDE
6.00	1.103	157.2	0.12	OUTSIDE	1.619	127.5	0.68	OUTSIDE
6.10	1.104	157.8	0.12	OUTSIDE	1.610	127.8	0.67	OUTSIDE
6.20	1.103	158.4	0.12	OUTSIDE	1.602	128.1	0.66	OUTSIDE
6.30	1.106	159.1	0.12	OUTSIDE	1.594	128.5	0.64	OUTSIDE
6.40	1.107	159.7	0.12	OUTSIDE	1.586	128.9	0.63	OUTSIDE

STABLE REGION OUTSIDE OR INSIDE THE STABILITY CIRCLE

REFLECTION COEFFICIENTS FOR MAXIMUM STABLE GAIN

FREQ	*----- INPUT PLANE -----*				*----- OUTPUT PLANE -----*				GAIN
	GAMMA S		IMPEDANCE OHMS		GAMMA L		IMPEDANCE OHMS		
GHZ	MAG	ANG			MAG	ANG			DB
5.90	0.918	157.7	2.2	+J(9.8)	0.712	101.2	13.8	+J(39.2)	12.2
6.00	0.918	158.8	2.2	+J(9.4)	0.717	102.8	13.2	+J(38.2)	12.1
6.10	0.918	159.4	2.2	+J(9.1)	0.723	103.5	12.8	+J(37.8)	12.0
6.20	0.917	160.1	2.2	+J(8.8)	0.730	104.2	12.4	+J(37.4)	11.9
6.30	0.917	160.8	2.2	+J(8.5)	0.736	105.0	11.9	+J(37.0)	11.9
6.40	0.916	161.4	2.2	+J(8.2)	0.743	105.8	11.5	+J(36.6)	11.8

*** POTENTIALLY UNSTABLE TRANSISTOR ***
MSG= 14.14304DB FREQ = 6.200
CONSTANT OPERATING POWER GAIN CIRCLES

GAIN(DB)	RADII	CENTER.MAG	CENTER.ANG
4.00000	0.79946	0.20599	128.11469
6.00000	0.70549	0.30364	128.11472
8.00000	0.58267	0.43321	128.11469
10.00000	0.43677	0.59284	128.11469
12.00000	0.29042	0.77241	128.11469
14.00000	0.20561	0.95492	128.11469

TABLE 6

***** NE8002 GAASFET ANALYSIS *****

S-PARAMETERS IN 50.0 OHM SYSTEM DEVICE GAIN-STABILITY DATA

FREQ	S11		S12		S21		S22		S21	K	DELTA
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	DB	FACT	MAG
5.9	0.834	140.	0.066	16.	1.302	-29.	0.555	161.	2.3	0.9	0.408
6.0	0.830	138.	0.070	15.	1.300	-31.	0.560	160.	2.3	0.9	0.407
6.1	0.825	136.	0.074	13.	1.299	-33.	0.564	159.	2.3	0.9	0.404
6.2	0.822	133.	0.078	10.	1.296	-36.	0.572	157.	2.3	0.8	0.404
6.3	0.816	132.	0.082	10.	1.298	-37.	0.573	156.	2.3	0.8	0.400
6.4	0.810	126.	0.090	5.	1.290	-43.	0.590	152.	2.2	0.7	0.403

STABILITY CIRCLE LOCATIONS

FREQ	*---- INPUT PLANE ----*				*---- OUTPUT PLANE ----*			
	MAG	ANG	RAD	STABLE	MAG	ANG	RAD	STABLE
5.90	1.155	-143.0	0.16	OUTSIDE	1.587	-174.7	0.61	OUTSIDE
6.00	1.158	-141.5	0.17	OUTSIDE	1.575	-173.5	0.61	OUTSIDE
6.10	1.163	-139.7	0.19	OUTSIDE	1.566	-172.2	0.62	OUTSIDE
6.20	1.163	-137.2	0.20	OUTSIDE	1.538	-170.1	0.62	OUTSIDE
6.30	1.171	-136.1	0.21	OUTSIDE	1.543	-169.6	0.63	OUTSIDE
6.40	1.172	-130.7	0.23	OUTSIDE	1.496	-165.6	0.62	OUTSIDE

STABLE REGION OUTSIDE OR INSIDE THE STABILITY CIRCLE

REFLECTION COEFFICIENTS FOR MAXIMUM STABLE GAIN

FREQ	*----- INPUT PLANE -----*				*----- OUTPUT PLANE -----*				GAIN
	GAMMA S		IMPEDANCE OHMS		GAMMA L		IMPEDANCE OHMS		
GHZ	MAG	ANG			MAG	ANG			DB
5.90	0.880	-144.7	3.5	+J(-15.9)	0.648	-152.4	11.3	+J(-11.7)	10.4
6.00	0.879	-143.3	3.6	+J(-16.5)	0.653	-150.7	11.2	+J(-12.5)	10.4
6.10	0.877	-141.7	3.7	+J(-17.3)	0.656	-149.0	11.1	+J(-13.2)	10.4
6.20	0.879	-139.3	3.7	+J(-18.5)	0.658	-146.8	11.2	+J(-14.2)	10.5
6.30	0.875	-138.3	3.8	+J(-18.9)	0.661	-145.8	11.1	+J(-14.7)	10.4
6.40	0.878	-133.2	3.9	+J(-21.5)	0.667	-141.5	11.1	+J(-16.7)	10.7

*** POTENTIALLY UNSTABLE TRANSISTOR ***
MSG= 12.20710DB FREQ = 6.200
CONSTANT OPERATING POWER GAIN CIRCLES

GAIN(DB)	RADII	CENTER.MAG	CENTER.ANG
2.00000	0.80216	0.20561	-170.11221
4.00000	0.71071	0.30224	-170.11221
6.00000	0.59266	0.42962	-170.11221
8.00000	0.45532	0.58527	-170.11221
10.00000	0.32250	0.75869	-170.11221
12.00000	0.24651	0.93315	-170.11221

TABLE 7

DESIGN OF THE MEDIUM-POWER BLOCK

FREQ. LOW : 5.90 GHZ FREQ. CENTRAL : 6.20 GHZ FREQ. UPP : 6.40 GHZ
MICROSTRIP ATTENUATION : 0.10 dB NUMBER OF ELEMENTS : 16

ELEMENT #	TYPE	Z(OHMS)	LENGTH/LAMBDA	LENGTH (DEGREES)
1	TL	50.000	0.208	75.000
2	SC	810.000	0.000	0.000
3	TL	50.000	0.125	45.000
4	TL	13.691	0.200	72.000
5	TL	33.934	0.070	25.200
6	FT	0.000	0.000	0.000
7	TL	47.691	0.069	24.840
8	TL	17.625	0.157	56.520
9	SC	810.000	0.000	0.000
10	TL	43.375	0.227	81.720
11	TL	22.625	0.130	46.800
12	FT	0.000	0.000	0.000
13	TL	24.243	0.185	66.600
14	TL	50.000	0.125	45.000
15	SC	810.000	0.000	0.000
16	TL	50.000	0.208	75.000

ELEMENT # 6 IS TRANSISTOR TYPE : NE9001
ELEMENT # 12 IS TRANSISTOR TYPE : NE8002

ANALIX

FREQ (GHZ(	GAIN (DB)	K NUM	GROUP DELAY (NSEC)	R.L.(IN) (DB)	R.L.(OUT) (DB)
5.90	19.691	0.662	0.931	1.5982	8.2322
6.00	21.419	0.582	0.880	2.3383	7.7162
6.10	22.193	0.636	1.015	3.4733	7.7352
6.20	22.000	0.829	0.858	5.3486	8.0659
6.30	21.106	1.086	0.761	6.5491	8.7369
6.40	19.341	1.612	1.470	10.1120	7.4513

DUROID 6010.5 ER : 10.5 H : 0.635 T : 0.0344

ELEMENT #	TYPE	Z(OHMS)	LENGTH(MM)	WIDTH(MM)
1	TL	50.00	3.889	0.527
2	CS	810.00	1.100	0.000
3	TL	50.00	2.333	0.527
4	TL	13.69	3.531	4.155
5	TL	33.93	1.258	1.139
6	FT	0.00	3.000	0.000
7	TL	47.69	1.282	0.587
8	TL	17.63	2.672	3.010
9	CS	810.00	1.100	0.000
10	TL	43.38	4.178	0.717
11	TL	22.63	2.256	2.140
12	FT	0.00	4.000	0.000
13	TL	24.24	3.404	1.937
14	TL	50.00	2.333	0.527
15	CS	810.00	1.100	0.000
16	TL	50.00	3.889	0.527

PHASE NOISE INTERMODULATION AND DYNAMIC RANGE

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The radio receiver lives and works in a non-benign environment. It needs to pick out a very weak wanted signal from a background of noise at the same time as it rejects a large number of much stronger unwanted signals. These may be present either fortuitously, as in the case of the overcrowded radio spectrum, or because of deliberate action, as in the case of Electronic Warfare. In either case, the use of suitable devices may considerably influence the job of the equipment designer.

Dynamic range is a "catch all" term, applied to limitations of intermodulation or phase noise: it has many definitions depending upon the application. Firstly, however, it is advisable to define those terms which limit the dynamic range of a receiver.

Intermodulation

This is described as the "result of a non linear transfer characteristic". The mathematics have been exhaustively treated, and Ref. 1 is recommended for those interested.

The effects of intermodulation are similar to those produced by mixing and harmonic production, insofar as the application of two signals of frequencies f_1 and f_2 produce outputs of $2f_2-f_1$, $2f_1-f_2$, $2f_1$, $2f_2$ etc. The levels of these signals are dependent upon the actual transfer function of the device and thus vary with device type. For example, a truly square law device, such as a perfect FET, produces no third order products ($2f_2-f_1$, $2f_1-f_2$). Intermodulation products are additional to the harmonics $2f_1$, $2f_2$, $3f_1$, $3f_2$ etc. Fig. 1 shows intermodulation products diagrammatically.

The effects of intermodulation are to produce unwanted signals, and these degrade the effective signal to noise ratio of the wanted signal. Consider firstly the discrete case of a weak wanted signal on 7.010 MHz and two large unwanted signals on 7.020 and 7.030 MHz. A third order product (2 x 7.02 - 7.03) falls on the wanted signal, and may completely drown it out. *Fig. 2 shows the toal HF spectrum from 1.5 to 41.5 MHz and Fig. 3 shows* the integrated power at the front end of a receiver tuned to 7 MHz. It may be seen that just as white light is made up from all the colours of the spectrum, so the total power produced by so many signals approximates to a large wide band noise signal. Now, it has already been shown that 2 signals, f_1 and f_2, produce third order intermodulation products of $2f_1-f_2$ and $2f_2-f_1$. The signals will produce third order products somewhat greater in number, viz: $2f_1-f_2$, $2f_1-f_3$, $2f_2-f_1$, $2f-f_3$, $2f-f_1$ and $2f_3-f_2$. An increase in the number of input signals will multiply greatly the effects of intermodulation, and will manifest itself as a rise in the noise floor of the receiver.

The amplitude relationships of the third order intermodulation products and the fundamental tones may be derived from Ref. 1, where it is shown that the intermodulation product amplitude is proportional to the cube of the input signal level. Thus an increase of 3dB in input level will produce an increase of 9dB in the levels of the intermodulation products. Fig. 4 shows this in graphic form, and the point where the graphs of fundamental power and intermodulation power cross is the THIRD ORDER INTERCEPT POINT.

The third order intercept point is, however, a purely theoretical concept. This is because the worst possible intermodulation ratio is 13dB (Ref. 2), so that in fact the two graphs never cross. In addition, the finite output power capability of the device leads to GAIN COMPRESSION.

Thus, it is apparent that the intermodulation produced noise floor in a receiver is related to the intercept point, and Figs. 5, 6 and 7 show the noise floor produced by various intercept points, in a receiver fed from an antenna - a realistic test! Fig. 5 shows that a large number of signals are below the noise floor and are thus lost; this represents a 0dBm intercept point. Fig. 7 shows a +20dBm intercept point noise floor, and it is obvious that many more signals may be received.

Because of the rate at which intermodulation products increase with input level (3dB on the I.P. for 1dB on the fundamental), the addition of an attenuator at the front end can improve the signal to noise ratio, as an increase in attenuation of 3dB will reduce the wanted signal by 3dB, but the intermodulation will decrease by 9dB. However, it is a fair comment that aerial attenuators are an admission of defeat, as suitable design does not require it!

The concept of dynamic range is often used when discussing intermodulation. Fig. 8 shows total receiver dynamic range, which is defined as the spurious Free Dynamic Range. Obviously an intermodulation product lying below the receiver noise floor may be ignored. Thus the usable dynamic range is that input range between the noise floor and the input level at which the intermodulation product reaches the noise floor. In fact

EQUATION (1)

$$D.R. = \frac{2}{3} (I_3 - N.F.)$$

Where D.R. is the dynamic range in dB

I_3 is the intermodulation input intercept point in dBM

N.F. is the noise floor in dBM.

Note that in any particular receiver, the noise floor is related to the bandwidth; dynamic range is similarly so related.

HF receivers will often require input intercept points of +20dBm or more. The usable noise factor of HF receivers is normally 10-12dB: exceptionally 7 or 8 dB may be required when small whip antennas are used. An SSB bandwidth would have a dynamic range of 105.3 dB. The same receiver with a 100 Hz C.W. bandwidth would have a dynamic range of 114.6 dB and thus dynamic range is quite often a confusing and imprecise term.

VHF receivers require noise figures of 1 or 2dB for most critical applications, and where co-sited transmitters are concerned, signals at 0 dBm or more are not uncommon. However, such signals are usually separated by at least 5% in frequency and filters can be provided. Close in signals at levels of -20dBm are not uncommon, and dynamic ranges in SSB bandwidths of about 98 dB are required.

The achievement of high input intercept points and low noise factors is not necessarily easy. The usual superhet architecture follows the mixer with some sort of filter, frequently a crystal filter, and the performance of this filter may well limit the performance. Crystal filters are not the linear reciprocal two part networks that theory suggests, being neither linear or reciprocal. It has been suggested that the IMD is produced by ferrite cored transformers, but experiments have shown that ladder filters with no transformers suffer similarly. Thus, although ferrite cored transformers can contribute, other mechanisms dominate in these components. The most probable is the failure of the piezo-electric material to follow Hook's Law at high input levels, and possibly the use of crystal cuts other than AT could help insofar as the relative mechanical crystal distortion is reduced. The use of SAW filters is attractive, since they are not bulk wave devices and do not suffer to such an extent from IMD; however, it is necessary to use a resonant SAW to achieve the necessary bandwidths and low insertion losses.

The design of active components such as amplifiers is relatively straightforward. Amplifiers of low noise and high dynamic range are fairly easy to produce, especially with transformer feedback, although where high reverse isolation is required, care must be taken. Mixers are however, another matter.

Probably the most popular mixer is the diode ring (Fig. 9). Although popular, this mixer does have some drawbacks, which have been well documented. These are:-

insertion loss (normally about 7dB)
high L.O. drive power (up to +27dBm)
termination sensitive (needs a wideband 50 ohms)
poor interport isolation (40dB)

The insertion loss is a parameter which may be classed merely as annoying, although it does limit the overall noise figure of the receiving system. The high L.O. drive power means a large amount of D.C. is required, affecting power budgets in a disastrous way, while termination sensitivity may mean the full potential of the mixer cannot be realised.

For the diode ring to perform adequately, a good termination "from D.C. to daylight" is required: definitely at the image frequency (LO$\pm$ sig. freq.) and preferably at the harmonics as well. Finally, interport isolation of 40dB with a +27dBm LO still leaves - 13dBm of LO radiation to be filtered or otherwise suppressed for reaching the antenna.

A further problem with the simple diode ring of this form is that the "OFF" diodes are only OFF by the forward voltage drop of the ON diodes. Thus the application of an input which exceeds this OFF voltage leads to the diodes trying to turn ON, giving gain compression and reduced IMD performance.

Fig. 10 shows a variation of this in which series resistors are added. The current flow through these resistors increases the reverse bias on the OFF diodes which gives a higher gain compression point: such a mixer can give +36dBm intercept points with a +30dBm of LO drive. Nevertheless, as is common to all commutative mixers, the intermodulation performance is related to the termination, and the LO radiation from the input port is relatively high.

Variations of this form of mixer include the Rafuse Quad MOSFET mixer of Fig. 11, which suffers with many of the same problems. Fig. 12 shows a dual VMOS mixer capable of good performance, but requiring a large amount of D.C. power and with limited isolation of the LO injection.

Many advantages accrue to the choice of the transistor tree type of approach (Fig. 13). Here the input signal produces a current in the collectors of the lower transistors and this current is commutated by the upper set of switching transistors. Because the current is to a first order approximation independent of collector voltage, the transistor tree does not exhibit the sensitivity to load impedance that the diode ring does, and indeed, by the use of suitable load impedances, gain may be achieved. The non linearity of the voltage to current conversion in the base emitter junction of the bottom transistors is the major cause of intermodulation, but by using suitably large transistors and emitter degeneration, very high performances (+32dBm input intercept) can be achieved. The Plessey SL6440 has been described (Refs. 3, 4, 5) and uses these techniques to achieve a high standard of performance. (See Fig. 16).

Phase Noise

The mixing process for the superhet receiver is shown in Fig. 14, where an incoming signal mixes with the local oscillator (LO) to product the intermediate frequency (IF). Fig. 15 shows the effect of noise modulation on the LO, where the noise sidebands of the LO mix with a strong, off channel signal to produce the IF. This means that the phase noise performance of the LO affects the capability of the receiver to reject off channel signals, and thus the receiver selectivity is not necessarily defined by the signal path filters.

This phenomena is referred to as RECIPROCAL MIXING, and has tended to become more prominent with the increased use of frequency synthesisers in equipments.

The performance level requirements of receivers is dependent upon the application. Some European mobile radio specifications call for 70dB of adjacent channel rejection equating to some -122 dBc/Hz, while an HF receiver requiring 60dB rejection in the adjacent sideband needs -94 dBc/Hz at a 500Hz offset. The use of extremely high performance filters in the receiver can be completely negated if the phase noise is poor. For example, a receiver using a KVG XF9B filter with a rejection in the unwanted sideband of 80dB at 1.2KHz, would require a local oscillator with -114dBc/Hz phase noise at 1.2KHz if the filter performance was not to be degraded.

To put these levels in perspective, relatively few signal generators are adequate to the task of being the LO in such a system. For example, "industry Standards" like the HP8640B are not specified to be good enough: neither are the HP8642, Marconi 2017/2018, or Racal 9082, all of which are modern, high performance signal generators.

All this suggests that is is very easy to over-specify a receiver in terms of selectivity, and simple synthesisers are not necessarily ideal in all situations.

The ability of the receiver to receive weak wanted signals in the presence of strong unwanted signals is therefore determined not only by the intermodulation capabilities of the receiver, but by phase noise and filter selectivity.

The usual approach to high performance syntheais has used multiple loops for good close in performance. Notable exceptions are those equipments using factional N techniques with a single loop. Nevertheless, such equipments not generally specified as highly as multi-loop synthesisers. A vital part of the synthesisers is still the low noise VCO, for which many approaches are possible. This VCO performance should not be degraded by the addition of the synthesiser: careful choice of technologies is therefore essential. For example, Gallium Arsenide dividers are much worse in phase noise production than silicon, and amongst the silicon technologies, TTL is better than ECL.

From equation (1)

$$D.R. \quad \frac{2}{3}(I_{p3} - N.F.)\ dB$$

where I_{p3} = input intercept point dBm
NF = noise floor dBm

The phase noise governed dynamic range is given by $DR_\phi = P_n + 10 \log_{10} B$ Db-tq2

Where P_n is the phase noise spectral density in dBc/Hz at any offset
B is the IF bandwidth in Hz.

(N.B. This is not quite correct if B is large enough such that noise floor is not effectively flat inside the IF bandwidth).

Ideally the ratio $\frac{DR_{IM}}{DR_\phi}$ should be 1

in a well designed receiver - i.e., the dynamic range limited by phase noise is equal to the dynamic range limited by intermodulation.

Certain aspects of low noise synthesiser design have been touched upon and Ref. 6 provides further information.

The performance of a receiver in terms of its capabilities to handle input signals widely ranging in input level is dependent upon the receiver capability in terms of intermodulation and phase noise. Neglect of either of these parameters leads to performance degradation, and it has been shown that specifications are not only often difficult to meet, but sometimes contradictory in their requirements.

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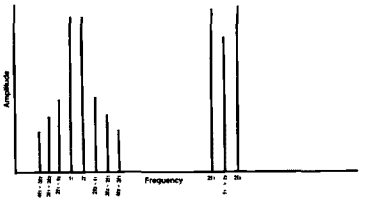


Intermodulation Products
fig 1

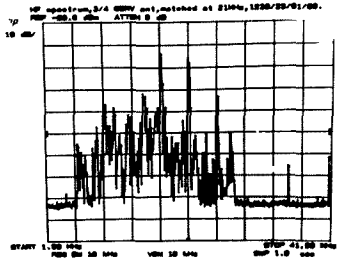


fig 2

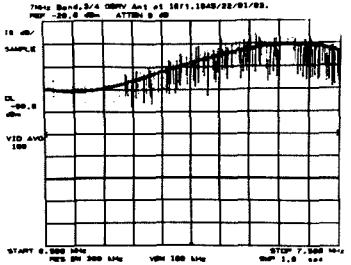


fig 3

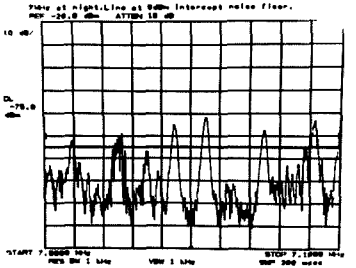


fig 5

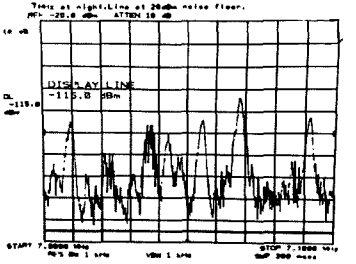
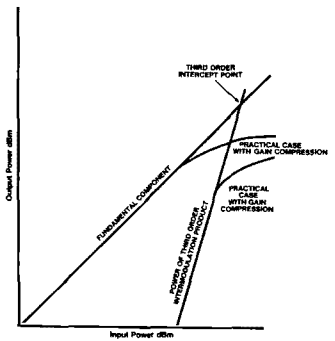


fig 7


THIRD ORDER INTERCEPT POINT
PRACTICAL CASE WITH GAIN COMPRESSION
PRACTICAL CASE WITH GAIN COMPRESSION
FUNDAMENTAL COMPONENT
POWER OF THIRD ORDER INTERMODULATION PRODUCT
Output Power dBm
Input Power dBm

Third Order Intercept fig 4

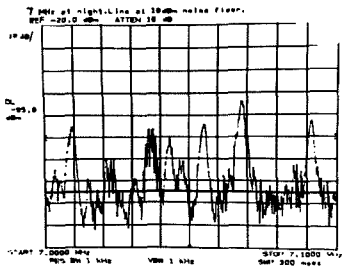


fig6

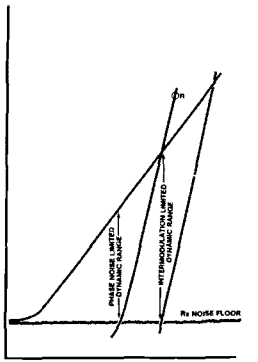
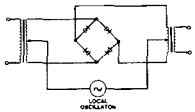
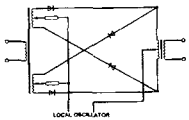


fig 8



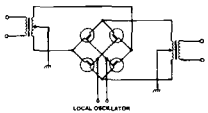
Diode ring

fig 9



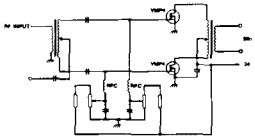
Resistive loaded high intercept point mixer

fig 10



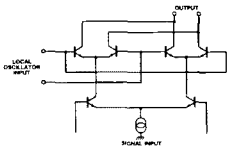
Quad MOSFET commutative mixer

fig 11



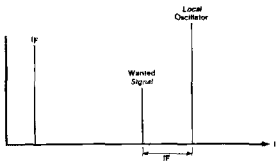
VMOS mixer

fig 12



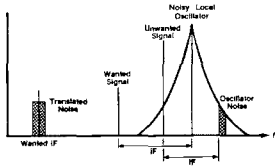
The translator tree

fig 13



Superhet mixing

fig 14



RECIPROCAL MIXING

fig 15

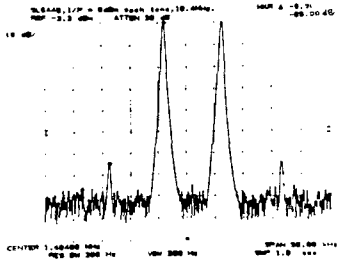


fig 16

INTERMODULATION

Intermodulation is caused by odd order curvature in the transfer characteristic of a device. If two signals F_1 and F_2 are applied to a device with third order term in its transfer characteristic, the products are given by:

$$(\text{Cos } F_1 + \text{Cos } F_2)^3 = \text{Cos}^3F_1 + 3\text{Cos}^2F_1\text{Cos}F_2 + 3\text{Cos}^2F_2\text{Cos}F_1 + \text{Cos}^3F_2$$

from the trig identities Cos^3A, Cos^2A and CosACosB, this is

$\frac{1}{4}\text{Cos}^3F_1 + \frac{1}{2}\text{Cos}F_1 + 3/2\text{Cos}^2F_1\text{Cos}F_2 + 3/2\text{Cos}F_1\text{Cos}^2F_2 + \frac{1}{2}\text{Cos}F_2 + \frac{1}{4}\text{Cos}^3F_2 + \frac{1}{2}\text{Cos}F_2$

(where $F_1 = A$ and $F_2 = B$) Neglecting coefficients, the terms $\text{Cos}^2F_1\ \text{Cos}F_2$ and $\text{Cos}F_1\ \text{Cos}^2F_2$ are equal to

$\text{Cos}(2F_1 + F_2) + \text{Cos}(2F_1 - F_2)$ and
$\text{Cos}(2F_2 + F_1) + \text{Cos}(2F_2 - F_1)$

By inspection, it may be seen that frequencies of F_1, F_2, $3F_1$, $3F_2$, $(2F_1 + F_2)$ and $(2F_2 \pm F_1)$ are present in the output. Of these, only $2F_2 - F_1$, and $2F_1 - F_2$ are close to wanted frequencies F_1 and F_2.

The application of three signals F_1, F_2 and F_3, produces a similar answer, in that the resulting products are:

$3F_1$, $3F_2$, $3F_3$, $F_1 + F_2 + F_3$, $F_1 + F_2 - F_3$, $F_1 - F_2 + F_3$, $F_1 - F_2 - F_3$, $F_2 - F_1 + F_3$, $F_2 - F_1 - F_3$, $-F_1 - F_2 - F_3$, $-F_1 - F_2 + F_3$ in addition to the products

$2F_1 \pm F_2$, $2F_2 \pm F_1$, $2F_2 \pm F_3$, $2F_3 \pm F_2$, $2F_1 \pm F_3$, $2F_3 \pm F_1$

if a greater number of signals are applied such that the input may be represented by :

$\text{Cos}F_1 + \text{Cos}F_2 + \text{Cos}F_3 + \text{Cos}F_4 \ldots \text{Cos}\ F_n$

The results of third order curvature can be calculated from:

$$(\text{Cos}F_1 + \text{Cos}F_2 + \text{Cos}F_3 + \text{Cos}F_4 \ldots \text{Cos}F_n)^3$$

This expansion produces terms of

$\text{Cos}(F_1 \pm F_2 \pm F_3)$, $\text{Cos}\ (F_1 \pm F_2 \pm F_4)$, $\text{Cos}\ (F_1 \pm F_2 \pm F_n)$ etc from which it can be seen that the total number of products is:

$$\frac{n!}{3!(n-3)!} = 4 \times 1/6n\,(n-1)\,(n-2)$$

(The factor of 4 appears because each term has four possible sign configurations i.e. $\text{Cos}(F_1 + F_2 + F_3)$, $\text{Cos}\ (F_1 + F_2 - F_3)$ etc) This agrees with RefA1.

By a similar reasoning, n signals produce:

$2n(n-1)$ products of the form $(2F_1 \pm F_2)$ $(2F_2 \pm F_1)$ etc and n 3rd harmonics.

Thus the total number of intermodulation products produced by third order distortion is:

$$n + 2n(n-1) + 2/3n(n-1)(n-2) \qquad (1)$$

Reduction of the input bandwidth of the receiver modifies this. Consider, for example, a receiver with sub-octave filters, rather than the "wide-open" situation analysed above. In this case, the third harmonics produced by any input signals will not fall within the tune band, as will some of the products such as $F_1 + F_2 + F_3$, $F_1 - F_2 - F_3$, etc. In this case, the total number of intermodulation products is reduced. There are only three possible sets of products of the form $F_1 \pm F_2 \pm F_3$, i.e. $F_1 + F_2 - F_3$, $F_1 - F_2 + F_3$ and $F_3 - F_1 - F_2$ which can give products within the band. Note that for products to be considered, they must have an effective input frequency at the receiver mixer equivalent to an on-tune desired signal. In addition, products of the form $2F_1 + F_2$, $2F_2 + F_1$ etc are again out of band. Thus half of the $2n(n-1)$ products of this class are not able to cause problems and the total number of products to be considered is now:-

$$n(n-1) + \tfrac{1}{2}n(n-1)(n-2) \qquad (2)$$

This result does not agree with Barrs (Ref A2) who uses the results in (1). The results in (2) are an absolute worst case, insofar as a number of the intermodulation products are out of band.

(For the purposes of this analysis, IMD in a mixer is assumed to produce an "on tune" signal. Thus not all the possible intermodulation frequencies appearing in a half octave bandwidth will be able to interfere).

The same arguments apply to narrower front end bandwidths. However, the narrower the front end bandwidth, the higher is the probability that the distribution of signals will produce I.M.D.

products outside the band. For example, a receiver with ±2.5% front end bandwidth tuned to 10MHz will accept signals in a band from 9.75 to 10.25MHz. Signals capable of producing a product of the form $2F_1$-F_2 must have one of the signals (F_1 or F_2) in the band 9.875 - 10.25 for a product to appear on tune. Thus the two signal apparent bandwidth is less than would be expected. Similar constraints apply to the $F_1 + F_2$-F_3 product.

Similar arguments apply to other orders of curvature. Second order curvature, for example, will not produce any products in band for input bandwidths of less than 2:1 in frequency ratio.

The actual levels of intermodulation produced can be predicted from reference A1. In practice, the situation is that the input signals to a receiver are rarely all of equal unvarying amplitude and assumptions are made from the input intercept points and the input signal density.

If a series of amplitude cells are established for given frequency ranges, such as that in table 1, then a prediction of the number of intermodulation products for any given number of input signals and amplitudes may be obtained, either from equation 1 or 2 (as applicable) or from RefA1 (for higher orders). Where the input bandwidth of the receiver is deliberately minimised, the maximum cell size in the frequency domain should be equal to the input bandwidth.

The total input power in each cell is

n Pav

where n is the number of signals and Pav is the average power of each signal.

A worst case situation is to assume that all signals in the cell are equal to the cell upper power limit boundary, e.g. if the cell amplitude range is from -40 to -30dBm, then an assumption that all signals in this cell are at -30dBm is a worst case.

If, however, it is assumed that signals will have a Gaussian distribution of input levels within a cell, then the total input power becomes:

Pt = 0.55n P

where Pt is the total power
n is the number of signals
P is the power level at the upper boundary of the cell

Because the total IMD power is the sum of all the IMD powers, the average input power is

$$Pav = \frac{0.55nP}{n}$$

The IMD power produced by third order curvature is:-

$10\log_{10}[\frac{1}{3}n(2n^2+1)]$ Antilog 1/10 [Pav-3(I_3-Pav)]dBm
where P_{IM} is the total power of the intermodulation products
I_3 is the third order input intercept point

Because the coefficients of the amplitudes of the intermodulation products are (depending on product)

a^3, a^2b, ab^2,abc, b^3

where a, b and c are approximately equal, the use of a^3 as the general coefficient is justified.

From equations 1 or 2 and 3, the total I_{MD} power and number of products may be calculated. As "n" increases in number, the number of products will mean that the resultant I_{MD} tends more to a noise floor increase in the receiver, thus reducing the effective sensitivity.

The amount of this degradation is such that the noise floor is:

$$\frac{\frac{1}{3}(n.0.55P)^3}{I_3} \cdot \frac{I_3}{(fmax-fmin)} \cdot \Delta f$$

where (fmax-fmin) is the bandwidth prior to the first intermodulating stage. Δf is signal bandwidth in a linear system.

The Gaussian Factor of 0.55 is somewhat arbitrary, since errors in this assumption are cubed.

The intermodulation Limited Dynamic Range is

$\frac{2}{3}(I_3 + 174 - 10\log_{10}\Delta f - NF)$

where NF is the Noise Figure in dB.

The effects of Reciprocal Mixing are similar, except that signals may be taken one at a time. The performance is affected by the frequency separation between an "off-tune" interfering signal

and an "on-tune" wanted signal unless the separation is such that the oscillator noise floor has been reached. Here again, reduction of front end bandwidth reduces the number of signals.

Generally speaking, the effects of reciprocal mixing are limited to close in effects - say within ± 50KHz, unless very poor synthesisers are used.

The response at some separation f_o from the tune frequency is:$(L - 10_{log}\ 10\ \Delta f)$ dB

where L is phase noise spectral density in dBc/Hz and Δf is the IF bandwidth.

This assumes that the spectral density does not change within the receiver bandwidth: Ref1 shows this to be generally applicable for narrow bandwidths.

The intermodulation free dynamic range is defined as:

$\frac{2}{3}[I_3 - \text{noise floor}] = \frac{2}{3}[I_3 + 174 - 10_{log\ 10}\Delta f\text{-NF}]$ dB

where I_3 is the input 3rd order intercept point in dBm
NF is the noise figure in dB
Δf is the IF bandwidth in Hz

It has been claimed (Ref A3) that there is 6dB rejection of phase noise in diode commutative mixers. Thus the relationship between IMD and phase noise can be expressed as:

IMD dynamic range = phase noise dynamic range + 6dB
$= (L\text{-}10_{log\ 10}\Delta f) + 6$dB

Thus at any offset, it is important to ensure that the two dynamic ranges are approximately equal if performance is not to be compromised.

A receiver for example with an input intercept point of + 20dBm and input signals of -30dBm will will produce an IMD product at -130dBm which, for an HF receiver with a noise factor of 8dB, will be just above the noise floor, in an SSB bandwidth. The noise floor of the L.O. will need to be such that the noise is at -133dBm if degradation is not be occur, and this will be produced by a noise floor of -137dBc/Hz in the synthesiser at the frequency separation of the signals in question. Thus the high intermodulation performance may well be compromised by poor phase noise.

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P. E. Chadwick
Plessey Semiconductors
Cheney Manor
Swindon
SN2 2QW

Single Chip Frequency Synthesisers using Bipolar Technology have been available for some years. Introduced originally for T.V. tuning, devices for broadcast radio were rapidly provided and Ref. 1 provides information on the earliest of these TV devices. Developments have now pushed the upper operating frequency to over 2 GHz, but, nevertheless, these devices have historically been limited to the consumer market for a number of reasons. These are:-

1. Power Consumption (150-200 mW)
2. Phase Comparison Frequency

In T.V. applications, the use of a 62.5 KHz step size for fine tuning allows the use of a fixed prescaler at the front end of the chip - Fig. 1. To achieve the small channel step size used in communications, the phase comparison frequency must be reduced to a few hundred hertz, and thus the device is no longer attractive. Nevertheless, the well tried technology of an ECL prescaler and I^2L low frequency logic has certain merits, making integration onto one chip feasible and attractive. However, existing IC processes demand current levels such that CMOS technology becomes attractive if the frequency response performance can be achieved, and recent advances have now made this possible.

The 2 micron technology introduced by Plessey has been used to introduce a new family of frequency synthesiser parts operating at VHF, with every promise of extension to the UHF band. Before describing this new family in detail, some review of existing practice is justified.

As is widely known, it is desirable to keep the reference frequency in a single loop synthesiser as high as possible consistent with multiplied reference phase noise. The use of fixed prescaling (Fig. 2) is therefore limited to wide channel spacings or narrow loop bandwidths, while alternative methods of mixing (Fig. 3) or multi-modulus division (Fig. 4) provide the majority of answers to this problem. Where multi-modulus division is used, the choice of modulus is dependent upon a number of constraints, viz:

1. Minimum divide ratio is N^2-N, where moduli are N, N+1
2. Loop delay must not exceed $\frac{N}{Fin}$
3. $\frac{Fin}{N}$ must be less than the maximum count frequency of the control circuit counters *A* and *M*

In addition, the choice of various values for N can make the programming of the synthesiser easier, insofar as, for example, the use of a 40/41 divider provides "nice" programming for a 25 KHz spacing system. The increasing use of serial data bus control with microprocessors has produced some changes in outlook here, however, as even the simplest radios now seem to have a microprocessor included.

It is in the case of the hand held radio that power consuaptlon is especially important. Thus the pressure has been placed on semiconductor manufacturers to reduce the current drains of ICs and in the case of the VHF synthesiser, it is practicable to build a complete synthesiser drawing some 10-12 mA at 5 Volts. This is shown schematically in Fig. 5, where the power consumptions are about 4 mA each for the bipolar prescaler and the CMOS control chip.

The advances in small geometry CMOS technology have made it practical to integrate a CMOS prescaler with the CMOS control chip - Fig. 6. Amongst the advantages that accrue are the fact that there are no logic level output swings at the divider output frequency to be considered, which can require relatively large amounts of current - some 0.5 mA or so just to charge and discharge the capacitance of the transistor, bond pad, package and a gate input.

The Plessey Semiconductors NJ88C30 family represent a new generation of CMOS synthesiser parts. The prescaler is integrated onto the chip, and operation to 200 MHz is guaranteed in the NJ88C30. Other members of the family have been optimised for broadcast radio use (the NJ88C31) and here arrangements have been made to bypass the internal 2 modulus prescaler when operating in the medium wave (520-1600 KHz) band, (Figs. 6 and 7).

These devices employ serial data programming; the commercial demand for full parallel programming is now limited to applications requiring fast frequency changing, and, in any case, in single loop synthesisers, loop dynamics are generally the largest part of the lock-up time when low (<50 KHz) phase comparison frequencies are used.

The NJ88C30 consists of an input amplifier, 2 modulus divider (15/16 division) A and M counters and a reference oscillator and divider chain. The reference divider chain is not fully programmable, but provides a number of reference frequency possibilities dependent upon the crystal oscillator frequency. In common with other CMOS oscillators using invertors, the stability is adequate for the majority of commercial applications, but is not in the highest class: typically, some 1 ppm of drift over the temperature range can be attributed to change in phase shift through the device when operating at 10 MHz. The divider chains feed the digital phase detector with outputs suitable for use in a standard charge pump low pass filter. As mentioned earlier, and shown in Fig. 7, the NJ88C31 has some changes to make it more applicable to broadcast radio applications.

In these applications, the upper frequency limit of the input divider need only be some 120 MHz, while the number of reference frequency division ratios is limited, spacings of 4.5, 5, 9, 10, 12.5 and 25 KHz sufficing for the MF and VHF broadcast bands. The provision of a 4.5 MHz output to drive a microprocessor clock input, and a standby current of under 2 mA minimise power drain requirements when the radio is switched off, even though the crystal oscillator is still required for the clock function in some radio receivers.

Although the use of analogue phase detectors has been advised for some years in order to remove the effects of the dead zone in digital phase detectors, this has not proved necessary in many synthesisers, adequate performance being obtained from the classical "charge pump" detector. An area in which the L.F. phase noise introduced by the charge pump detector is in the reception of AM stereo signals, especially on the Motorola CQAM system. However, calculations show that the spurious phase modulation introduced is about 0.03 degrees - far enough down to produce inaudibility. Note that signal to noise ratios in car radios are often subject to "specmanship" - not even a Rolls-Royce will allow the use of a 70 dB signal to noise ratio! In any case, the phase variation produces only "wandering" of the stereo image.

The difficulty in the use of the analogue phase detector lies in addressing the requirements of a transmitter synthesiser. Where the synthesiser is directly modulated, the effects of modulation at a frequency outside the loop bandwidth is to exercise the phase detector by an amount dependent upon the deviation. When large (50-75 KHz) deviations are required, a high gain analogue phase detector may well be driven into limiting, and the production of spurious outputs at the reference frequency increased.

Sonarbuoys have such modulation requirements: the reproduction of an audio band from 5 Hz to 50 KHz with such deviations is desirable, and the use of an analogue phase detector is not desirable in such a synthesiser, unless a much higher reference frequency is used. Performance of analogue integrated phase detectors at this much higher frequency (375 KHz) leaves much to be desired: the 2 micron CMOS geometry is still capable of providing adequate performance, while the market size (some 750,000 p.a. in the Western World) is attractive.

The provision of access to the signal input of the phase detector is useful, insofar as trouble-shooting and test is concerned. It also allows the use of an external phase detector if this is desirable, although some care may be necessary to minimise the generation of spurious sidebands by direct pick up of the logic signals on the VCO control line. The use of open drain outputs provides some reduction in noise when the outputs are not used, compared with the use of full logic swings: nevertheless, it is probably better to earth these pins when not used. The simplicity of the synthesiser system may be seen by inspection of Fig. 8, where the use of a programmable operational amplifier in the charge pump adds an extra dimension of flexibility in terms of power consumption. The system does require, however, that the common mode rejection ratio of the operational amplifier be good, as it is this parameter which provides most of the reference frequency rejection. Offset in the device must be small, as must noise, and the loop filter design should take into account the open loop response of the amplifier in performing loop stability analyses.

It has been shown that the application of new semiconductor technologies to existing device architectures can produce a significant power and cost saving. It grows more and more impossible to predict the limits of high frequency performance of semiconductors - already, silicon bipolar technology has reached levels which only a few years ago would have been believed impossible for any solid state technology other than Gallium Arsenide. Obviously, the next stage in the development of single chip frequency synthesisers must be operation at higher frequencies, with 512 MHz being the next logical breakpoint. Meanwhile, the size, complexity and power consumption of the VHF synthesised radio can be reduced, while multiplication to the UHF bands is not impossible, on grounds of phase noise, power consumption or both. For more details on the overall phase noise benefits of multiplying see Ref. 2. Synthesiser design has come a long way in the last twenty years, and the introduction of single chip low power VHF and UHF synthesisers will provide equipment designers with a new weapon in the fight to cut cost, size and power consumption.

Ref. 1 A 1 GHz Single Chip PLL for TV, Lawton R, Gaussen P, Cowley N, IEEE-CE Digest of Technical Papers pp 122-123, June, 1982.

Ref. 2 Design Compromise in Single Loop Frequency Synthesisers. P.E. Chadwick, R.F. Technology Expo 1985, Anaheim, Cal. Proceedings published by R.F. Design, 6530 S. Yosemite St., Englewood, Co. 80111 U.S.A.

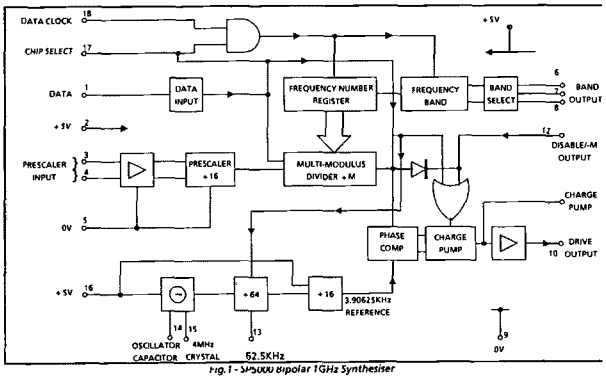

Fig.1 - SP5000 Bipolar 1GHz Synthesiser

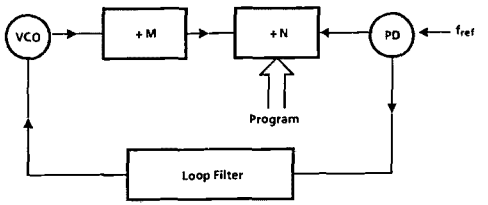

Fig.2 Use of a Fixed Prescaler

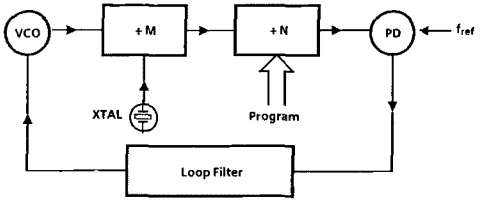

Fig.3 Mixing in the Loop

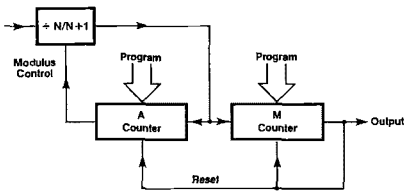

Fig.4 **Two modulus divider**

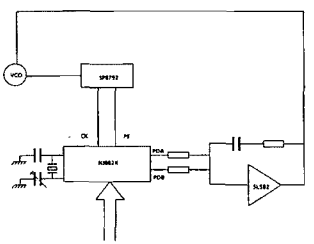

Fig. 5 MULTI-CHIP SYNTHESISER

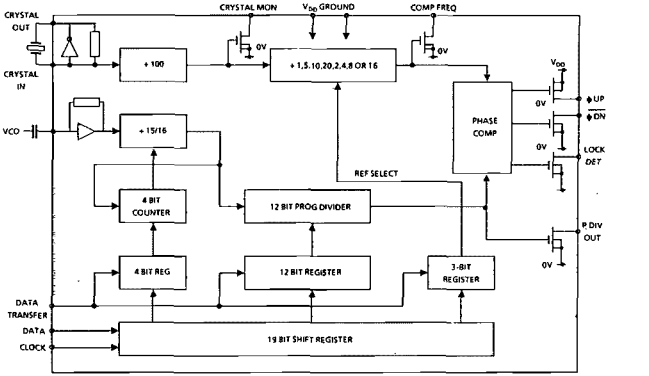

Fig.6 - NJ88C30 Single Chip 200MHz

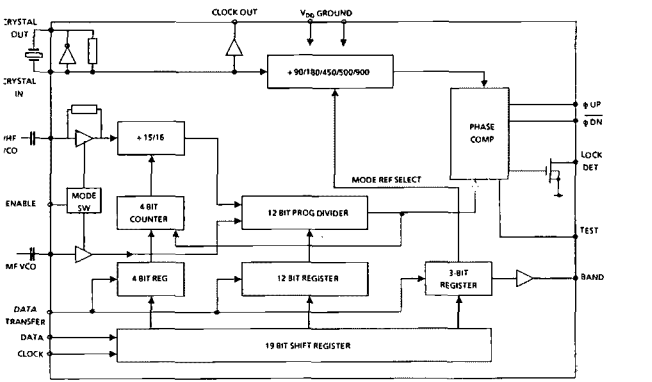

Fig.7 - NJ88C31 Broadcast Radio Synthesiser

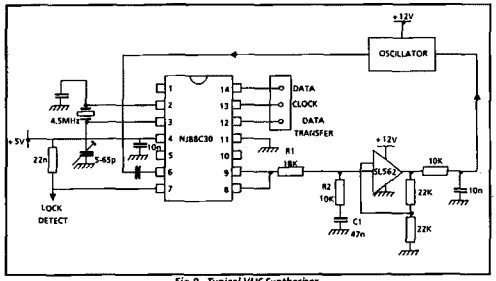

Fig.8 - Typical VHF Synthesiser

HF/VHF/UHF

Power Static Induction Transistor Performance

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Introduction

A new class of JFET, the static induction transistor (SIT), is attracting a great deal of attention [1-6] because of its exceptional high-performance in the HF, VHF, and UHF frequency ranges. SITs are vertical devices, designed with very short conducting channels fabricated with low carrier concentration semiconductor material. The channel is, therefore, depleted of carriers even at low gate bias voltage levels. Conduction in this channel is controlled by inducing electrostatic fields from the gate and the drain. This explains, to some extent, the name "static induction transistor" given to these devices by Jun-ichi Nishizawa, who first demonstrated SIT operation [7]. The method of current control in an SIT is fundamentally different from that in a JFET. In a JFET, the high series resistance of the neutral channel region and the weak electric field penetration from drain to source result in saturated, pentode-like dc I-V characteristics. In an SIT the field-controlled potential barrier results in exponential dc I-V characteristics.

In addition to describing generally how SITs operate, this paper will show that SITs are extremely well suited for cw and pulsed power, high-frequency applications, especially in the HF, VHF, and UHF range; experimental single-ended devices have thus far shown very high cw and pulsed UHF power levels comparable to or higher than BJTs, MOSFETs, ISOFETs, or JFETs and push-pull balanced SITs have demonstrated high-power, high-gain, broad-band HF/VHF frequency performance. SITs are relatively easy to build and are highly reproducible. They will be used in applications where no other semiconductor devices have proved satisfactory, for example, in very efficient phased-array antenna systems, as replacements for bulky and expensive magnetrons in microwave ovens, in AM and FM radio broadcasting power amplifiers; and in high power and broadband HF/VHF/UHF power amplifiers for military applications.

At lower frequencies, very high-power SITs have already been used in ultrasonic cleaners, in low-distortion audio amplifiers having kilowatt output power capability [8] and as fast switches in a high-voltage thyristor form [9]. Fast solid state relays, dc/dc converters, laser modulators, radio transmitters, and switching power supplies are presently under consideration. The SIT has thus become an important new class of power semiconductor device.

SIT Operation

SITs are a new class of transistors having a short-channel JFET structure in which the current, flowing vertically between the source and drain, is controlled by the height of an electrostatically induced potential energy barrier under the source. This barrier develops when the channel is depleted of mobile charge carriers by reverse biasing the gate junction. The height of the barrier is influenced by both the applied gate and drain bias potentials. A two-dimensional drawing of an elementary SIT cell is shown in Figure 1a. Figure 1b shows the corresponding potential distribution along the path of electron flow in the center of the channel when gate and drain bias voltages are applied. Figure 1c is a more graphic illustration of this potential barrier and the path of electron flow. If the drain potential, V_d, is kept constant and the gate potential, V_g, is varied, the barrier height changes, producing a significant change in the drain current. The SIT differs from long-channel devices such as conventional JFETs or MESFETs because, in addition to the gate bias voltage, the drain voltage also has a substantial influence on the current, through changes in the potential energy barrier height (Figure 1b). Thus, the SIT has unsaturated (triode-like) current-voltage characteristics rather than the saturated (pentode-like) characteristic of a conventional JFET or MESFET. A set of typical SIT dc current-voltage characteristic curves is shown in Figure 2.

The SIT is a majority carrier device, therefore, its speed is not limited by minority carrier stored charge as is the case in a BJT. In addition, since electron velocities are higher than hole velocities, the channel regions are generally fabricated using n-type epitaxial material. Because, for SIT operation, these channel regions must be depleted of charge carriers at low gate bias voltages, relatively high resistivity n-type material must be used. This results in a device which exhibits high breakdown voltages. Since in silicon, electrons reach saturation velocity at high electric fields, this allows device operation at high frequencies while operating at relatively high bias voltage levels.

Electron mobility decreases with increasing temperature in a majority carrier device, thus, the SIT channel is thermally stable. High-power devices may be fabricated in the conventional manner by paralleling low-power cells, but without using ballast resistors. Ballast resistors, which prevent thermal runaway in power BJTs, increase the fabrication complexity of these devices relative to SITs. The current distribution is also different in an SIT than in a BJT. Due to the "emitter crowding" effect in bipolars, the current density is maximum at the edge of the emitter periphery (Figure 3a) This is due to the transverse voltage drop in the base. In an SIT, the current density is more uniform in a source finger of equivalent width (Figure 3b). This means that the active source area is used more efficiently in an SIT than the emitter area in a BJT. In addition, the fact that the current flows through the semiconductor bulk in an SIT and not along the semiconductor surface, such as in a MOSFET, makes the SIT less sensitive to oxide and interface defects which contributes to reliability and high radiation hardness levels.

SIT Power Performance

Power HF/VHF/UHF (1 MHz to 1200 MHz) SITs have been developed and characterized and their performance demonstrated by GTE Laboratories. Devices of various sizes have been fabricated and tests have been performed under various operating conditions. Amplifiers have also been designed and tested

Previous publications [2,3,5] have provided information about GTE SIT performance at the higher UHF frequencies. Significant advances have been made recently, however, in the performance of SITs in the lower UHF frequency range. To date, the largest cw power static induction transistor fabricated is the 12-cell (W_g = 24 cm), 7-μm pitch SIT shown in the pictorial, Figure 4a. As shown in Figure 4b, this transistor has been exercised to demonstrate up to 215 W cw at 225 MHz, with 7-dB gain and 70% drain efficiency. The terminal impedance of high-voltage power UHF SITs is comfortably high compared to more conventional transistors. This 12-cell SIT exhibits the 215-W power level while working into a 6 + j6 ohm load impedance, approximately a factor of 5 higher than a more conventional, comparably powered transistor. We therefore expect to build single-ended SITs capable of much higher output power before we reach the limiting low impedance levels of present-day power transistors. Having reached the highest practical single-ended transistor power level, we may then consider building a balanced SIT to provide another factor of 2 increase in output power performance. Of course, innovative package designs will be necessary to realize this performance in view of the very high power dissipation levels and the electrical phase length to be accommodated.

Peak pulse power performance at 400 MHz for a single-ended SGSIT using our 3-cell chip design has been demonstrated at levels up to 325 W (Figure 5a). This new device, shown in Figure 5b, with 20 cells connected (W_g = 40 cm) was operated in our test system at a 78-V power supply level in a Class AB mode with a 10 μsec on time and 10% duty cycle, pulsed drive. As indicated in Figure 5a, the terminal impedances of this device are still quite manageable. In fact, increasing the total gate width of the device by a factor of 2, to provide enough capacity for a 600-W transistor, would still result in manageable impedance levels (approx. 1 ohm).

Most of our single-ended power SITs, both for cw and pulsed operation, have been set up in the common-gate configuration. Although common-source operation promises higher gain and potentially higher output power, the drain-gate feedback capacitance results in less stable operation. Nevertheless, performance results with new SITs operated in a common-source, push-pull configuration with cross neutralization [1] have shown a high degree of stability with very attractive broad-band frequency operation and with high-gain and high-output power levels.

These experimental cross-neutralized SITs were fabricated using two 4-cell, 7-μm pitch SGSITs connected in a single, balanced transistor package along with a pair of 18-pf chip capacitors mounted inside the package to provide the neutralization. The photograph in Figure 6 shows one of these cross-neutralized common-source balanced power SITs. An amplifier was designed and fabricated using coaxial 4:1 transformers and baluns loaded with high-permeability ferrite material (Figure 7). Large signal power tests were conducted with this amplifier at frequencies over the 1- to 200-MHz band. Figure 8 illustrates the measured gain, output power and efficiency for the test amplifier. As shown on this figure an output power level of approximately 100 W with greater than 13 dB power gain has been observed from 1- to 100-MHz. The output power performance rolls off to 60 W from 100- to 200-MHz, however, the gain remains relatively flat. Swept measurements have confirmed this data and show no anomalous inflections in the response. With transistor package and amplifier modifications, output power levels in excess of 100 W are expected to be achieved across the band with this design.

Conclusion

This new device, the static induction transistor, is proving to be extremely attractive for applications which require rf power amplification. It has been shown to demonstrate high output power, high-gain, high-efficiency, and broad-band frequency operation. Additionally, it exhibits high-voltage breakdown characteristics, high terminal impedance and preliminary tests indicate a high tolerance to radiation. Coupled with a straightforward processing technology, the SIT has a high potential to advance the performance of future rf power systems.

Acknowledgment

The authors gratefully acknowledge Marguerite Delaney and Peter Palermo for their work in device packaging; Brian Devlin, Charles Herrick, Steve Rose and Maureen Sullivan for their work in device processing and Paul Haugsjaa, Harry Lockwood, and Les Riseberg for their general support during the program.

This work was supported, in part, by the U.S. Air Force Systems Command under Contract No. F33615-82-C-1702 and by the U.S. Army Communications Electronics Command under Contract No. DAAL02-85-C-0160.

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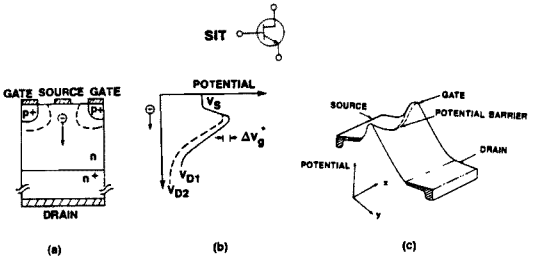

Figure 1. Elementary SGSIT cell (a), and corresponding potential distribution in center of channel along path of electron flow (b), graphic illustration of potential barrier (c).

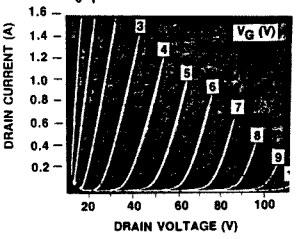

Figure 2. SGSIT DC I-V characteristics (W_s = 24 cm).

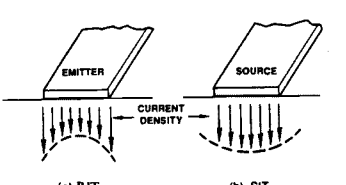

Figure 3. Current density distribution BJT vs SIT.

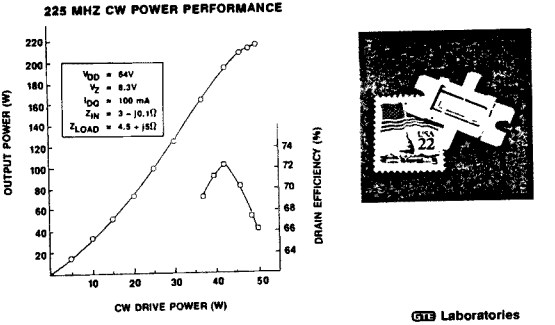

Figure 4. Performance of 12 cell (W_s = 24 cm) SGSIT.

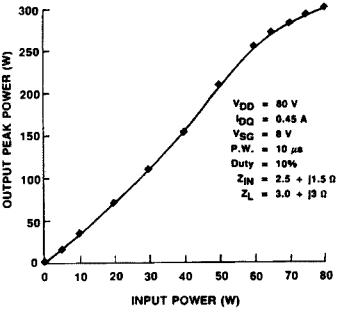

Figure 5(a). 400 MHz peak pulsed power SGSIT performance.

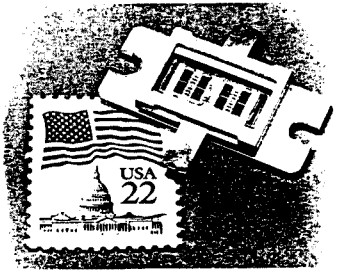

Figure 5(b). 325 W 400 MHz peak pulse power SGSIT.

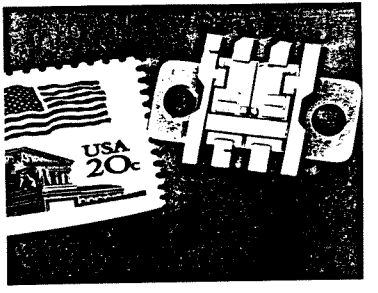

Figure 6. Cross-neutralized common-source push-pull SIT.

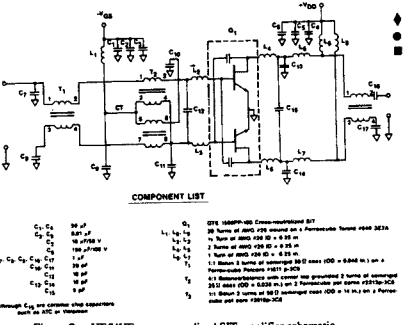

Figure 7. HF/VHF cross neutralized SIT amplifier schematic.

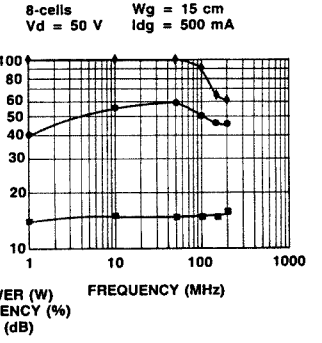

Figure 8. Broadband SIT amplifier performance.

A High Performance SAW Filterbank Achieves 80dB Rejection

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I. Introduction

This filter bank was designed as part of a general-purpose receiver system, which was to be able to isolate signals of differing center frequencies and bandwidths, to separate these signals from the surrounding spectrum and then to demodulate these signals. The features of the filterbank which were essential to this system were: excellent rejection, good control of bandwidth , filter selectivity, good amplitude and phase ripple and equal noise power in each channel. Surface wave filters meet these primary requirements nicely while maintaining a small outline and requiring little power.

This paper will present the specific requirements for a filterbank requiring 80dB of stopband rejection, followed by a discussion of both the electronic circuit and surface wave filter design. Results from production filters will be presented, followed by indications of improvements to these sorts of filterbanks.

II. The Requirements

The detailed specifications for this filterbank are presented in Appendix I. The essence of the filterbank is presented in the schematic shown in Figure 1. An input signal passes through a wideband roofing filter and a low-noise amplifier and then through one of nine channels

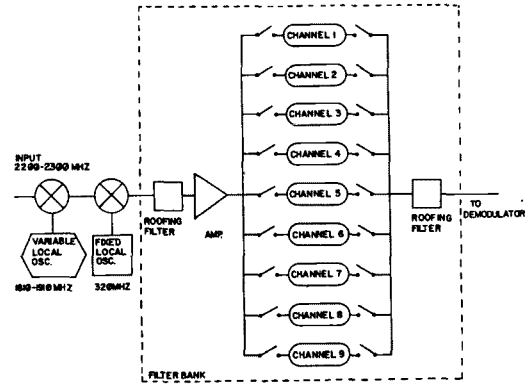


Figure 1

having bandwidths from 0.1 MHz (channel 1) to 12.0 MHz (channel 8) and 25 Mhz (channel 9, direct). All channels had a common center frequency (70 MHz) and were required to have equal noise powers (for white noise, the power levels in each channel were supposed to be the same), so the insertion losses varied from 29dB for channel 1 (0.1 MHz) to 50dB for channel 8 (12.0 MHz) and 53dB for channel 9 (direct).

The most strenuous specification was the requirement for 80dB of rejection for each channel. This rejection had to be maintained from 5 MHz to 400 MHz outside seven 3dB bandwidths from the center frequency and drove most of the design, as will be discussed in section III. The next most important specification was the requirement for 50dB of insertion loss for channel 8, which put a severe constraint on the noise floor for the filterbank. These two specifications forced most of the interesting design decisions.

The requirements for precisely controlled bandwidth and shape is common to most surface acoustic wave filter designs. Since an enormous number of transmission zeros can be designed in a very small space, surface wave filters can provide excellent selectivity which is essentially independent of matching and insertion loss. Also, manipulation of these zeros can compensate for second order distortions which affect filter symmetry. The requirements of less than one dB of amplitude ripple and less than ten degrees of phase error in each channel, as well as the differential phase error specification, are also straightforward and easily satisfied with surface wave devices.

The entire operating filterbank had to meet a series of mechanical and environmental conditions including vibration and shock as well as a powered burn-in.

III. The Design Approach

A. General Considerations

The requirements for this filterbank specified nine channels, one of which was a direct channel and one of which had a 0.1 MHz bandwidth. Early analyses of channel 1 (0.1 MHz) showed that surface wave filters for this bandwidth would be much too large, so the customer agreed to supply a bulk crystal filter which met their requirements. The direct channel also needed no filter (other than an overall roofing filter to reject out-of-band noise). Probably the most important specification items were the combination of 80dB of rejection with a required 50dB insertion loss on channel 8; for an input signal at 0dBm, this puts a requirement on the noise floor to be at -130dBm. This really stems from the customer's desire to have equal noise power in each channel, so the insertion loss of the widest channel had to be considerably higher than that of the narrowest channel. Proper grounding and shielding and overall control of the noise in the circuit board was by far the most difficult aspect of the development of the filterbank.

B. Electronics

The requirement for 80dB of stopband rejection regardless of the channel selected forced the choice of dual PIN diode switches for each of the nine channels in the filterbank. These switches did not have to be

quick because the bandwidth selection was to be by mechanical thumbwheel switches, so the diodes were chosen to give a switching time of about one microsecond at 70 MHz. Each series-shunt diode switch has an on-to-off ratio of 54dB at 70 MHz for a combined isolation of 108dB for a single channel all by itself. Since all nine channels were bussed in parallel, with all channels selected off, the isolation from bus to bus was 89dB, a 9dB margin on the 80dB specification.

The requirement of 50dB of loss for channel 8 (12.0 MHz) combined with 80dB of rejection meant that the incoming signal level had to be high enough that the 80dB rejection level was at or above thermal noise. This was accomplished by driving the SAW devices at about +20dBm with an amplifier. Additional LC roofing filters at input and output were necessary to keep the noise floor below the rejection level for channel 8 and also served to suppress SAW harmonic responses, as will be discussed below.

C. The SAW Filters

This filterbank has filters whose center frequency is 70 MHz and whose channel bandwidths range from 0.1 MHz to 400 MHz. As discussed in section IIIA, channels 2 through 8 were implemented with SAW filters whose percentage bandwidth (3dB bandwidth normalized to the center frequency) varied from about 0.4% (channel 2) to about 17% (channel 8). Since the maximum achievable bandwidth for a piezoelectric surface wave material is a function of its electromechanical coupling constant [1], different SAW substrate materials were used for different channels. Specifically, ST-X quartz was used for channels 2, 3 and 4 (0.3, 0.5 and 0.75 MHz), YX quartz was used for channel 5 (1.5 MHz) and YZ lithium niobate was used for channels 6, 7 and 8 (4.0, 6.0 and 12.0 MHz). These materials all have different temperature coefficients, but this filterbank is used in an environment whose temperature does not very much and in a system that can adapt to differing center frequency shifts due to temperature, so the different substrate materials for each channel was not a problem.

The requirement for 80dB of stopband rejection cannot be met on narrowband quartz materials due to the presence of surface wave diffraction on these substrates; 45-50dB of stopband rejection is about the best that can be achieved with filter shape factors of around 2.5 on quartz. This means that all of the quartz SAW filters had to be implemented as cascaded pairs. The substrate material used for other channels, YZ lithium niobate, happens to be autocollimating; surface waves exhibit almost no diffraction on this material. This means that it may be possible to achieve the 80dB rejection requirement in a single filter, and indeed, the design simulations predicted that channel 8 (12.0 MHz) could be built as a single filter. Channels 6 and 7, however, had design sidelobes higher than 80dB and so these channels were designed as cascaded pairs.

Surface acoustic wave bandpass filters generally exhibit two kinds of frequency domain spurious, harmonic responses and bulkwave responses [2, 3]. The harmonic response is governed by the choice of the number of electrodes per wavelength (for example, 3 electrodes per wavelength supports the second harmonic and 4 electrodes per wavelength supports the third harmonic) and generally only the first harmonic response above the

fundamental is large enough to be a problem. Bulkwave responses can be caused by a number of different acoustic modes generated by the transducer in addition to the surface wave. On quartz, these bulk modes generally manifest at about twice the center frequency and can be very troublesome. On lithium niobate or any other high-coupling material, a multi-strip coupler structure can be used between the transducers to eliminate bulkwave spurious. For the quartz filters, the bulk end harmonic responses were eliminated by designing one transducer to operate at 70 MHz at its second harmonic and designing the other transducer to operate at 70 MHz at its third harmonic. No other harmonic responses coincided, so the spurious responses were eliminated. The lithium niobate filters were designed to operate at 70 MHz at the fundamental using a multi-strip coupler to suppress bulkwave spurious and relied on the LC roofing filters to suppress the harmonic response.

A significant advantage of surface wave filters is the flexibility the designer has to meet specific spectral shape requirements. This filterbank required control over the minimum and maximum 3dB bandwidth, the maximum 60 and 70dB bandwidths, the symmetry of the passband and the specific value of the insertion loss for each channel. These requirements are typical of almost any surface wave bandpass filter and can be fulfilled in a straightforward manner. In addition, the choice of cascaded filters allowed the designers to implement a time domain spurious suppression trick that reduced both amplitude and phase ripple across the passband (the specifications did not require this, but it cost nothing to design in and it improves the performance.)

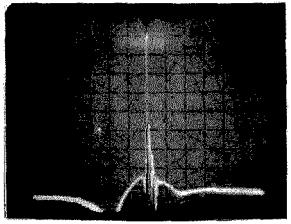
This filterbank has been in production for some time and the need to design the filters and their matching networks for minimal handling in a production environment was recognized from the start of the design. Accordingly, each filter design was subjected to a matching network sensitivity analysis for standard component tolerances. Only designs that were tolerant of the component variations expected were used to cut down on production line alignment and tuning time. Also, procedures were developed to keep the alignment process from becoming tedious and to streamline assembly.

IV. The Results

Figures 2-14 present data from a representative filterbank from a production run. Spectra for channels 1 through 9 are shown, and the rejection of the worst filter (channel 8) is presented from 5 MHz to 400 MHz. Notice that the filters uniformly achieve 80dB of rejection well inside seven 3dB bandwidths from the center frequency; in fact, most achieve 80dB on the monotonic skirts. This clean shape is a direct consequence of the choice of cascaded filters to achieve the rejection. Compare the narrower channels with channel 8, which was implemented with a single filter. Channel 8 showed some close-in spurious at about 72dB, but achieved 80dB within seven 3dB bandwidths. Also, Figure 12 shows the passband response of a representative filter, (channel 4). Figures 13 and 14 show the difference between two identical filter channels, one not employing the triple travel canceling scheme and the other utilizing it. All production filterbanks met the specifications outlined in section II

REJECTION SPECTRUM OF CHANNEL 1

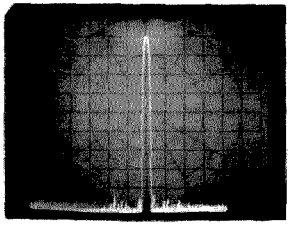
0.100 MHz



Vertical: 10dB/cm Horizontal: 60 MHz to 80 MHz linear
Figure 2

REJECTION SPECTRUM OF CHANNEL 2

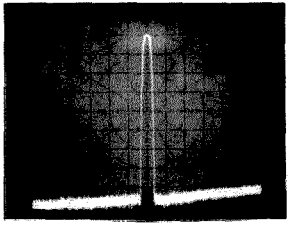
0.300 MHz



Vertical: 10dB/cm Horizontal: 60 MHz to 80 MHz linear
Figure 3

REJECTION SPECTRUM OF CHANNEL 3

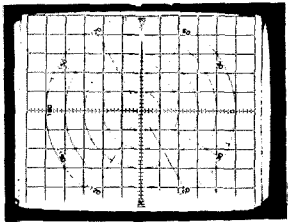
0.500 MHz



Vertical: 10dB/cm Horizontal: 60 MHz to 80 MHz linear
Figure 4

REJECTION SPECTRUM OF CHANNEL 4

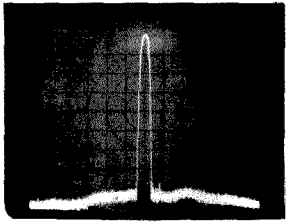
0.75 MHz



Vertical: 10dB/cm Horizontal: 40 MHz to 100 MHz linear
Figure 5

REJECTION SPECTRUM OF CHANNEL 5

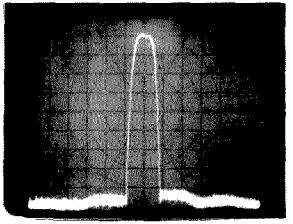
1.5 MHz



Vertical: 10dB/cm Horizontal: 40 MHz to 100 MHz
Figure 6

REJECTION SPECTRUM OF CHANNEL 6

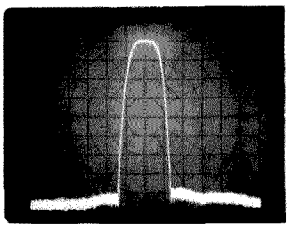
4.0 MHz



Vertical: 10dB/cm Horizontal: 40 MHz to 100 MHz linear
Figure 7

REJECTION SPECTRUM OF CHANNEL 7

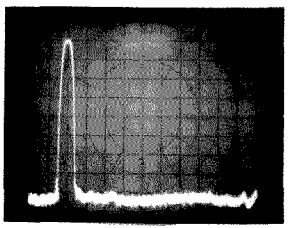
6.0 MHz



Vertical: 10dB/cm Horizontal: 40 MHz to 100 MHz
Figure 8

REJECTION OF CHANNEL 8 (12.0 MHz BANDWIDTH)

FROM 5 MHz TO 400 MHz



Vertical: 10dB/cm Horizontal: 5 MHz to 400 MHz linear
Figure 10

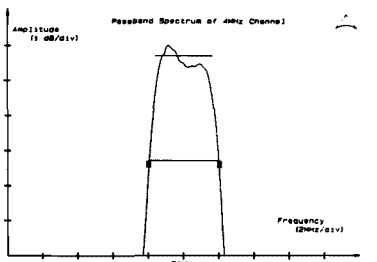
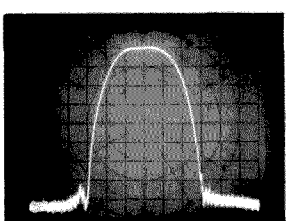


Figure 12

REJECTION SPECTRUM OF CHANNEL 8

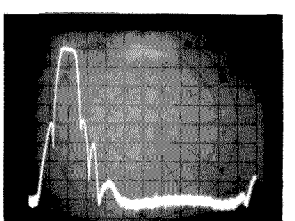
12.0 MHz



Vertical: 10dB/cm Horizontal: 40 MHz to 100 MHz linear
Figure 9

REJECTION SPECTRUM OF CHANNEL 9

DIRECT



Vertical: 10dB/cm Horizontal: 5 MHz to 400 MHz linear
Figure 11

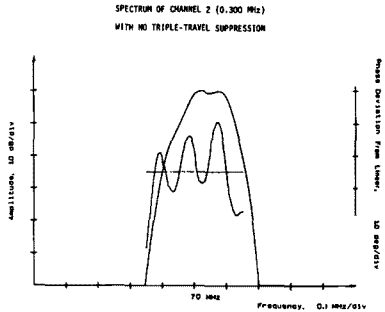

SPECTRUM OF CHANNEL 2 (0.300 MHz)
WITH NO TRIPLE-TRAVEL SUPPRESSION
Amplitude, 10 dB/div
Phase Deviation From Lock, 10 deg/div
70 MHz
Frequency, 0.1 MHz/div

Figure 13

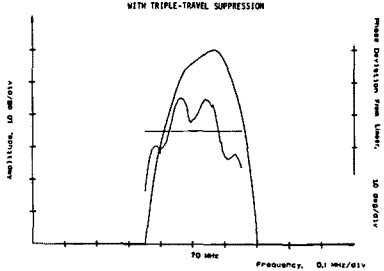


Figure 14

and Appendix I; more than 100 filterbanks were produced.

V. The Application

As can be seen from Figure 1, the filterbank was used in conjunction with a low-phase noise oscillator to form the IF section of a general purpose receiver. The operator of this receiver can select the frequency to be analyzed by choosing the synthesized oscillator's frequency and then can select the analysis bandwidth by choosing the appropriate filterbank channel. *Following this module is a general demodulator module, which* allows the operator to select one of a variety of demodulation techniques (AM, FM, PM and so forth).

Specifications for both the variable oscillator and for the filterbank will be presented, followed by data from the multichannel system. Interesting performance parameters will be discussed in depth.

Appendix I presents the electrical specifications for the synthesized local oscillator shown in Figure 15 and also the electrical specifications for the filterbank shown inside the dotted line in Figure 1.

Figure 15 presents the schematic of the synthesized local oscillator. It is a single phase locked loop driven by an external, low noise reference oscillator at 10 MHz (supplied by the customer). It was fabricated using microstrip circuits and only screened components (resistors, inductors, capacitors, semiconductors) were used. *Figure 16 shows the phase noise for* a typical production unit. All electrical specifications were met over all the environmental conditions; this includes the random vibration (whose level is about 7G RMS). Units were tested to 10G RMS for more than four hours with no degradations of any specification (including phase noise and

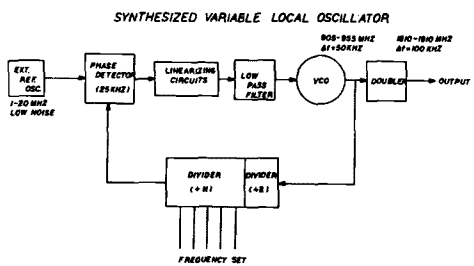


Figure 15

SYNTHESIZED OSCILLATOR PHASE NOISE

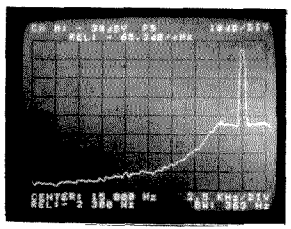


Figure 16

spurious level).

VI. The Future

The size of the filterbank presented here was 6.63 inches long by 6.5 inches wide and 0.61 inches deep. The area occupied by four of the PIN diode switches was 2.5 inches by 2.0 inches. Since the time that this filterbank was designed and built, Andersen has produced a hybridized version of the PIN diode switches that occupies an area of 1.25 inches by 0.75 inches and achieves better uniformity in a package that is less than half the size of the discrete unit. These switches were used in a four channel filterbank that measured 3.0 inches by 2.0 inches by .05 inches.

In the filterbank described here, the matching networks for the surface wave filters was external to the filter package. Since then, Andersen has produced filters with 60dB of rejection where the matching networks were hybridized and internal to the surface wave filter package. The trend toward future systems is for higher frequencies, smaller sizes and improved performances. Hybridized filterbanks achieving 80dB or more rejection at frequencies up to 1 GHz are realizable now and can be arranged to be screened to space qualification levels if desired. The combination of surface wave filters, with their ability to do complex signal processing in small sizes, and hybridized switching and amplifying networks makes small, rugged and reliable modules for the next generation of communications, radar and electronic warfare systems.

REFERENCES

[1] G. Hartmann, O. Bell and R. Rosenfeld, "Impulse Model Design of Acoustic Surface Wave Filters," IEEE Transactions on Microwave Theory and Techniques, vol. MTT-21, number 4, p. 171 (1973).

[2] S. Datta, Surface Acoustic Wave Devices, Prentice-Hall, p. 12, section 1.2.3 (1986).

[3] D. Morgan, Surface Wave Devices for Signal Processing, Elsevier, p. 66 (1985).

APPENDIX I

FILTER BANK SPECIFICATIONS

70 MHz nominal center frequency

Channel Number	3dB BW[1] (MHz)	IL[2] (dB)	Phase Linearity[3] max. (deg.)	Passband Ripple[4] max.(dB)	Fo (KHz)	Passband Symmetry[5]
1	0.1	29	±5	±0.5	N/A	±5%
2	0.3	34	±5	±0.5	±8.5	±8%
3	0.5	36	±5	±0.5	±8.5	±5%
4	0.75	36	±5	±0.5	±160	±5%
5	1.5	41	±5	±0.5	±160	±5%
6	4.0	45	±4	±0.5	±200	±5%
7	6.0	47	±4	±0.5	±250	±5%
8	12.0	50	±4	±0.5	±500	±5%

1. 3dB BW tolerance = ±5%, max.

2. IL tolerance = ±1dB, max.

3. Phase linearity is the phase deviation from the best linear fit over 60% of the 3dB BW.

4. Passband ripple is the amplitude ripple over 80% of the 3dB BW excluding monotonic roll off from the minimum loss point.

5. Passband symmetry calculated at 25°C by the following formula:

$$\text{symmetry} = \frac{f1 - f2}{f1 + f2} \times 100\%$$

where f1 = fo - lower 3dB frequency
f2 = fo + upper 3dB frequency
fo = 70 MHz

FILTER BANK SPECIFICATIONS

Rejection	80dB, minimum on all channels from 5 MHz to 400 MHz outside seven 3dB bandwidths from center frequency.
Shape Factor (all channels except 1 and 9)	$\frac{60dB\ BW}{3dB\ BW} = 2.5$, max. $\frac{70dB\ BW}{3dB\ BW} = 3.0$, max.
VSWR (input and output)	1.6:1, max., over 60 to 80 MHz
Two Tone, Third Order Intermodulation	>70dB below any 2 tones within selected passband for all power levels up to -30dBm.
Input RF Power	All specifications to be met for any input power up to -30dBm. The unit shall withstand +20dBm CW without burnout.
Operating Temperatures	-20 C to +50 C
Channel Selection	Shall be by TTL signal according to the following table.

Channel	3dB BW (MHz)	A (MSB) 0	A 1	A 2	A (LSB) 3
1	0.1	0	0	0	0
2	0.3	0	0	0	1
3	0.5	0	0	1	0
4	0.75	0	0	1	1
5	1.5	0	1	0	0
6	4.0	0	1	0	1
7	6.0	0	1	1	0
8	12.0	0	1	1	1
9	Direct	1	0	0	1

Differential Phase	Differential Phase between any 2 like filters over 80% of 3dB BW shall be 10 degrees, maximum.

SYNTHESIZED OSCILLATOR SPECIFICATIONS

Tuning Cycle	Continuous
Tuning Range	1810.0 MHz to 1910.0 MHz in 0.1 MHz steps
Frequency Control	4 wire/digit BCD parallel logic, TTL compatible
Accuracy	Dependent upon and same as external reference
Harmonics	-40dBc
Spurious	-60dBc
Phase Stability	Using low noise, stable source for input:

Customer Supplied Source		Synthesizer Output	
Offset from Carrier (Hz)	Phase Noise* (dBc/Hz)	Offset from Carrier (Hz)	Phase Noise* (dBc/Hz)
10	-98	10	-55
100	-98	100	-55
1,000	-120	1,000	-60
10,000	-135	10,000	-80
above 10,000	-145	100,000	-95
		1,000,000	-105
		2,000,000	-115
		above 2 MHz	<-120

* Single sideband phase noise in 1 Hz bandwidth.

ENVIRONMENTAL CONDITIONS (OPERATING): SYNTHESIZER AND FILTER BANK

Altitude:	Sea level to 15,000 feet
Humidity:	MIL-STD-810, Method 507, Procedure I
Vibration:	MIL-STD-810, Method 514, Procedure IA, Figure 514.2-2 (W_o = 0.06 G^2/Hz from 15 to 2000 Hz)
Sand and Dust:	MIL-STD-810, Method 510, Procedure I
Shock:	MIL-STD-810, Method 516, Procedure V
Burn-In:	160 hours at +50 °C, powered

BANDPASS AND BANDSTOP FILTERS IN THE 100 TO 1000 MHZ FREQUENCY RANGE

or, "THE SEARCH FOR Q"

by

R.V.Snyder
RS Microwave Co., Inc.
November 12, 1986

1.0 Introduction

The frequency range between 100 and 1000 MHz has always posed special problems for the designer. Lumped element techniques are difficult to apply using conventional circuits because component values are of the order of parasitic levels, while distributed networks are too large for many applications.

Constructing networks which achieve economic and technical goals requires a compromise between size and Q. Certain approaches place greater constraints upon the quality of capacitive elements while others demand higher Q inductive elements. In this frequency range much can be accomplished by combining lumped and distributed components in one structure, taking the best of both. In order to do this, it is necessary to characterize inductive and capacitive elements. Surprisingly, capacitors are more of a problem than inductors, insofar as Q is concerned. Thus, some circuits employ lumped inductances combined with distributed capacitors. The "surprise" mentioned above is due to the lack of availability of high Q commercial lumped capacitors, contrary to what is indicated in the catalog of every capacitor manufacturer. Of course, some designs use lumped capacitors and distributed inductors.

In this paper we will discuss lumped minimum phase bandpass filters with essentially symmetrical skirts. These filters are interesting because most such bandpass filters require "extra" low pass or high pass elements to increase the slope of one side of the stop band or must be overdesigned with the shortcomings of the less steep skirt kept in mind.

We will discuss bandstop filters which are lumped "analogues" of distributed circuits, which would be too large for general use in the frequency range under discussion.

Examples of the various networks will be given.

2.0 Lumped Bandpass Filters

In this section, we will cover the following topics:

a. "Dumbell" or tubular types, semi-low pass
b. Capacitively coupled, semi-high pass (a la Cohn)
c. Alternating L-C for symmetrical response
d. Wide-band, i.e. greater than an octave
    1. Conventional
    2. Generalized Chebychev (for sharper skirts, smaller size, less loss)

Figure 1 presents typical schematics and response characteristics for (a)-(c), above. The symmetrical response of (c) results from the alternation of the series L and C elements. Contrast the conventional network shown in Figure 2. This network is actually semi-high pass in nature, resulting in an upper stopband slope not as steep as the lower. In similar fashion, the tubular network is semi-low pass, with consequent degradation of the lower slope. The alternating approach achieves slope symmetry and thus avoids the necessity of overdesigning for a less steep characteristic on one side of the passband. Figure 3 describes the approach used for the more interesting and innovative network of (d)-2. These generalized Chebychev filters offer a small range of element impedances combined with the sharp skirts resultant from the finite frequency transmission zeroes located near the passband. Thus, these filters offer the realization advantages of conventional Chebychev filters with the sharp response of Elliptic Function designs. By realization advantage we mean that this design avoids the problem associated with a very large inductor coupled to a very small capacitor, or vice-versa. The transmission zeroes are "scientific" traps which cause great attenuation near the passband but with little effect on the passband. Figures 4 to 6 show the circuit and response characteristics for two different examples of generalized Chebychev low-pass high-pass cascades connected to achieve bandpass response. In these figures, the high attenuation near the passband edge is evident, as is the rippled nature of the stopband region. Power levels for filters of these types are relatively low, i.e. less than 10 watts for small units, somewhat higher if size can grow. Peak power levels can go to a Kw of so. Q values range from 80 for the ferrite loaded low frequency units to 500 or more for units operating in the 500 to 1000 MHz range.

3.0 Distributed element types

In this section, we will discuss the various types of distributed element (i.e. non-lumped element) filters that commonly are built. Our discussion will include:

a. Inductive, capacitive and iris couplings
b. Cavity filters-max bandwidth 10%, low loss,large
c. Helical resonators-small, inductively coupled
d. Printed quarter wave types.

Inductively coupled filters are typified by the helical resonator structures. Here, the resonant elements are wound coils which may be contained in a cavity. These coils have the electrical properties of a foreshortened quarter wavelength open circuited line. If the cavity encloses most of the coil, coupling from resonator to resonator occurs through an iris hole, and the inductively coupled design degenerates to an iris coupled one. Similarly, real capacitors may be used to couple the sections. As discussed in Section 2.0, inductive

or capacitive coupling result in filters with non-symmetrical skirts. Proper iris configurations tend to achieve results similar to the alternating L-C design. Filters of this type are quite compact, but display Q values of only 200 to 500. This Q value is dependent upon the size of the confining cavity; however, this is limited by the incidence of unwanted or spurious modes of resonance if the size is too great.

If the resonators are effectively quarter wavelength open circuited lengths of coaxial line, and the line is constrained within a cavity, the resultant resonant cavities can be conveniently coupled with irises. Filters of this type are relatively large, but achieve unloaded Q values of 1000 to 2000. Therefore, the insertion loss of filters built using this approach is usually quite low. Also, this approach my be easily tuned by using a variable length for the center coaxial section.

A very interesting approach is the use of printed quarter wave lines in a variety of configurations. Figures 7 and 8 illustrate the design approach and response of such a filter. Although a printed design employs distributed line lengths, the dielectric loading reduces the physical size of such filters, at a cost of insertion loss. Unloaded Q levels of about 300 can be obtained. There are a wide variety of implementations available, including balanced suspended substrate, dielectric stripline, unbalanced microstrip, confined microstrip, etc. This is a study in itself. Suffice it to say that application of the technique is not indicated if the application is for a narrow band, temperature stable design or if the skirts are required to display monotonicity below 40 or 50 db.

4.0 Lumped-Distributed types

It is possible to construct filters using a combination of lumped and distributed elements. Although no general synthesis exists as a closed form design, combinations of the response characteristics of lumped and distributed elements results in compact and efficient filters. We will discuss two examples: evanescent mode and it's close relative, the comb line.

A simple comparison of the two approaches will explain why our discussion will really center on the evanescent design. The comb line filter employs coupled lines, with each line open circuit connected to a capacitor, which is in turn grounded. The equivalent electrical length of the line-capacitor combination is 90 degrees, resulting in a band pass filter response. The equivalent coupling network is derived using the assumption that a TEM wave is propagating in a slow-wave meander-line fashion through the filter. Thus, the Q of the structure is calculated from TEM assumptions and the consequent performance of the filter is based upon that calculation. Evanescent (GR. "Decaying Spirit") mode filters

utilize the scattering of waves from obstactles placed in below-cutoff waveguide to form high Q inductively coupled bandpass filters. A waveguide structure has a normally high pass frequency characteristic. By this is meant that frequencies lower than the cut-off frequency cannot normally proceed from one end of the waveguide to the other. The waves encounter a high impedance proportional to the dimensions of the waveguide. Note that any empty tube is a waveguide structure with cut-off dependent upon the cross-sectional dimensions of the tube. The tube can be of any geometric closed shape, including rectangular, circular, etc. We can represent the high-impedance properties by a simple circuit. This is shown in Figure 9. This "Pi" of inductors contains three elements. The shunt inductors are proportional to the cut-off frequency of the tube, while the series element is proportional to the length of the tube. If we resonate the shunt elements with capacitors and then cascade a numer of these sections, we obtain the illustrated bandpass filter.

Well, so what? How does this help us to achieve superior filters? Let us look further at the properties of a rectangular waveguide. The dominant mode (lowest possible frequency of operation) propagates through the waveguide in a very low loss manner. We can say that the losses associated with resonance are very low. As we decrease the frequency below cut-off, the losses increase, but they were low to start with. Thus, although the evanescent filter operates below cut-off, the associated losses are low-as the computed Q started with a dominant waveguide mode assumption, not a TEM one. Further, the waveguide will not allow non-resonated frequencies to propagate through until a frequency well above cut-off is reached. By building the filter in a waveguide small enough (i.e. operating far below cut-off), one can build low loss filters with very high stopband to passband width ratios. In short, the evansecent filter can have very wide stopbands and is thus suited to wide spectrum applications. Such filters may be built with waveguide, connectors, pins or with combinations. Many such filters handle high power. The technique is applicable from 10 MHz to at least 40 GHz, for bandwidths from 1% to 80% Examples of both comb and evanescent filters will be given. Power levels can be as great as a few hundred watts with proper design of the resonators and loading capacitors. Q values can be 300 to 1000 for compact filters over the entire frequency range.

5.0 Equalizers

The section on bandstop filters (Sec. 6.0) will discuss amplitude equalization. Here, we will cover delay equalization of bandpass filters. We will show a slide in

which a bridged-tee lumped all-pass network is hooked in series with a Chebychev bandpass filter. The all-pass network adds "bumps" to the group delay characteristic of the combination without affecting the amplitude shape. A 100 MHz equalized filter will be shown and discussed.

6.0 Bandstop filters.

In this section we will cover:

a. Distributed parallel coupled and capacitively coupled filters

b. Lumped bandstop filters, using low pass and high pass sections as inverters between resonators.

Figure 9A presents the schematics for both distributed and lumped bandstop filters. Figures 10 through 12 present the response characteristics for filters of this type. The lumped analogues have very similar characteristics to the distributed prototype units. Figure 13 shows a transformation from the simple open circuit case to an easier-to-build version using short circuited capacitors to foreshorten the resonators, in the same way that comb-line bandpass filters are achieved. A slide will be shown in which the basic distributed circuit is realized as a parallel-coupled air-strip line structure. This latter approach is useful when high power (several Kw) is a requirement.

If the Q of the bandstop filter is intentionally reduced, the ultimate attenuation of the bandsop filter is reduced. As well, the stopband becomes non-reflective as the low Q circuit absorbs the energy, rather than reflecting it. This phenomena is useful for building amplitude equalizers. In this application, it is desired to have a shaped amplitude characteristic without sacrificing VSWR. Several examples will be given.

7.0 Conclusions

We have tried to show that diversity is the name of the game in the 100 to 1000 MHz range. Many problems are faced in achieving small size and low loss. Element Q values are critical, and commercial capacitive elements are just not compatible with the impedance levels required within the filters. Ohmic losses within the capacitors are worsened due to the low filter impedances, in some applications. A variety of techniques have been presented which should enable the budding designer to "leap" into the field, hopefully with new ideas.

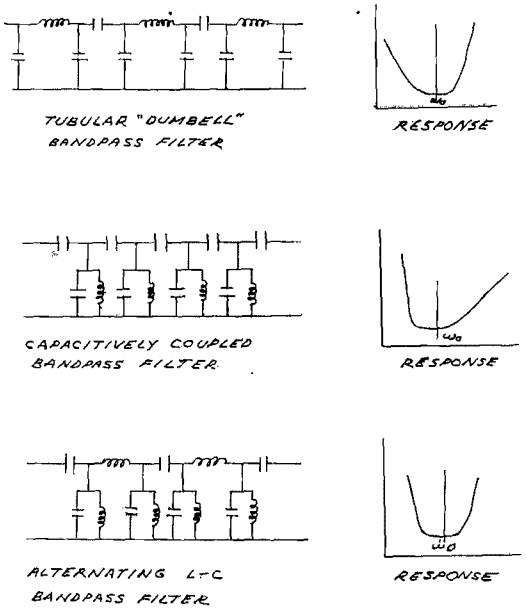


FIG. 1

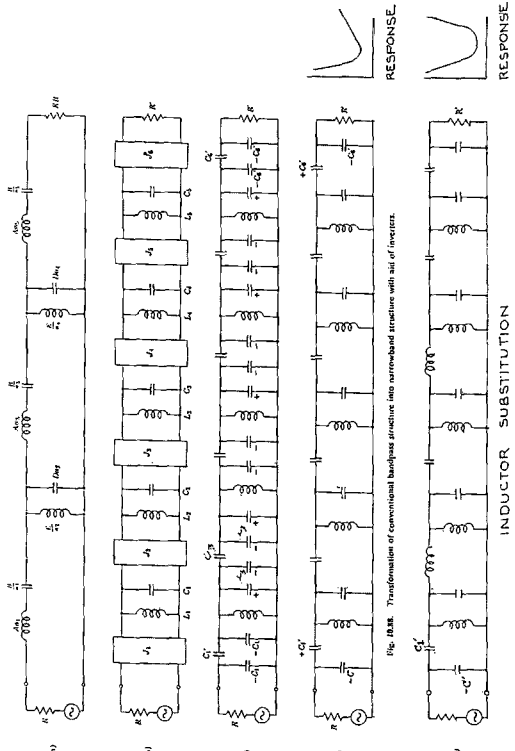
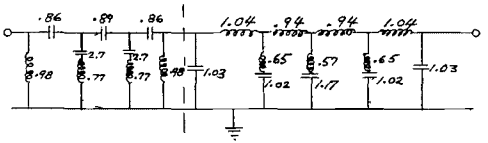


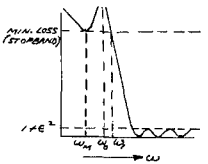
Fig. 10.31. Transformation of conventional bandpass structure into narrowband structure with aid of inverters.

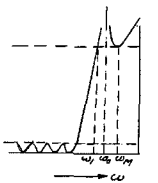
FIG. 2



HIGH PASS
N=7
MIN. α= 50 db
$\omega_0 = 0.69$
$\omega_1 = 0.75$

LOW PASS
N=9
MIN α= 50 db
$\omega_0 = 1.23$
$\omega_1 = 1.14$





GENERALIZED CHEBYCHEV LOW PASS -HIGH PASS

BEFORE DENORMALIZATION

F16.3

REQUIRED PASSBAND: 20 TO 480 MHz

INSERTION LOSS: 2.5 db max

STOPBAND: 60 db min at 10 MHz and 560 MHz, up to 1200 MHz

SWIDE3 2/17/86
"J 480 MHz LP WITH NW11 AND HP WITH NW7

RL	50
PL	3.9E-07
SR	.5
	100
SC	1.28E-10
SRLC?	R= .5 L= 2.72E-07 C= 6.21E-10
	6.21E-10
SR	.5
	100
SC	1.28E-10
SRLC?	R= .5 L= 2.72E-07 C= 6.21E-10
	6.21E-10
SR	.5
	100
SC	1.28E-10
PL	3.9E-07
PC	6.1E-12
SR	.5
	100
SL	1.6E-08
SRLC?	R= .5 L= 1.17E-08 C= 6.1E-12
	6.1E-12
SR	.5
	100
SL	1.6E-08
SRLC?	R= .5 L= 9.8E-09 C= 7.2E-12
	7.2E-12
SR	.5
	100
SL	1.6E-08
SRLC?	R= .5 L= 9.8E-09 C= 7.3E-12
	7.2E-12
SR	.5
	100
SL	1.6E-08
SRLC?	R= .5 L= 1.17E-08 C= 6.1E-12
	6.1E-12
SR	.5
	100
SL	1.6E-08
PC	6.1E-12
RL	50

VS

FREQUENCY (HZ)	INSERTION LOSS (DB)	ANGLE	(DB)	ANGLE	RETURN LOSS REAL	J(REACT)	INPUT IMPEDANC
1.0000E+07	-62.34	+151.8	-0.61	-74.4	2.79		37.90
2.0000E+07	-1.41	+31.5	-18.27	+97.5	50.10		-12.31
3.0000E+07	-0.52	+196.6	-22.63	-155.5	57.09		2.51
4.0000E+07	-0.44	+255.2	-26.83	+112.4	51.58		-4.35
5.0000E+07	-0.43	+289.7	-30.54	+12.1	47.17		-0.59
6.0000E+07	-0.42	+313.9	-30.96	-59.1	48.51		2.36
7.0000E+07	-0.41	+332.8	-30.86	-119.0	51.34		2.57
8.0000E+07	-0.40	+348.5	-29.02	-168.8	53.98		0.74
9.0000E+07	-0.39	+2.1	-26.50	+156.9	54.46		-2.00
1.0000E+08	-0.39	+14.4	-24.60	+133.1	53.98		-4.66
1.1900E+08	-0.40	+25.6	-23.14	+115.0	52.60		-6.67
1.2000E+08	-0.40	+36.1	-22.14	+100.4	50.82		-7.86
1.3000E+08	-0.41	+46.1	-21.51	+88.1	49.03		-8.30
1.4000E+08	-0.41	+55.6	-21.19	+77.5	47.46		-8.14
1.5000E+08	-0.42	+64.9	-21.14	+68.1	46.24		-7.58
1.6000E+08	-0.42	+73.9	-21.36	+60.0	45.42		-6.78
1.7000E+08	-0.42	+82.7	-21.82	+53.0	44.98		-5.86
1.8000E+08	-0.43	+91.5	-22.54	+47.3	44.92		-4.95
1.9000E+08	-0.43	+100.2	-23.53	+43.3	45.19		-4.15
2.0000E+08	-0.43	+108.9	-24.77	+41.6	45.73		-3.52
2.1000E+08	-0.43	+117.6	-26.20	+43.4	46.46		-3.14
2.2000E+08	-0.44	+126.3	-27.58	+50.0	47.29		-3.03
2.3000E+08	-0.44	+135.1	-28.40	+61.7	48.12		-3.22
2.4000E+08	-0.45	+144.0	-28.18	+74.6	48.84		-3.68
2.5000E+08	-0.46	+153.0	-27.12	+84.1	49.36		-4.33
2.6000E+08	-0.48	+162.1	-25.83	+88.5	49.61		-5.08
2.7000E+08	-0.49	+171.4	-24.58	+89.2	49.58		-5.81
2.8000E+08	-0.51	+180.8	-23.80	+87.6	49.32		-6.39
2.9000E+08	-0.52	+190.5	-23.24	+84.6	48.89		-6.74
3.0000E+08	-0.54	+200.4	-23.00	+80.9	48.42		-6.81
3.1000E+08	-0.56	+210.5	-23.08	+77.2	48.02		-6.60
3.2000E+08	-0.57	+221.0	-23.49	+73.9	47.79		-6.17
3.3000E+08	-0.59	+231.9	-24.23	+71.9	47.80		-5.61
3.4000E+08	-0.61	+243.1	-25.25	+72.1	48.10		-5.02
3.5000E+08	-0.63	+254.9	-26.40	+75.9	48.64		-4.52
3.6000E+08	-0.66	+267.2	-27.31	+83.7	49.35		-4.23
3.7000E+08	-0.70	+280.0	-27.55	+93.5	50.08		-4.20
3.8000E+08	-0.74	+293.6	-27.12	+101.2	50.67		-4.39
3.9000E+08	-0.78	+308.0	-26.53	+104.6	50.99		-4.66
4.0000E+08	-0.84	+323.3	-26.22	+104.6	51.02		-4.84
4.1000E+08	-0.90	+339.7	-26.36	+103.0	50.86		-4.78
4.2000E+08	-0.97	+357.4	-26.87	+100.9	50.66		-4.52
4.3000E+08	-1.07	+16.8	-27.39	+97.0	50.34		-4.27
4.4000E+08	-1.19	+38.1	-27.55	+83.6	49.36		-4.12
4.5000E+08	-1.34	+62.0	-26.65	+48.9	46.92		-3.30
4.6000E+08	-1.57	+89.2	-22.76	-0.9	43.22		0.10
4.7000E+08	-1.92	+120.9	-17.72	-43.9	40.82		7.49
4.8000E+08	-2.45	+158.7	-14.92	-80.2	44.25		16.17
4.9000E+08	-3.34	+208.5	-18.45	-84.3	47.49		11.45
5.0000E+08	-7.32	+278.3	-6.50	-57.7	22.74		22.99
5.1000E+08	-16.83	+335.0	-2.12	-103.9	15.51		61.49
5.2000E+08	-27.27	+7.1	-1.16	-133.1	20.54		112.18
5.3000E+08	-37.48	+27.6	-0.80	-152.8	39.86		198.85
5.4000E+08	-47.78	+41.9	-0.60	-167.5	132.34		414.12
5.5000E+08	-58.63	+52.0	-0.48	-179.2	1716.83		422.24
5.6000E+08	-70.53	+58.1	-0.39	+171.0	170.01		-588.91
5.7000E+08	-84.82	+59.2	-0.33	+162.7	41.14		-324.27
5.8000E+08	-103.46	+49.9	-0.28	+155.5	17.73		-229.28
5.9000E+08	-133.45	+26.2	-0.24	+149.2	9.75		-180.31
6.0000E+08	-155.09	+345.1	-0.21	+143.5	6.12		-151.48

F16.4

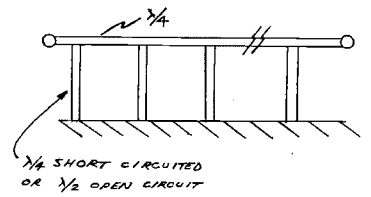
R. V. SNYDER 11/6/85
60 TO 150 MHZ LP WITH N=5 AND HP WITH N=7

```
                RL          50
1               PL          1.34E-07
2               SR          .4
0                           100
3               SC          4.7E-11
4               SRLCP       R= .4 L= 1.05E-07  C= 1.6E-10
0                           1.6E-10
5               SC          4.7E-11
6               SR          .8
0                           100
7               SRLCP       R= .4 L= 1.05E-07  C= 1.6E-10
0                           1.6E-10
8               SC          4.7E-11
9               SR          .8
0                           100
10              PL          1.3E-07
11              PC          2E-11
12              SL          5.12E-08
13              SR          .8
0                           100
14              SRLCP       R= .4 L= 3.2E-08  C= 2E-11
0                           2E-11
15              SL          4.63E-08
16              SR          .4
0                           100
17              SRLCP       R= .6 L= 2.8E-08  C= 2E-11
0                           2E-11
18              SL          4.63E-08
19              SR          .4
0                           100
20              SRLCP       R= .6 L= 3.22E-08  C= 2E-11
0                           2E-11
21              SL          5.12E-08
22              SR          .4
0                           100
23              PC          1.5E-11
                RS          50
```

FREQUENCY (HZ)	INSERTION LOSS (DB)	ANGLE	(DB)	ANGLE	RETURN LOSS REAL	+J(REACT)	INPUT IMPEDANCE
1.0000E+07	-71.70	+122.9	-0.65	-47.5	2.24	21.97	
2.0000E+07	-55.87	+158.4	-0.52	-98.9	3.55	58.34	
3.0000E+07	-52.44	+198.4	-0.33	-157.6	25.17	250.46	
4.0000E+07	-72.10	+283.8	-0.23	+133.2	4.15	-115.54	← COMPUTED W_1 = 95 MHZ
5.0000E+07	-17.07	+339.4	-0.84	+39.6	2.74	-17.96	ACTUAL 50 dB FREQ = 94.6 MHZ
6.0000E+07	-1.05	+153.0	-19.67	-8.9	40.67	1.32	
7.0000E+07	-0.69	+242.3	-33.22	+25.4	48.06	-0.90	
8.0000E+07	-0.63	+300.8	-20.84	+6.5	41.72	-0.87	
9.0000E+07	-0.60	+347.4	-22.55	-61.8	46.21	5.10	
1.0000E+08	-0.60	+28.5	-27.00	-150.7	54.00	2.37	
1.1000E+08	-0.65	+67.3	-27.80	+100.7	50.60	-4.06	
1.2000E+08	-0.73	+105.8	-24.48	+12.5	44.48	-1.15	
1.3000E+08	-0.85	+146.2	-21.24	-40.6	43.56	4.95	
1.4000E+08	-1.06	+191.6	-17.79	-51.0	41.71	8.50	
1.5000E+08	-1.30	+246.9	-9.33	-67.6	32.07	22.94	
1.6000E+08	-4.17	+310.4	-4.22	-114.7	35.91	64.62	
1.7000E+08	-5.87	+59.6	-7.89	-126.2	61.01	47.38	
1.8000E+08	-29.62	+159.0	-0.69	-158.2	53.45	248.37	
1.9000E+08	-55.84	+179.1	-0.35	+177.1	977.08	-1199.40	← COMPUTED W_2 = 186 MHZ
2.0000E+08	-34.27	+308.6	-0.24	+160.3	22.97	-286.00	ACTUAL 50 dB FREQ = 187.3 MHZ

V6

FIG. 5



PRINTED STUB FILTER

FIG. 7

V7

R. SNYDER
N=6 PRINTED STUB FILTER

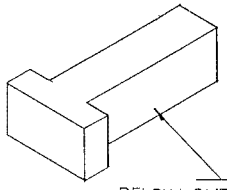
```
                RL          50
1               PTL         Z0= 33.25 LENGTH= 30 VELOCITY FACTOR= 1
0                           1
2               TR          1E+07
0                           200
3               STL         Z0= 63.4 LENGTH= 15 VELOCITY FACTOR= 1
0                           1
4               PTL         Z0= 63.02 LENGTH= 30 VELOCITY FACTOR= 1
0                           1
5               TR          1E+07
0                           200
6               STL         Z0= 86.68 LENGTH= 15 VELOCITY FACTOR= 1
0                           1
7               PTL         Z0= 48.68 LENGTH= 30 VELOCITY FACTOR= 1
0                           1
8               TR          1E+07
0                           200
9               STL         Z0= 90.11 LENGTH= 15 VELOCITY FACTOR= 1
0                           1
10              PTL         Z0= 48.68 LENGTH= 30 VELOCITY FACTOR= 1
0                           1
11              TR          1E+07
0                           200
12              STL         Z0= 86.68 LENGTH= 15 VELOCITY FACTOR= 1
0                           1
13              PTL         Z0= 63.02 LENGTH= 30 VELOCITY FACTOR= 1
0                           1
14              TR          1E+07
0                           200
15              STL         Z0= 63.4 LENGTH= 15 VELOCITY FACTOR= 1
0                           1
16              PTL         Z0= 33.24 LENGTH= 30 VELOCITY FACTOR= 1
0                           1
17              TR          1E+07
0                           200
```

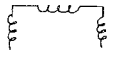
```
                RS          50
```

FREQUENCY (HZ)	INSERTION LOSS (DB)	ANGLE	RETURN LOSS (DB)	ANGLE	REAL	+J(REACT)	INPUT IMPEDANCE
2.5000E+08	-271.01	+21.6	-0.06	-0.1	0.18	0.04	
2.7000E+08	-116.91	+293.5	-0.07	-9.7	0.20	4.24	
2.9000E+08	-85.35	+295.6	-0.07	-19.5	0.22	8.58	
3.1000E+08	-67.56	+301.3	-0.08	-29.6	0.26	13.21	
3.3000E+08	-53.26	+311.9	-0.10	-40.3	0.32	18.33	
3.5000E+08	-40.18	+328.3	-0.12	-51.7	0.41	24.22	
3.7000E+08	-26.45	+350.5	-0.15	-64.1	0.61	31.31	
3.9000E+08	-9.65	+40.5	-0.26	-77.7	1.24	40.28	
4.1000E+08	-0.77	+171.1	-0.89	-92.6	5.36	52.04	
4.3000E+08	-0.44	+252.9	-4.59	-103.7	30.52	53.61	
4.5000E+08	-0.53	+316.9	-11.50	-92.6	44.39	25.40	
4.7000E+08	-0.40	+12.1	-16.97	-85.0	46.89	13.51	
4.9000E+08	-0.32	+65.0	-25.64	-55.7	46.97	4.06	
5.1000E+08	-0.33	+116.8	-25.28	+58.2	47.02	-4.37	
5.3000E+08	-0.45	+169.8	-16.76	+85.0	46.77	-13.82	
5.5000E+08	-0.60	+225.0	-11.32	+92.9	44.26	-25.93	
5.7000E+08	-0.59	+289.6	-4.49	+103.3	29.79	-53.66	
5.9000E+08	-1.04	+12.5	-0.97	+52.0	5.78	-51.44	
6.1000E+08	-10.60	+139.7	-0.36	+77.2	1.69	-39.90	
6.3000E+08	-27.09	+187.7	-0.24	+63.6	0.97	-31.02	
6.5000E+08	-10.73	+299.1	-0.20	+51.3	0.72	-23.99	
6.7000E+08	-53.80	+222.5	-0.18	+33.9	0.60	-18.14	
6.9000E+08	-68.16	+231.4	-0.17	+23.2	0.53	-13.04	
7.1000E+08	-86.75	+235.5	-0.17	+19.1	0.49	-8.42	
7.3000E+08	-118.33	+225.6	-0.16	+9.4	0.47	-4.09	
7.5000E+08	-220.73	+19.5	-0.17	-0.2	0.48	0.11	

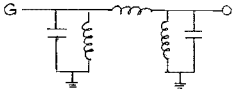
FIG. 8

V8





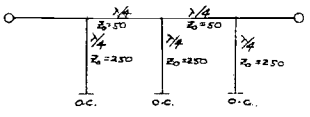
ADD CAPACITIVE PINS:



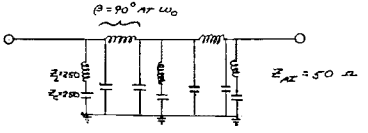
RESULT:
INDUCTIVELY
COUPLED
BAND PASS FILTERS
WITHOUT SPURIOUS
UNTIL $f > f_c$

EVANESCENT MODE PRINCIPLE

FIG. 9



N=3 DISTRIBUTED
BAND STOP FILTER



N=3 LUMPED EQUIVALENT
BAND STOP FILTER
PI CIRCUITS USED AS 90° INVERTERS
PASSBAND MAINTAINED TO ABOUT 1.9 ω_0
(HIGHER ORDER INVERTERS PROVIDED WIDER PASSBAND)
CAPACITIVE PI (HIGH PASS) MAINTAINS PASSBAND
DOWN TO 0.7 ω_0 BUT UP TO $2\omega_0$ OR $3\omega_0$.

FIG. 9A

VA

```
R, SNYDER
3 POLE DISTRIBUTED BANDSTOP FILTER
                RL              50
1               STL             Z0= 145.1 LENGTH= 7.5 VELOCITY FACTOR= 1
0                               1
2               TR              1E+09
0                               500
3               STL             Z0= 76.3 LENGTH= 7.5 VELOCITY FACTOR= 1
0                               1
4               STL             Z0= 85.5 LENGTH= 7.5 VELOCITY FACTOR= 1
0                               1
5               TR              1E+09
0                               500
6               STL             Z0= 76.3 LENGTH= 7.5 VELOCITY FACTOR= 1
0                               1
7               STL             Z0= 145.1 LENGTH= 7.5 VELOCITY FACTOR= 1
0                               1
8               TR              1E+09
0                               500
                RS              50
FREQUENCY       INSERTION LOSS                          RETURN LOSS     INPUT IMPEDANCE
(HZ)            (DB)    ANGLE          (DB)    ANGLE    REAL +J(IMAGE)
5.0000E+08      -0.11  +136.9          -15.44  +133.2    59.84   -13.45
5.5000E+08      -0.11  +154.2          -16.97  +115.9    54.66   -14.22
6.0000E+08      -0.08  +173.7          -19.25   +96.5    50.05   -10.98
6.5000E+08      -0.04  +196.8          -30.96   +74.6    49.19    -2.69
7.0000E+08      -0.16  +225.8          -16.30   -137.7    51.26    12.93
7.5000E+08      -1.35  +268.7           -6.07   -179.4    148.94    1.98
8.0000E+08      -5.84  +319.1           -1.45   +130.1    22.65  -163.34
8.5000E+08      -14.14   +1.8           -0.26   +87.2     1.45   -47.60
9.0000E+08      -25.78  +34.2           -0.09   +54.2     0.33   -25.58
9.5000E+08      +44.66  -60.7           -0.06   +26.0     0.23   +11.55
1.0000E+09      -140.91  +76.5          -0.08    -0.4     0.23     0.15
1.0500E+09      +43.94 +300.5           -0.09   -26.8     0.27    11.90
1.1000E+09      -23.42 +327.0           -0.12   -53.0     0.42    26.03
1.1500E+09      -13.30 +289.7           -0.21   -88.2     1.25    48.44
1.2000E+09      -5.72   +42.5           -1.57  -131.3    25.55   105.38
1.2500E+09      -1.34   +92.7           -6.32  +178.4    143.17    -4.89
1.3000E+09      -0.19  +134.2          -16.76  +137.4    60.84   -12.17
1.3500E+09      -0.07  +163.9          -30.04   -76.8    49.20     3.02
1.4000E+09      -0.11  +186.9          -19.17   -97.3    50.19    11.09
```

FIG. 10

V10

```
R, SNYDER
LUMPED 3 POLE BANDSTOP FILTER EQUIVALENT TO DISTRIBUTED EXAMPLE
                RL              50
1               SRLCP           R= .5 L= 2.4E-08  C= 1.05E-12
0                               1.05E-12
2               PC              2.27E-12
3               SL              1.13E-08
4               PC              2.27E-12
5               SRLCP           R= .5 L= 1.4E-08  C= 1.79E-12
0                               1.79E-12
6               PC              2.27E-12
7               SL              1.13E-08
8               PC              2.27E-12
9               SRLCP           R= .5 L= 2.4E-08  C= 1.05E-12
0                               1.05E-12
                RS              50
FREQUENCY       INSERTION LOSS                          RETURN LOSS     INPUT IMPEDANCE
(HZ)            (DB)    ANGLE          (DB)    ANGLE    REAL +J(IMAGE)
5.0000E+08      -0.05  +105.8          -20.57   -16.1     41.76     2.19
5.5000E+08      -0.03  +119.2          -24.38   -29.6     44.93     2.69
6.0000E+08      -0.02  +133.8          -34.41   -45.4     48.66     1.32
6.5000E+08      -0.03  +150.4          -31.44  +120.9     51.34    -2.36
7.0000E+08      -0.06  +169.7          -23.48  +101.1     50.85    -6.71
7.5000E+08      -0.10  +193.7          -22.62   +78.0     47.99    -6.98
8.0000E+08      -0.15  +227.7          -27.39  -148.0     53.70     2.43
8.5000E+08      -1.90  +288.0           -5.50  +156.8    123.11   -65.74
9.0000E+08      -12.63   +1.2           -0.52   +85.2     2.78    -45.94
9.5000E+08      -32.49   +45.3          -0.19   +38.2     0.61    -17.31
1.0000E+09     -102.91  +255.1          -0.17    +1.8     0.50     -0.78
1.0500E+09      -39.24  +310.4          -0.18   -32.5     0.57     14.59
1.1000E+09      -21.18  +341.9          -0.24   -67.9     0.99     33.68
1.1500E+09      -11.37   +19.0          -0.58  -106.2     4.66     66.44
1.2000E+09       -5.45   +59.2          -1.82  -147.0    57.55    148.28
1.2500E+09       -2.19   +96.8          -4.57  +173.5    182.55    -36.65
1.3000E+09       -0.65  +134.7          -10.31  +138.5    71.29    -11.77
1.3500E+09       -0.17  +167.2          -35.39  +154.8    51.56     -0.75
1.4000E+09       -0.49  +197.2          -11.17  -109.4    51.74     29.20
```

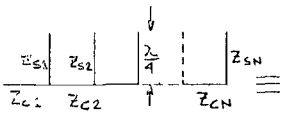
FIG. 11

V11

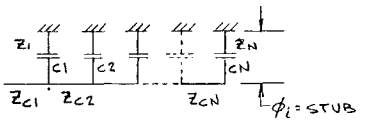
```
R, SNYDER
DISTRIBUTED BANDSTOP FILTER
                RL              50
1               PTL             Z0= 145.1 LENGTH= 7.5 VELOCITY
0                               1
2               TR              1E+09
0                               500
3               STL             Z0= 76.3 LENGTH= 7.5 VELOCITY
0                               1
4               PTL             Z0= 85.5 LENGTH= 7.5 VELOCITY
0                               1
5               TR              1E+09
0                               500
6               STL             Z0= 76.3 LENGTH= 7.5 VELOCITY
0                               1
7               PTL             Z0= 145.1 LENGTH= 7.5 VELOCITY
0                               1
8               TR              1E+09
0                               500
                RS              50
FREQUENCY       INSERTION LOSS          RETURN LOSS     INPUT IMPEDANCE
(HZ)            (DB)    ANGLE          REAL +J(IMAGE)
5.0000E+08      -0.11  +136.9          -15.46   +66.5     41.79     2.19
5.5000E+08      -0.11  +154.2          -14.04   +79.5     43.19    -2.69
6.0000E+08      -0.08  +173.7          -11.13   +96.3     46.28    -8.98
6.5000E+08      -0.04  +196.8          -8.57   +109.5     44.32   -14.62
7.0000E+08      -0.16  +225.8          -5.39   +119.6     38.85   -18.64
7.5000E+08      -1.35  +268.7          -3.39   +95.7      24.83    -7.77
8.0000E+08      -5.84  +319.1          -0.46   +66.4      2.48     3.09
8.5000E+08      -14.14   +1.8          -0.14   +65.5      0.50     0.54
9.0000E+08      -25.78  +34.2          -0.07   +49.1      0.26     0.72
9.5000E+08      +44.66  +60.7          -0.07   +25.4      0.22     0.56
1.0000E+09      -140.91  +76.5          -0.08    -5.4      0.23     0.78
1.0500E+09      +43.94 +300.5          -0.08   -45.1      0.26     1.05
1.1000E+09      -23.42 +327.0          -0.11   -79.1      0.36     1.48
1.1500E+09      -13.30 +289.7          -0.17   -70.0      0.73     1.25
1.2000E+09      -5.72   +42.5          -0.50   -86.8      2.74     0.38
1.2500E+09      -1.34   +92.7          -1.46  +100.0     10.68     1.98
1.3000E+09      -0.19  +134.2          -3.56  +108.7     27.64     4.76
1.3500E+09      -0.07  +163.9          -7.11  +109.3     44.58     7.03
1.4000E+09      -0.11  +186.9          -11.24   -97.8     46.19    11.09
```

FIG. 12

V12



RESONATOR SLOPE PARAMETER = $X_{Ji} = \frac{\pi}{4} Z_{Si}$



RESONATOR SLOPE PARAMETER = X_{Ji}

APPENDIX:

EQUIVALENCE OF $\lambda/4$ OPEN CIRCUIT (O.C.) STUB FILTER TO SHORT CIRCUITED, CAPACITIVELY COUPLED STUB FILTER WITH EQUIVALENT STUB LENGTH PLUS CAPACITOR PHASE SHIFT TOTALING $\lambda/4$.

SEE EQS (1) – (4)

(1) $X_{Ji} = \frac{\pi}{4} Z_{Si}$

(2) $F(\phi_i) = \phi_i \sec^2 \phi_i + \tan \phi_i$

(3) $F(\phi_i) = \frac{2X_{Ji}}{Z_i}$

(4) $\omega_0 C_i = \frac{1}{Z_i \tan \phi_i}$

FIG. 13

FIGURE 15
HIGH POWER 500 MHz BANDPASS FILTER

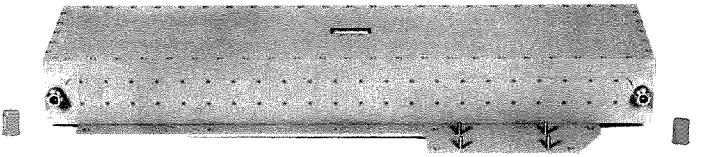
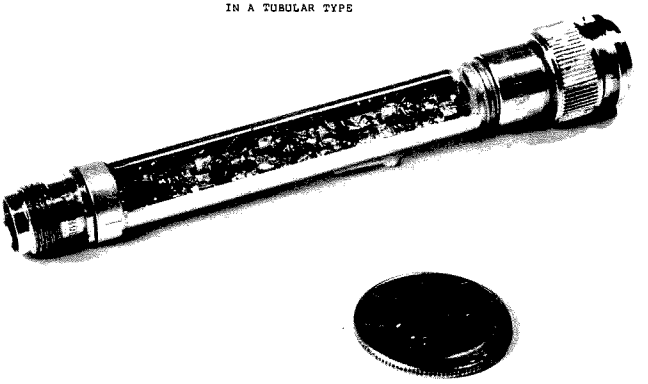


FIGURE 14
LUMPED ELEMENT BANDPASS
IN A TUBULAR TYPE



PART 1

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A Phase Lock Loop That Works - Almost Part 1.

So the system phase lock loop has been built. All the study and calculations are finished. The natural frequency and damping ratios have been set. The long awaited VCO is installed, and now the loop is closed.

Just as anticipated, it works. Well maybe it almost works. A few adjustments and it will be fine. Many adjustments and lots of frustrating hours later it still almost works.

Does this sound at all familiar? There seems to be a lot of phase lock loops that never fully meet the expectations of their creators. Some may have never worked at all or work only after an application of "black magic". In this article some of basic problems that keep a phase lock loop from working correctly will be examined.

Basics of Loop Problem Analysis

It is important to keep in mind that a phase lock loop is a phase/frequency domain system. The loop may be buried deep in a totally digital IC board and used to generate computer clocks for timing but it remains a phase/frequency domain system. Thus frequency measurement techniques must be employed to properly verify the operation.

Designers with a digital logic background frequently rely on clock jitter measurements observed on an oscilloscope as a primary trouble shooting tool. Unfortunately in most cases time domain observations tell only a small part of the whole story To understand and analyze the loop operation prepare to move into the frequency domain.

Three rules of experience can be used to guide loop trouble shooting and verification. These may seem at first to be almost trivial but a rigorous adherance will almost guarantee the expected PLL performance.

The first rule is that all components of the loop must work by themselves as intended. Not only must parts like the VCO and phase detector work as described in the spec sheets but they must work correctly when mounted in place on the circuit board. Most of these parts are sensitive analog components and require a bit of consideration. A phase lock loop running from a five volt logic bus surrounded by many watts of TTL or ECL circuits is in trouble already.

The second rule is that the components when connected together open loop must work perfectly. More about this later but suffice to say without perfect open loop operation, there is little hope for the closed loop.

The third rule applies in cases of modulated or pulsed signals. The loop must work as predicted for CW inputs or again there is small hope for operation with modulation.

If it can be accepted that these levels of perfection are required at each step, the PLL designer will have much higher success ratio and fewer of the almost loops.

Beginning Trouble Shooting

Phase lock loop circuits often have other extra circuits attached to them. Frequency search circuits and phase lock indicators are cases in point. These must be separated out early to get the loop down to its basics. Before a search circuit can be properly evaluated it has to be shown that the loop will

phase lock once the VCO and reference are brought within range.
A quick analysis of whatever problems the loop exhibits may point out a course of action. But a good place to start most trouble shooting is with the components.

The three essential components of any PLL are the phase detector, the loop filter and the VCO. Usually the VCO is the most difficult hardware design of these components. The loop filter may require the most analytical work but in terms of the required parts it is usually very simple. A good phase detector is somewhere in between. The design requires a mixture of analytical effort and hardware effort to meet the PLL requirements.

What Makes a Good VCO

For most considerations in a PLL, the actual operating frequency of the VCO is not a factor. Divider delays and very high fractional ratio loop band widths may require the loop frequency in the calculations. For the average loop these are not a problem. But these are second order effects. So the VCO is considered as a loop element with an input/output transfer function.

Most literature advocates taking three or four frequency measurements by changing the control voltage and from this deriving a gain factor Kv. Kv for most loop analysis is in rad/sec/volt so any frequency change/voltage change ratios must be multiplied by 2π to convert ΔHz/Δ volts to the value required for loop forward gain.

The few points usually recommended for frequency measurements are not enough to guarantee a design. Computer controlled measurement equipment now makes a hundred point sweep with a high resolution graph a job that can easily be done in less than a minute. The sweep should extend to the voltage limits that could ever possibly be expected in loop operation.
The graph should be examined very carefully for slope changes, flat spots or at worst slope inversions. The trace without exception must be smooth and monotonic over all input voltages. The oscillator power supply should be varied over its extremes and the graph rerun. If operation over temperature is required the graph should again be repeated.

Over the environmental extremes a simple lateral shift of the control curve can usually be corrected by the loop. Slight slope changes can usually also be handled. But extreme changes in either cannot be tolerated.

A spectrum analyzer is almost essential at this point for any serious investigation. Using a low IF bandwidth and narrow frequency sweep, the VCO output should be closely tracked across the control voltage range. Harmonicaly related spectral lines are to be expected. But lines that come and go that are not a multiple of main output should be looked into. Output variations with power supply and temperature extremes should also be checked. An oscillator does not have a little parasitic oscillation. Either it is clean or it has a problem. Any parasitic oscillation must be eliminated before using the VCO.

The VCO should also be checked over its full range for affects on the output by the load. Driving into any reasonable load the tuning must remain smooth with no breaks or discontinuities. Any tendency towards load pulling demands more isolation on the oscillator output. With a TTL output device this is as simple as adding another gate in series with the oscillator. Linear waveform units will require a pad or isolation amplifier.

Oscillator phase jitter is a parameter that is often ignored until it is too late. Logic clocks seem to exhibit a particular lack of concern. If the

frequency is right, the PLL must be right seems to be the rule. But this is not the entire story. Phase noise specifications may be derived from involved statistical processes but the effects of a noisy loop are obvious. Television pictures from a noisy sync scan are fuzzy on the edges. Clock gates that are supposed to arrive at a particular time occasionally don't make it. These are direct time domain examples of phase noise.

A PLL will attempt to clean up a VCO output and make it look like a replica of the input reference. But this action can only function inside the loop bandwidth. Outside the loop bandwidth, the VCO spectral output is basically unchanged. It looks like the free running output noise. A simple solution might seem to be to make the loop bandwidth as wide as possible and eliminate all noise. For a multitude of reasons this is not the solution.

The only solution that produces results is to use a VCO with the least possible noise that will fit the loop needs. At different frequency ranges, different oscillators are optimum. At a few MHz, typically current tuned RC oscillators are the noisest, LC varactor tuned oscillators are a big improvement and voltage controlled crystal oscillators are among the quietest. Figure 1 contrasts the spectral noise output of a standard current tuned RC DIP oscillator and a simple TTL varactor tuned LC oscillator. Although the observed spectral noise has AM and FM noise components, the overwelming majority of the noise power is concentrated in phase noise. The difference between the two oscillator output is obvious. The 40dB more noise from the RC oscillator was more than enough to keep a major computer system clock generator on hold until it was replaced with the LC oscillator.

Phase noise can only be properly evaluated with a spectrum analyzer. Observing time domain jitter on a clock edge for instance with an oscilloscope is a very subjective measurement. Differences between oscillator performance that can only be guessed at with an oscilloscope become as clear as the contrasting traces in Figure 1.

One last VCO characteristic that affects the loop operation is the modulation frequency response roll off. As previously mentioned the VCO is simply a block in a PLL. The output frequency is not a concern. The gain factor Kv is the DC gain factor for this block. The information that is missing is the poles and zeroes of the transfer function. This is not necessarily the same as the modulation bandwidth specifications. There does not seem to be wide spread industry agreement on the meaning and measurement of modulation bandwidth. There is virtually no information available on the actual VCO transfer function nor is there a recognized measurement method. In lieu of this the best choice is to specify a modulation bandwidth several times higher than the widest loop bandwidth anticipated. This will be disccussed in more detail later on.

A VCO must be constructed with special consideration. As mentioned, tight voltage regulation and output isolation are musts. It should be separated from digital circuits. Digital clock circuit paths should not cross the VCO layout area. Only with this type of special attention can a VCO be expected to perform as required.

A Phase Detector Check

The phase detector serves as the loop error detector providing error information for loop control. Two types of detectors are in frequent use; the balanced mixer

and the logic level frequency/phase detector. Each has distinct advantages and problems.

For any detector the phase conversion function should be verified. At and near the point of intended operation the input phase differential versus output voltage graph must be smooth and linear. The graph must be monotonic and free of any hint of flat spots or slope inversions. This point is a particular problem with logic level frequency/phase detectors.

Figure 2 is a simplified version of the logic level MC4344 type of detector. Recent articles have discussed in detail sampling delays through these devices. However Figure 2 will illustrate a more major problem. Figure 2 shows two negative edge triggered flip flops with a NAND gate for feedback to a common clear line. When both Q outputs go high the gate will clear the flip flops. When both inputs are at the same frequency and the falling edges line up the detector op amp output should declare zero phase. However, the time delay through the gate and through the flip flop clear produces some curious results. Since the time delay is fixed it represents a greater phase ambiguity at higher frequencies. Thus the 4344 type detector that works well at 100KHz is in real trouble at 10MHz. Phase flat spots at zero phase produce a zero gain slope. Some units have been observed to produce a reverse gain slope across a small region. This results in positive loop feedback and a loop oscillation in the positive feedback region. The VCO output will have a seemingly incurable jitter in this situation. The phase detector is being used beyond the maximum input frequency.

The mixer phase detector does not normally display crossover flat spots. It is likely to be used for tracking filters with analog inputs and most applications above 50MHz. Since this phase detector is not a frequency discriminator, an external search loop of some sort is usually employed. To evaluate the phase detector or the PLL, this search loop should be disabled and a manual method used to establish frequency proximity. This prevents one loop from interfering with the other.

As a loop element, the phase detector's DC transfer function is the slope Ko Δ volts/Δ phase evaluated at the intended operating point. With a mixer type phase detector this is shown to be A volts/rad when the beat note output is a sine wave of peak amplitude A volts. If the output is not sinusoidal, a spectrum analyzer will provide the fourier series coefficients. For a waveform with $V = A\sin\theta - B\sin 3\theta + C\sin 5\theta$-...reference 2 shows the slope Ko at zero volts to be

$$K_0 = A-3B + 5C-\ldots\ldots \text{ volts/rad.}$$

This allows accurate slope determination for any waveform. However, the slope will change if the loop does not hold at crossover or if mixer offsets cause zero volts output to not represent 90° or $\Pi/2$ radians. In either case the phase detector gain is reduced as the loop operating moves away from 90°.

Neglecting any cross-over problems, the frequency/phase detector has a more constant slope Ko over its range. This is a big advantage in extending acquisition bandwidth and in demodulation schemes. The output as shown is balanced. To provide a distinct point that can be labeled as the phase detector output a differential input op amp may be used. The input low pass network is used to roll off fast logic edges that are beyond the bandwidth capabilities of the following op amp.

Thus higher order mixer products are reduced before they can appear as side bands on the VCO output. This input rolloff along with any poles contributed by the op amp combine with Kv to form the complete phase detector block transfer function. In most cases these poles are inconsequential but in a wide band loop they may begin to nibble away at the phase margin.

The op amp could be eliminated and the double ended detector outputs be connected to a differential input loop filter. This has the advantage of saving parts but as will later be discussed some valuable trouble shooting and loop verification aids are greatly reduced.

Phase detectors of either type are fairly simple circuits. Their correct operation as a loop building block must again be carefully checked. A smooth, monotonic transfer curve is essential. This is the loop error detector. The loop can only correct with the degree of accuracy that this element can provide.

Loop Filter

The selection of loop filter values has been the subject of many excellent books and articles. Most of these deal with idealistic situations in which all loop parameters are available and well defined. References 3,4 and 5 are the exception in that many real world problems are clearly pointed out. The loop filter will contribute an additional pole at the origin to determine the loop type, but the order and in large part the phase margin are set by factors beyond the designer's immediate control. Through the combination of op amp poles and VCO modulation poles a type two second order loop is shown to quickly evolve to a fifth or higher order loop.

The loop filter is about the only part of the loop over which a designer has a great deal of control. Through a combination of analysis and measurement, the higher order effects may be accounted for and in many cases the loop bandwidth and phase margin re-established.

The loop filter remains though an op amp and just a few resistors and capacitors. Selection of an appropriate amplifier is important. PLL's above 25KHz in bandwidth normally will require a wide band op amp. An open loop DC gain of 100d8 or more with a first breakpoint no lower than 1KHz will keep loop phase margin degradation to a minimum. Narrower bandwidth loops do not require such wide band op amps.

The tradeoff from using a wide band op amp usually comes from its inability to provide exacting DC balance and low leakages and offsets.

Leakage currents restrict the magnitude of input resistors that may be considered. With higher leakage currents and if the input resistor value becomes to large, the resultant voltage drop can move the desired loop phase set point. Lower bandwidth amplifiers usually have much lower leakages and thus do not present a problem.

Another problem that may appear on a finished printed wiring board is bulk mode leakage through the board material. This can be a particular nuisance in a board with all the parts mounted in plated through holes. Tiny leakage currents from power supplies and other sources can combine at the op amp input and force the phase detector output to provide a balancing current. This current is produced by the phase detector output moving off ground with a resultant input/output phase offset. This problem is usually noticed when a breadboard loop filter built in some casual fashion works well with little

offset, but the finished product shows a phase skew.

The offset and resultant shift can be severly affected by temperature, humidity and the manufacturing processes to which the board is subjected. It can be a nuisance in a CW PLL and a disater in a pulsed or bandwidth switching loop. Leakage can also reduce the apparent DC gain. Without a pole at the origin, the loop is reduced to a high gain type one system. The phase error then shifts with frequency. Keeping the input resistors as low as possible will minimize the problem. Mounting critical elements with clinched leads in unsupported holes will also help.

As with the other loop elements the loop filter must work by itself as an integrator before including it in a PLL. Simple voltage step inputs to observe the ramp voltage, DC leakage tests for output drift and input offset measurements will verify the hardware.

In evaluating problems in a PLL remember changing filter values is probably the simplest thing that can be done. For most loops a designer does not need to retreat deep into system analysis to find the problem. If the hardware is functioning properly and the loop still doesn't work, there is probably a unknown pole or delay. Change the filter values. Drop the bandwidth and try it again. A stable bandwidth will come out of this where the loop will lock. Theory and measurement will meet. The simplicity of the loop filter provides the design slack to back the loop bandwidth down then carefully bring it back up while cataloging unkown disturbances along the way.

End Part 1 Phase Lock Loop Components

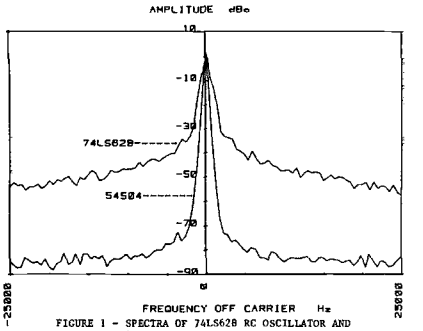


FIGURE 1 - SPECTRA OF 74LS628 RC OSCILLATOR AND 54S04 LC OSCILLATOR

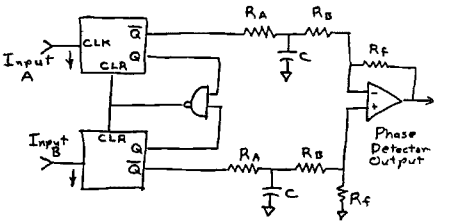


FIGURE 2 - FUNCTIONAL ILLUSTRATION OF LOGIC LEVEL FREQUENCY PHASE DETECTOR

VCO Tests
A Design Example

As part of a design example illustrating the techniques of this article, the problems and test data for a 1 MHz type two second order phase lock loop will be traced from the component test through the final closed loop data. The first item for test is the VCO.

The VCO is a varactor tuned circuit built expressly for illustrating various problems. The graphs and pictures represent actual measured data encountered during laboratory tests. Computer controlled test equipment has been extensively employed to create accurate, repeatable high resolution plots.

Figure A plots the frequency variation around 1 MHz versus the input control voltage for the VCO. This graphs seems to show a wide range of fairly constant slope from 0 volts to + 10 volts.

However, a slope analysis using a small moving window for a least squares linear regression curve fit produces the results of Figure B. This graph plots the slope of the curve in Figure A versus the input control voltage. A careful examination of Figure A will show small flat spots at about 0, 7.5 and 9.5 volts. These are dramatically pointed out in Figure B where the slope changes drastically at these points. The slope graph highlights what *might* easily be *missed* in Figure A. *Clearly* this is *not* acceptable. A spectral examination did in fact show the presence of parasitic oscillations at these points.

After the VCO circuit problems were corrected, the data for Figure C was recorded. The corresponding slope graph Figure D shows the slope is fairly constant between 4 volts and 8 volts. Figure E is new data for high resolution frequency at 1 MHz (0 Hz delta frequency). This plot still seems smooth and completely monotonic. Figure F bares this out. The slope data shows an almost constant slope from 5.5 volts to 7.5 volts. This will nicely center the VCO at 6.5 volts for 1 MHz operation with a slope Kv = 2660 Hz/volt.

Figure G is a spectral plot of the VCO with assorted parasitic oscillations. If the IF bandwidth of the analyzer is too high during a search for unwanted oscillations they may never be found.

Figure H is the spectral plot of the finished VCO. Note the lack of any hint of unwanted oscillations and the sharp clear center frequency spectral line *without wide noise skirts.*

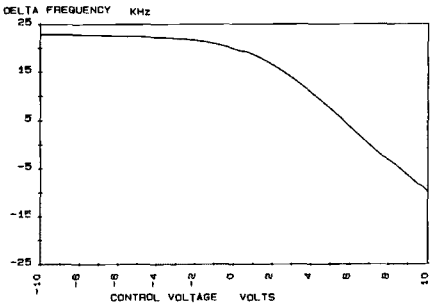


FIGURE VCO-A - TUNING CURVE OF 1MHZ VCO

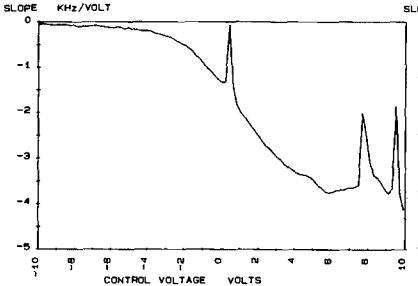


FIGURE VCO-B - SLOPE ANALYSIS OF 1MHZ VCO TUNING CURVE

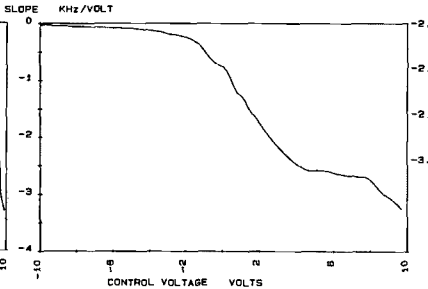


FIGURE VCO-D - SLOPE ANALYSIS OF VCO TUNING CURVE AFTER PARASITIC OSCILLATIONS WERE ELIMINATED

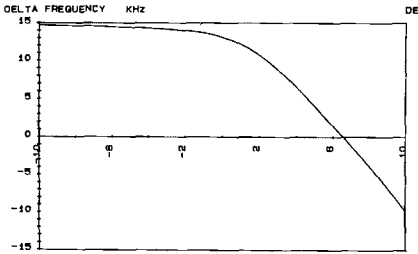


FIGURE VCO-C - VCO TUNING CURVE AFTER PARASITIC OSCILLATIONS WERE ELIMINATED

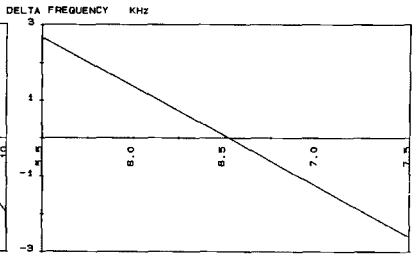


FIGURE VCO-E - HIGH RESOLUTION VCO TUNING CURVE AFTER CENTER FREQUENCY

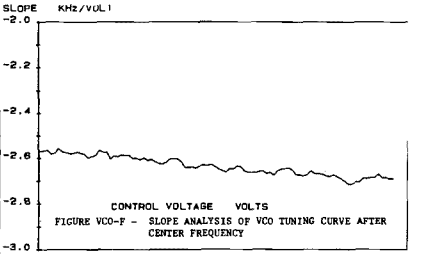


FIGURE VCO-F - SLOPE ANALYSIS OF VCO TUNING CURVE AFTER CENTER FREQUENCY

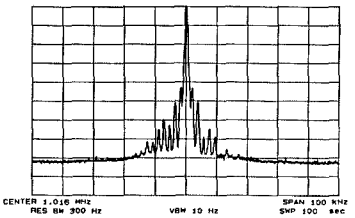


FIGURE VCO-G - VCO OUTPUT SPECTRUM WITH PARASITIC OSCILLATIONS

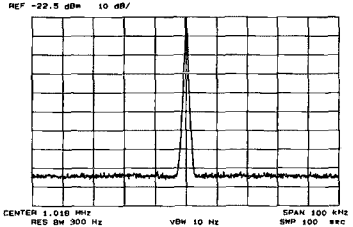


FIGURE VCO-H - VCO OUTPUT SPECTRUM AFTER PARASITIC OSCILLATIONS HAVE BEEN ELIMINATED

Phase Detector Tests

A double balanced diode mixer will work well as a phase detector. Figure A plots the output of a TO-5 50 ohm unit with 1 MHz inputs. The response is a smooth cosine wave with a zero crossing at 90 degrees. Figure B plots the slope of the data in Figure A using a linear regression least squares fit. It is important to note that the peak slope in volts/radian at 90 degrees from Figure B is equal to the peak voltage output at zero degrees from Figure A.

Figure C provides a high resolution look at the zero crossing area. Figure D plots the phase slope for the same region. Note that the slope is constant but with some curious dips. These dips would cause an open loop gain increase of about ten percent. Most closed loops could tolerate this without serious impact.

Figure E provides a wide phase sweep of a TTL frequency/phase detector constructed of 54F00 series gates with a differential input op amp.

Figure F shows the slope is constant at 2 volts/radian over $\pm$150 degrees except for the dip around zero degrees.

Figure G provides an expanded high resolution of the crossover region. Some of the problems caused by gate delays become apparent. These delays cause the rough, bumpy appearance of the trace. Figure H shows that the slope is indeed erratic around crossover. The slope at crossover is observed to be 3 volts/radian, a substantial increase over the wide sweep value of 2 volts/radian. This 50 percent increase in phase slope would cause a corresponding increase in open loop gain. Such an increase would seriously reduce the phase margin and stability of most loops if not properly accounted for. The slope data from the high resolution graph should be used in any closed loop component or stability calculations. This phase detector with a phase slope of 2.954 volts/radian will be used for this example.

Figure I illustrates the results from another version of the TTL detector that is currently in wide use. Note the flat spot between 0 and +2 degrees. In this region the phase gain is zero or slightly positive. A loop using this detector might lock but would oscillate within this 2 degree window. If this problem had not been discovered the output from a PLL using this detector would shake and no amount of loop bandwidth adjustment would help.

References

1. Floyd M. Gardner, "Phase Lock Techniques", 2nd Edition, John Wiley and sons, NY, 1979.
2. , "Phase Noise Measurements Techniques", Hewlett Packard, May 1982.
3. A.B. Przedpelski, "PLL Primer Part I", RF Design, March/April, 1983.
4. A.B. Przedpelski, "PLL Primer Part II", RF Design, May/June 1983.
5. A.B. Przedpelski, "PLL Primer Part III", RF Design, July/August, 1983.

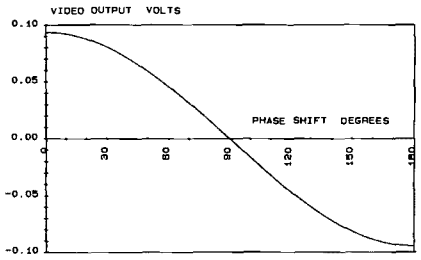


FIGURE PHASE DETECTOR-A - TRANSFER CURVE OF A DOUBLE BALANCED MIXER USED AS A PHASE DETECTOR

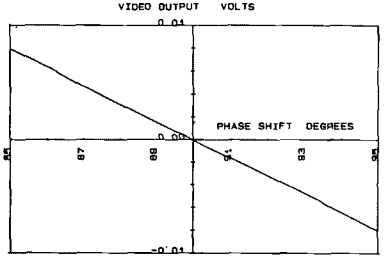


FIGURE PHASE DETECTOR-C - DOUBLE BALANCE MIXER PHASE TRANSFER CURVE AT ZERO VOLTAGE CROSSING

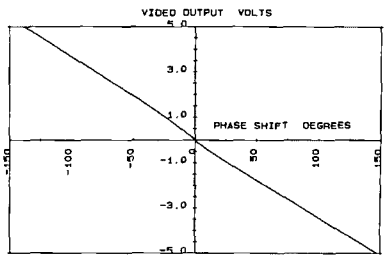


FIGURE PHASE DETECTOR-E - PHASE TRANSFER CURVE OF TTL PHASE DETECTOR

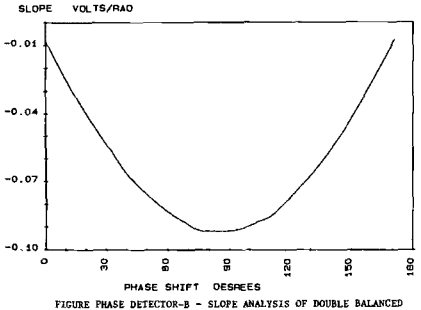


FIGURE PHASE DETECTOR-B - SLOPE ANALYSIS OF DOUBLE BALANCED MIXER PHASE TRANSFER CURVE

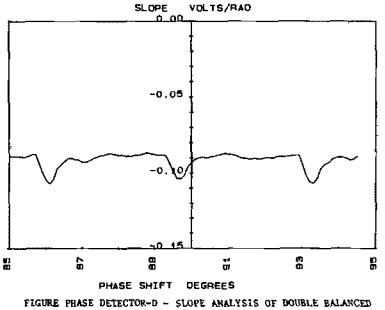


FIGURE PHASE DETECTOR-D - SLOPE ANALYSIS OF DOUBLE BALANCED MIXER AT ZERO VOLTAGE CROSSING

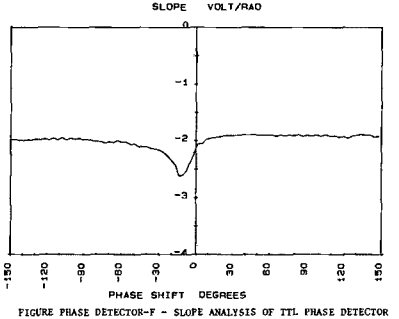


FIGURE PHASE DETECTOR-F - SLOPE ANALYSIS OF TTL PHASE DETECTOR TRANSFER CURVE

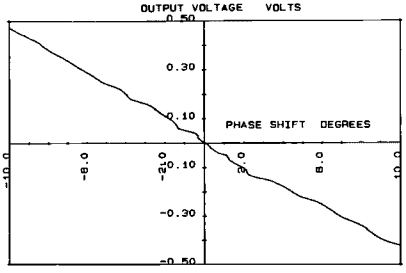


FIGURE PHASE DETECTOR-G - TTL PHASE DETECTOR TRANSFER CURVE AT ZERO VOLTAGE CROSSING

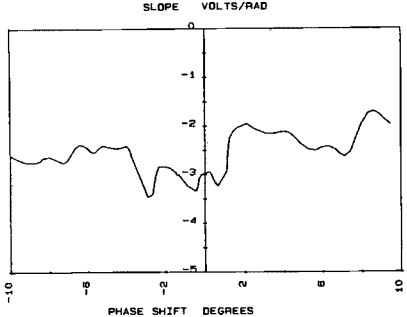


FIGURE PHASE DETECTOR-H - TTL PHASE DETECTOR SLOPE ANALYSIS AT ZERO VOLTAGE CROSSING

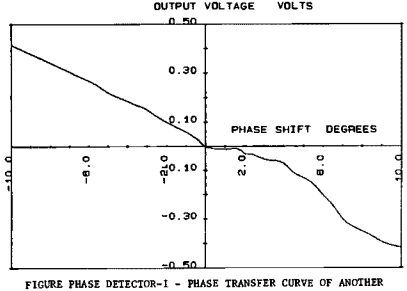


FIGURE PHASE DETECTOR-I - PHASE TRANSFER CURVE OF ANOTHER TTL PHASE DETECTOR

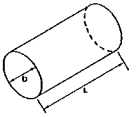


Figure 1. Cylindrical Waveguide of Length L.

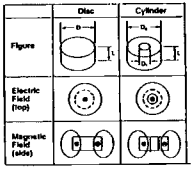


Figure 3. Typical Configuration Electric & Magnetic Fields

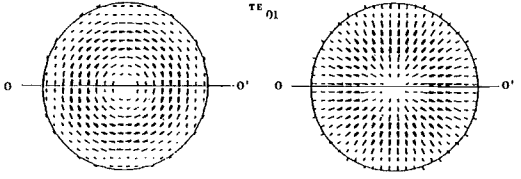


Figure 2. Transverse Electric Field (E) and Magnetic Field (H) for TE_{0i} Mode for infinite dielectric waveguide.

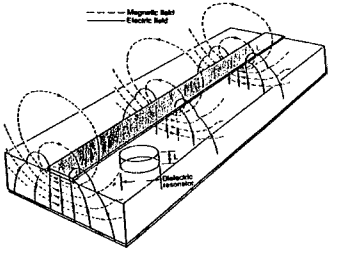


Figure 4. Fields Propagating Along Microstrip with Dielectric Resonator Nearby.

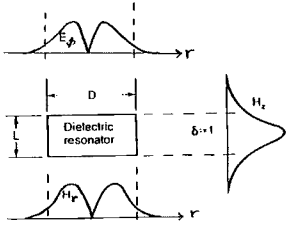
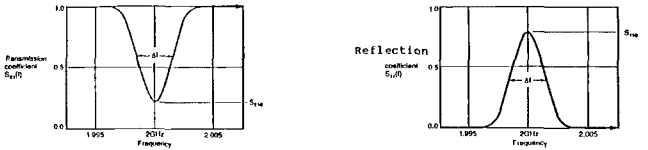


Figure 5. Approximate Field Structure for $TE_{01\delta}$ Mode in Free Space.



$$\beta = \frac{S_{11e}}{S_{11i}} = \frac{0.8}{0.2} = 4.0$$

Figure 6. (a) Transmission coefficient (b) Reflection Coefficient for Dielectric Resonator coupled to microstrip.

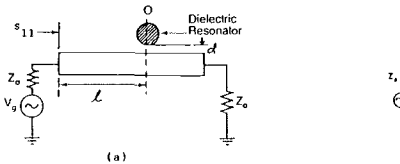


Figure 7. Microstrip of characteristic impedance Z_0 coupled to dielectric resonator (a) and its equivalent circuit (b).

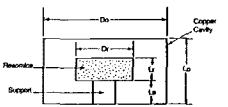


Figure 8. Test Set-up for Dielectric Resonator in Cavity

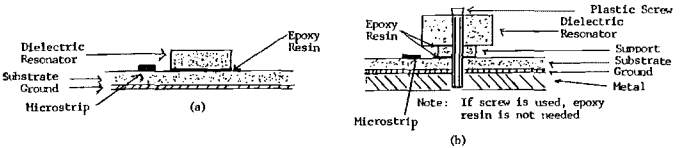
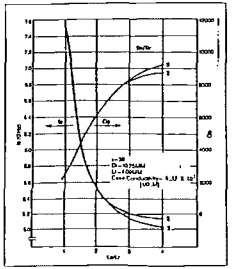


Figure 9. Mounting Systems for dielectric resonator on microstrip



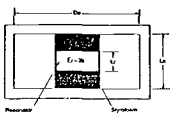


Figure 10. Illustration of the Effects of the Boundary Conditions on f_0, Q_0 for U Material Resonators (ϵ_r = 38).

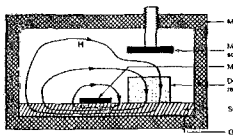


Figure 11. Dielectric Resonator on Substrate with Tuning Stub

CONSTRUCTION TIPS AND ENVIRONMENT FOR DIELECTRIC RESONATOR CIRCUITS

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Pennsylvania State University
Sponsored by MuRata Erie N. A.
Microwave/Technical Ceramics Group
August 18, 1986

This article is directed to the design engineer who wishes to use dielectric resonators in microwave circuit applications. The resonance cavity is first discussed and then some tips on choosing a dielectric resonator are provided. The effect of the environment on the electrical parameters of the dielectric resonator is developed. This is followed by a description of temperature variation and performance. The article concludes by describing a program disk for the IBM PC that is menu driven and helps the designer choose the appropriate dielectric resonator for his or her application.

METALLIC ENCLOSURE:

The concept of a resonator is a fundamental one of physics and applies to electric circuit performance as a function of frequency. A tuned circuit provides an impedance that changes with frequency but can be described as resonant at some frequency. This means that an electric circuit has some maximum or minimum impedance; this impedance can be in series or parallel (shunt). A metal resonant cavity has a precise resonance (actually a series of resonance modes) that is due to the modes that propagate in the cavity which satisfy the boundary conditions provided by the metal walls (Reference 1).

The metal resonant cavity, like a dielectric resonator, has an infinite number of resonances (modes) that depends on the length (L) and in the case of a cylindrical resonator the diameter (D) as shown in Figure 1. Similar resonant modes exist in a dielectric resonator, but the boundary condition for the dielectric resonator is the dual of the metal cavity.

The electromagnetic waves are confined to the metal container and satisfy the boundary conditions at the walls for a perfect electrical conductor and are such that the tangential electrical field vanishes at the surface of a conductor. To satisfy this boundary condition, the resonant cavity confines the electric field in a mode that is normal to the wall surface. Modes of the resonant cavity are field descriptions that are known to satisfy this boundary condition (Reference 1).

The boundary condition for the metal cavity where the tangential electric field vanishes may be considered a **SHORT** for an electric wall. A dielectric resonator has modes that satisfy the dual condition thought of as a magnetic wall where the tangential magnetic field vanishes and may be considered an **OPEN**.

These resonant modes are best understood by visualizing the resonant cavity shown in Figure 1 as a cylindrical waveguide of diameter D which has a length L. Thus, propagation in a metal waveguide is first developed in terms of modes such as TE_{01} and the end boundary condition requires that multiple half wavelengths for the cylindrical waveguide must be set up between the end walls. This provides that the third subscript, such as TE_{011}, is understood to be the TE_{01} cylindrical mode propagating such that one half wavelength in the cylindrical waveguide is equal to the length L.

Metal waveguides can propagate electromagnetic energy above some cutoff frequency in one or more modes that satisfy the boundary conditions at the walls of the waveguide. From cutoff to about 50% above cutoff, only one mode will propagate and this is used as the frequency band for a particular dimension waveguide. Circular waveguide is an appropriate starting description for the dielectric resonator because the ratios of the different modes are similar to that of dielectric resonators. A better model is a cylindrical dielectric waveguide that propagates energy through a dielectric with fields inside the dielectric as well as outside, but the fields outside must vanish at infinity. This allows the resonent modes to be specified for some length L as if almost all of the energy were propagating along a dielectric waveguide.

BOUNDARY CONDITIONS:

A microwave dielectric waveguide, like optical fiber, propagates energy along the guide with nearly all the fields confined within. Any fields outside the waveguide satisfy the boundary condition that fields go to zero at infinity. These fields are similar to a cylindrical metal waveguide and the modes are designated with the same convention. In Figure 2 the transverse electric field (E) and magnetic field (H) of the TE_{01} mode are shown in a dielectric waveguide having a certain rod diameter and frequency (Reference 2). The electric field (E) is in the ø direction and magnetic field (H) is in the r direction.

Assuming the energy in an infinite dielectric waveguide in Figure 2 is propagating in the z direction along the cylinder as shown in Figure 1, this TE_{01} mode (transverse electric) has no component of electric field but must have an H component in the direction of propagation. The two ends of the cylinder are considered an open circuit which reflects most of the energy in

the dielectric waveguide back such that the fields add constructively. This happens when the length is a approximate multiple of half wavelength in the dielectric waveguide.

The perfect magnetic boundary condition is an approximation that applies to the dielectric resonator for this particular field structure. For the cylindrical dielectric waveguide, H_r and H_z are perpendicular to the boundary at the surface. The electric field E_ϕ is tangential at the surface and must be continuous across this boundary.

The permeability μ_r of the dielectric resonator is the same as the free space value μ_o. However, the approximation of a perfect magnetic conductor considers a very large permeability μ so that the magnetic field at the boundary is perpendicular to the boundary. It is applied to the dielectric resonator TE_{01} mode because the symmetry of the magnetic field requires that H_r and H_z are normal to the surface for the cylindrical geometry.

A typical configuration for the electric and magnetic field is shown in Figure 3. This is consistent with the electric field in the ϕ diretion and the magnetic field in the radial direction shown explicitly in Figure 2. The magnetic field outside the dielectric resonator is somewhat dipole like as with a large component in the z direction which would be along the length of the cylinder L shown in Figure 1. The E_o and H_r component along the z axis of the cylinder are nearly zero so that a cylindrical hole of dimension D_1 has little affect on the field structure.

Thus, a dielectric resonator is a high dielectric material that has resonances inside the low loss ceramic material that stores the energy in a specific mode. A simple application is shown in Figure 4 where a resonator is placed near a microstrip which has a magnetic field propagating around the conductor and changes directions every half wavelength. The energy from the microstrip is coupled into the delelctric resonator through the magnetic field . For ϵ= 38, about 70 % of the magnetic energy is stored in the dielectric resonator and nearly all of the electric energy is stored inside the dieletric resonator (over 90 %).

The $TE_{01\delta}$ mode has a field stricture similar to a magnetic dipole as shown in Figure 3 where the magnetic field lines are directed along the axis of the dielectric resonator and couple primarily into the top and bottom of the dielectric resonator. Once the energy is coupled into the dielectric resonator, much of it is confined to the dielectric resonator in the $TE_{01\delta}$ resonant mode. The $TE_{01\delta}$ is usually but not always the fundamental mode; under certain conditions it may be the second or third mode.

The magnetic field can couple into the top and bottom of the dielectric resonator providing an H_z component. Consider the field shown in Figure 5 for the $TE_{01\delta}$ mode where the length of the resonant cavity (L) is some multiple δ of half wavelengths. The fields are drawn in a plane through the middle of the dielectric resonator as shown by OO' in Figure 2. H_r and H_z are perpendicular to the boundary and E_ϕ is parallel to the boundary. The dielectric resonator has a soft boundary condition, i.e. the tangential component of electric field E_ϕ and magnetic field H_r and H_z nearly vanishes at the boundary. The magnetic field H_z is normal to the surface at the end of the boundary of the cylinder as shown in Figure 5.

DIELECTRIC RESONATOR ON MICROSTRIP:

As the fields move down the microstrip as shown in Figure 4 and interact with the dielectric resonator, the resonator stores energy in the ceramic material at the resonant frequency and causes a deep notch in the transmission coefficient as shown in Figure 6(a). The reflection coefficient on the other hand peaks at this resonant frequency because the energy stored in the dielectric resonator couples back into the microstrip but travel in the opposite direction as shown in Figure 6(b) (Reference 3).

Assuming a lossless case the sum of the complex reflection coefficient and complex transmission coefficient must be unity (Reference 3):

$$S_{11} + S_{21} = 1 \qquad (1)$$

The real quantities representing the reflection coefficient S_{11o} and transmission coefficients S_{21o} at the resonant frequency of the dielectric resonator can be used to determine the coupling of the dielectric resonator to the microstrip by:

$$\beta = S_{11o}/S_{21o} = R/2Z_o \qquad (2)$$

and the width of the peak at half value is Δf which relates to the unloaded quality factor (Q_U) of the entire system by:

$$Q_U = f_o/\Delta f \qquad (3)$$

The coupling factor β depends on the distance d of the dielectric resonator from the microstrip line and the location of the dielectric resonator along the microstrip as shown in Figure 7(a). As the distance d is increased, β decreases. Changing the length ℓ ,causes a rotation on a Smith chart of the input reflection coefficient S_{11} into the microstrip. Thus, by changing d and ℓ of the dielectric resonator location with relation to the microstrip, any impedance can be realized looking into the microstrip at the generator. This allows a matching circuit of any value to be generated by a dielectric resonator along a half wavelength microstrip line (Reference 3).

The microstrip with a dielectric resonator in Figure 7 acts as a band reject filter and can be modeled by an

equivalent circuit shown in Figure 7(b). A parallel resistance R, inductance L and capacitance C can be used to model the dielectric resonator coupled to the microstrip of characteristic impedance Z_0. Microwave analysis programs such as Touchstone, Super-Compact and Microwave SPICE have the capability to use parallel or series RLC networks to model these devices. However, the designer *must determine* the values of R, L *and* C from the information contained in Equations (2) and (3).

The boundary conditions at the edge of the dielectric resonator do not completely control the resonant frequency because there is energy stored in the field outside of the dielectric resonator. Thus the interface with the substrate is important to the coupling of energy into the dielectric resonator. The metal container that houses the system also becomes part of the resonant circuit and affects the resonant frequency of the dielectric resonator. A dielectric resonator in free space will have a lower resonant frequency than the same material enclosed in a metallic box. In particular, the top and bottom of the cylinder have a large effect if the metallic plate is nearby because the energy cannot couple into the top and bottom of the dielectric resonator.

The support is shown in Figure 8 that holds the dielectric resonator away from the bottom. Ideally, the resonator is equally spaced in the middle of the metal enclosure and the enclosure is as large as possible. Some tuning can be accomplished by moving the dielectric in the metal enclosure and the dimensions of the cavity become more important in the calculations of the resonant frequency.

The quality factor of the resonator Q is affected by the metallic enclosure because energy is absorbed by currents in the non-ideal conducting walls (Reference 4). The amount of surface current in the walls depends on the field structure that is affected by how far away the dielectric resonator is. Basically, the better conductivity of the walls, the higher the Q, and the lower loss within the ceramic material generates a higher Q.

MOUNTING:

Mounting the dielectric resonator on the substrate, the type and thickness of the substrates affects the resonant frequency and the loaded Q the same way the metal container and support affected the resonant frequency. The boundary condition is considered a dielectric constant of ϵ_0 outside of the ceramic material so setting the dielectric resonator on the substrate changes the boundary conditions at the substrate resonator interface. In addition, since the substrate is usually thin (20 to 60 thousandths of an inch), the boundary conditions are changed considerably by the metal ground at the base of the microstrip. In particular, this affects the amount of coupled magnetic field that exists in the microstrip substrate coupling into the bottom of the resonator (see Figure 4).

The boundary conditions at a metal wall demand that the tangential electric field vanish, but the dielectric wall boundary conditions require the tangential magnetic field to be vanishingly small; a dual condition. Thus, the metal wall in close proximity to the top of a dielectric cylinder causes drastic changes in the resonant frequency. This condition often comes into effect when a dielectric resonator is placed on a thin substrate. This is the one reason that the dielectric support is used to couple the magnetic field into the dielectric resonator; the other reason is the Q of the system is affected. Since the currents in the metal enclosure cause loss and degrade the Q of the system, the dielectric resonator is best placed equally distant from the metal conductors.

Figure 9(a) shows the usual mounting method of dielectric resonators for Microwave Integrated Circuit (MIC) applications. The dielectric resonator Q_d is deteriorated by epoxy resin, therefore the amount used should be kept to a minimum. In this mounting method, the unloaded quality factor, Q_u, of the device is a function of the Q of the dielectric resonator, cavity and substrate:

$$\frac{1}{Q_u} = \frac{1}{Q_d} + \frac{1}{Q_c} + \frac{1}{Q_s} \quad (4)$$

Another way of mounting the dielectric resonator is shown in Figure 9(b) which uses a support and a plastic screw. Sometimes the screw is not used and the epoxy resin fastens the dielectric resonator and support to the substrate. The configuration shown in Figure 9(b) raises the resonator above the substrate and allows for better coupling through the ends for the magnetic field generated by the microstrip. This method provides the highest unloaded Q_u that is approximately equal to that of the dielectric resonator:

$$Q_u = Q_d \quad (5)$$

TUNABILITY:

The dielectric resonator has an inherent resonant frequency that is determined in a test chamber and is provided by the manufacturer as in Table 1. The ratio of the Length (L_r) to Diameter (D_r), is kept nearly constant at about 0.45 which is chosen for mode separation and performance considerations. The resonant frequency ranges are about 8% for each of MuRata Erie's Part Numbers listed in the table. The resonators are supplied to the lowest frequency of this range. The frequency is measured by the test configuration in Figure 10. A different cavity will have a different resonant frequency for the same dielectric resonator.

In Figure 10, the resonant frequency and unloaded Q are shown as a function of L_o/L_r. It is seen that for L_o/L_r greater than 3 the frequency ranges between 5.0 and 5.2 GHz and the Q_u between 8300 and 9300. For ratios of frequency L_o/L_r less than 3, variation in frequency is possible but the Q deteriorates rapidly down to 2000. This is due conductivity losses in the cavity walls.

Several methods to adjust the resonant frequency are as follows:

(1) Change the boundary conditions

   a) Change cavity dimensions
   b) Using tuning stub

(2) Change length L_r of the dielectric resonator.

The most typical approach is to purchase a dielectric resonator from the manufacturer that is pretuned at the lowest frequency as those shown in Table 1.

The resonant frequency can be adjusted by the use of a tuning stub as shown in Figure 11. Typically 3% variation in frequency can be achieved with acceptable Q in many applications as shown in Figure 10.

A second method of tuning is accomplished by moving the dielectric resonator along the microstrip by a distance ℓ or moving it perpendicular to the microstrip a distance d as shown in Figure 7. In general, walls that are more than 3 times the dimensions of the resonator (L_r for height and D_r for radial distances) have little effect on the resonant frequency.

A third method is to change the length of the dielectric resonator L_r physically by grinding. This increases the frequency and can be accomplished by the user or the manufacturer. The manufacturer (MuRata Erie N. A.) can supply dielectric resonators custom machined to the actual dimension. In this case a correlation test cavity should be provided by the end user.

TEMPERATURE COMPENSATION:

The manufacturer can supply a variety of temperature coefficients within a material to compensate for any variance of the substrate or metallic wall due to temperature. These structural changes will change the resonant frequency of the system. By adjustment of the TC of the resonator, the designer can compensate for these effects so as to stabilize frequency with respect to temperature.

The designer usually starts out with a 0 TC dielectric resonator and then measures the variation of the system through the desired temperature range. The dielectric resonator can then be changed to compensate for any variances.

CONCLUSION:

In this article, the physical operation of the dielectric resonator particularly on microstrip inside a metal container has been examined. The resonant frequency is slightly tunable by the location of the dielectric resonator with respect to the microstrip. The size of the container and its location with respect to the dielectric resonator, microstrip and substrate are seen to be important considerations. How does a designer determine what particular dielectric resonator to use?

A computer program has been developed for the IBM PC that stores the particular dielectric resonator dimensions available from MuRata Erie,N. A. for the designer to choose. This program has routines available that calculate the eigenvalues for a configuration from the characteristic equation (Reference 4) by an approximation from Reference 5. The program is menu driven and asks the designer for the dimensions of the cavity, the substrate thickness and dielectric constant. It then calculates the resonant value for this configuration and picks a dielectric resonator from available values for this particular design.

The designer will still have to use the dielectric resonator in a circuit to generate a matching network for an oscillator or filter, but he or she now has the dielectric resonator that is desired for a particular frequency range. The temperature compensation should be done for the system starting with a zero temperature coefficient of frequency and determining the temperature variation and then compensate for it by varying the temperature coefficient of the dielectric resonator. In short, the dielectric resonator offers a unique component in microwave circuits that have a known response at a particular frequency but little affect below that frequency. These dielectric resonators have very high Q so there is little loss in the dielectric resonator even at the resonant frequency. Some tuning is available to adjust for variations in FET or other component values. The resonator is mechanically stable and does not change with time. Many possible uses are available in microwave circuits. It is up to the designers imagination to develop and use this unique component.

ACKNOWLEDGEMENT:

The author wishes to thank T. Nishikawa, J. Fijedziuszko, R. Bonetti, and A Khanna for their technical evaluations of this paper. T. Sudo, J. Alberici and my students at the Pennsylvania State University have provided valuable insight into the information needed by design engineers.

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(2) Kajfez, D. "Model Field Patterns in Dielectric Rod Waveguide", Microwave Journal, May, 1983.

(3) Soares, R., J. Graffeuil and J. Obregon "Applications of GaAs MESFETs", Artech House, Dedham, MA, 1983.

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Dimensions and Frequency Range

TABLE 1

Dr ±0.05 (mm)	Lr ±0.05 (mm)	Frequency Range*(GHz)
4.65	2.06	11.46-12.45
5.06	2.24	10.54-11.45
5.50	2.44	9.69-10.53
5.98	2.65	8.91-9.68
6.50	2.88	8.20-8.90
7.07	3.14	7.54-8.19
7.69	3.41	6.93-7.53
8.36	3.71	6.38-6.92
9.09	4.03	5.87-6.37
9.88	4.38	5.40-5.86
10.75	4.77	4.96-5.39
11.68	5.18	4.56-4.95
12.70	5.63	4.20-4.55
13.81	6.13	3.86-4.19
15.02	6.66	3.55-3.85
16.33	7.24	3.27-3.54
17.76	7.88	3.00-3.26
19.31	8.56	2.76-2.99
21.00	9.31	2.54-2.75
22.83	10.13	2.34-2.53
24.82	11.01	2.15-2.33
26.99	11.97	1.98-2.14
29.35	13.02	1.82-1.97
31.91	14.15	1.67-1.81
34.70	15.39	1.54-1.66

* Frequency is measured under the condition: Lr/Lo = 0.33

ADDENDUM

Typical Applications

Typical applications of dielectric resonators are dielectric filter and dielectric resonator oscillators. The following references are papers presented by Murata Manufacturing Co., LTD. regarding dielectric resonators.

(a) K. Wakino, K. Minai and H. Tamura, "Microwave Characteristics of (Zn,Sn) TiO_4 And BaO-PbO-Nd_2-TiO_2 Dielectric Resonators", J. Amer. Cer. Soc., 67, No. 4, pp. 278-281 (1984).

(b) H. Tamura, T. Konoike, Y. Sakabe and K. Wakino, "Improved High-Q Dielectric Resonator With Complex Perovskite Structure", Comm. Amer. Cer. Soc., 67, No. 4, C-59-61 (1984).

(c) K. Wakino, T. Nishikawa and Y. Ishikawa, "800 MHz Band Channel Dropping Filter Using TM^0_{10} Mode Dielectric Resonator" IEEE MTT-S International Microwave Symposium, IEEE Cat. No. 84CH2034-7, pp. 199-201 (1984).

(d) K. Wakino, T. Nishikawa, S. Tamura and H. Tamura, "An X-Band GaAs FET Oscillators Using A Dielectric Resonator", Proceedings of Ffequency Control Symposium (1983). (In print.)

(e) K. Wakino, T. Nishikawa, H. Matsumoto and Y. Ishikawa, "Quarter Wave Dielectric Transmission Line Duplexer For Land Mobile Communications", IEEE MTT-S International Microwave Symposium, IEEE Cat. No. 79CH1439-9, pp. 278-280 (1979).

(f) K. Wakino, T. Nishikawa, H. Matsumoto and Y. Ishikawa, "Miniaturized Bandpass Filters Using Half Wave Dielectric Resonator With Improved Spurious Response", IEEE MTT-S International Microwave Symposium, IEEE Cat. No. 78CH1279-5, pp. 230-232 (1978).

NON-LINEARITY EFFECTS IN RF CIRCUITS

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Abstract

This paper illustrates how to derive a model and evaluate key non-linearities for an amplifier and a voltage controlled oscillator (VCO), using a commercially available non-linear Computer-Aided Design (CAD) program called mwSPICE™.

Introduction

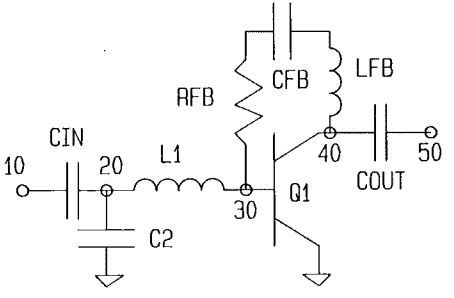
RF and microwave circuit performance can be simulated and accurately predicted using linear analysis programs, provided that the circuit elements are fairly linear. Non-linear elements such as bipolar or field effect transistors are usually modeled in a linear analysis program using small signal S-parameters, which assume the device is operating over a fairly linear region.

These linear programs do not, however, take into account the effects of temperature, harmonics (either generated by the device or introduced into the device), bias supply variations, gain compression or distortion. Some of these effects can be estimated with linear analysis programs but they are strictly done by linear approximation.

This paper focuses on how to use mwSPICE for two different devices, an amplifier and an oscillator, and evaluate device non-linearities. First, amplifier non-linearities which are evident by evaluating the power handling capabilities of a device are presented. Second, critical VCO characteristics such as start up transients, settling time, and frequency versus voltage response are evaluated to insure that steady state oscillation occurs as expected, and that the VCO is operating over a fairly linear range.

Amplifier Design

In this example we've designed a 400 MHZ to 1000 MHZ 16 DB Gain Amplifier as shown in Figure 1.



.4-1GHZ 16DB GAIN AMPLIFIER

FIGURE 1

The amplifier uses a NEC02135 bipolar transistor biased at VCE=10Volts and IC=20ma. As with any linear analysis program, the data for the transistor comes from the manufacturer's data sheet S-parmmeters. The gain response is shown in Figure 2 and the input and output match is in Figure 3.

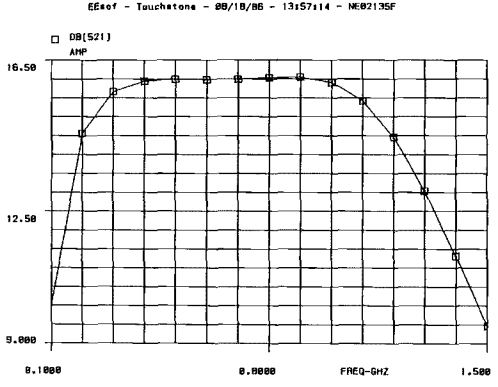


FIGURE 2

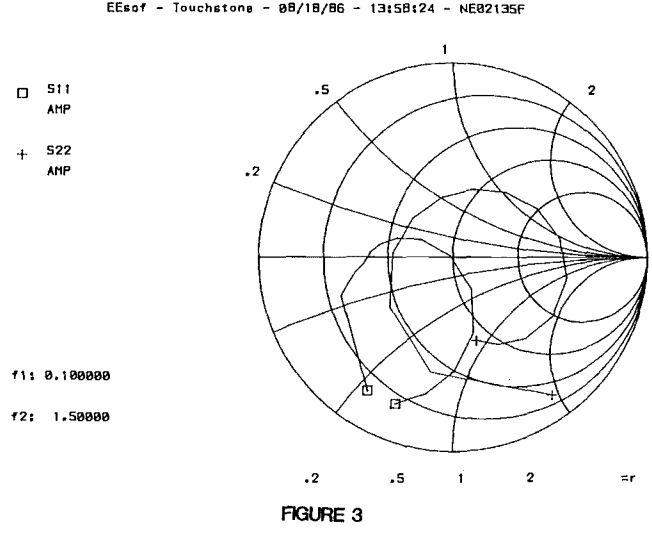


FIGURE 3

In order to look at the non-linear characteristics, we will construct a Touchstone/MWSpice circuit file as shown in Figure 4.

```
! 400-1000MHZ Amplifier with 16DB gain
CKT                                          ! Circuit for Touchstone/MWSpice
 CAP_CIN   10 20   C=46.7                    ! Input Network
 CAP_C2    20  0   C=6.29
 IND_L1    20 30   L=1.89
 IND_LL1   30 31   L=1.5          ! Bipolar Transistor VCE=10V IC=20MA
 S2PA_Q1   31 40 70   NE02135.S2P [MODEL=NE02135]
 IND_LFB1  70  0   L=0.3
 RES_RFB   30 33   R=235                     ! Feedback Network
 IND_LFB   33 37   L=5.60
 CAP_CFB   37 40   C=400
 CAP_COUT  40 50   C=14.7                    ! Output Network
DEF2P 10 50 AMP
FREQ                                         ! Touchstone Frequencies
 SWEEP .1 1.5 .1
OUT                                          ! Touchstone Analysis Outputs
 AMP S11
 AMP S22
 AMP DB[S21] SR1
 AMP K
MODEL                                                ! Spice Model for Q1
 NE02135 NPN
 + IS=346.5E-18
 + BF=94.57   IKF=174.9M NF=1.008  ISE=7.101F NE=1.595
 + BR=2.770   IKR=244.4M NR=1.004  ISC=2.953P NC=1.467
 + VAF=27.43 VAR=4.747
 + EG=1.11    XTI=3.0     XTB=0.0
 + RE=1.849   RB=1.2136   RC=1.742        RBM=1.0
 + CJE=4.69P  VJE=558M    MJE=37.65M      FC=0.5
 + CJC=.556P  VJC=316.4M  MJC=34.91M      XCJC=0.35
 + CJS=.56P   VJS=.82     MJS=0.5
 + TF=18P     XTF=0       PTF=38.2   ITF=1.0    TR=.18N
 + AF=1       KF=0
 + IRB=8.2P VTF=1.5
SOURCE                                               ! Bias and RF Sources
 AMP IVS_VCC   100    0 DC=20                        ! VCC=20V
 AMP RES_RCC   100   40 R=472                        ! Collector Bias
 AMP RES_RBB1 40    30 R=75B7                        ! Base bias
 AMP RES_RBB2 30     0 R=B61                         ! Base bias
! RF Input Source
 AMP IVS_VIN   3     0 AC=1 TRAN=SIN(0 .63 7E9) PWR=(-40 -40 0 7E8 7E8 0)
 AMP RES_RIN   3     7 R=50                         ! Input Load Resistor
 AMP IVS_V1    7    q0 DC=0                         ! Power sensing point
 AMP RES_ROUT 50     0 R=50                         ! Output Load Resistor
CONTROL
 AMP AC LIN 15 100MEG 1500MEG                       ! Small Signal Analysis
 AMP TEMP -55 25 125
 AMP TRAN 10PS 4NS 0 10PS                           ! Transient Analysis
 AMP PWR IVS_VIN RES_RIN                            ! Power Analysis
 AMP FOUR .7B V(50)                                 ! Fourier Analysis
SPICEOUT
 AMP AC V(ALL) I(ALL)                               ! Small Signal Output
 AMP TRAN V(ALL) I(ALL)                             ! Transient Output
 AMP PWR IVS_VIN 3 0 IVS_V1 10 0 RES_ROUT 50 0    ! Power Analysis Output
```

FIGURE 4

This circuit file will allow the circuit to be analyzed either in Touchstone or mwSpice. The Model section is added to characterize the device parameters for MWSpice. Also biasing aust now be included along with a signal source.

The first non-linear response measured is a standard curve tracer response, Figure 5, of collector current versus collector voltage as determined by base current. In this case base current was varied from 0 to 1 milliamp in .1 milliamp steps. Also plotted is the DC load line for this circuit and the maximum limits based on the manufacturer's data sheet. The maximum VCE is listed as 12V; the maximum collector current is 70 milliamps, and the maximum power dissipation for this package style is 290 milliwatts at 25 degrees centigrade. A point of interest is that the data sheet lists S-parameters for a bias condition of VCE=10V and IC=30ma for this package whioh is outside of their own power dissipation liaita at 25 degrees centigrade, to say nothing of 85 or 125 degrees.

If we were planning to use this amplifier with a 0 dbm input signal and expecting to get 16 DB gain, think again. Figure 6 shows that as the input power in dbm (the X axis) is increased, the gain decreases from about 16 DB at -40 DBm in, down to 11.5 DB gain with 0 DBbm in. Figure 7 shows a time domain analysis of the output waveform with 1-milliwatt (0 DBm) input. As you can see there is a significant amount of distortion on the waveform.

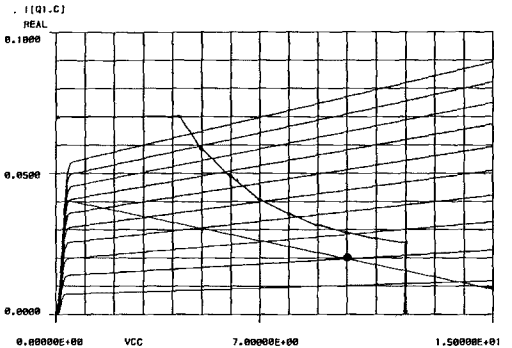


FIGURE 5

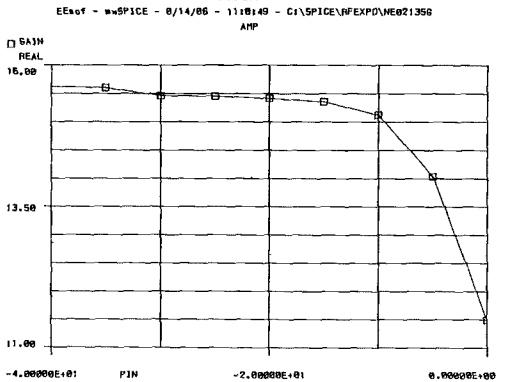


FIGURE 6

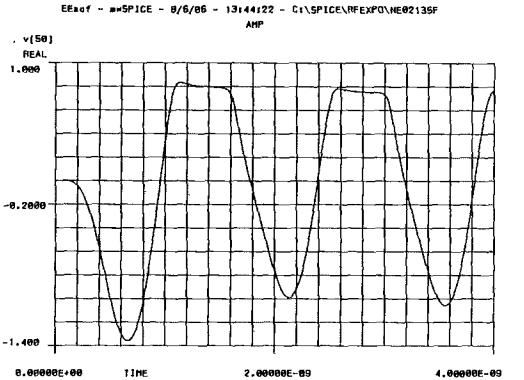


FIGURE 7

And as you'd expect a fourier analysis reveals the second harmonic is only about 14DB below the fundamental as shown below.

**** FOURIER ANALYSIS TEMPERATURE = 27.000 DEG C

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(50)

DC COMPONENT = 4.244D-02

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	DB BELOW CARRIER
1	7.000D+08	9.541D-01	1.000000	
2	1.400D+09	1.929D-01	.202218	-13.89
3	2.100D+09	1.017D-01	.106567	-19.45
4	2.800D+09	8.223D-03	.008619	-41.29
5	3.500D+09	2.324D-02	.024357	-32.27
6	4.200D+09	1.263D-02	.013239	-37.56
7	4.900D+09	3.082D-03	.003230	-49.82
8	5.600D+09	5.324D-03	.005580	-45.07
9	6.300D+09	2.091D-03	.002192	-53.18

TOTAL HARMONIC DISTORTION = 23.051669 PERCENT

In Figure 8 the performance of the amplifier was analyzed at -55, 25, and 125 degrees centigrade. It can be seen that gain varies about +/-.5 DB over that temperature range. Different biasing methods could be quickly tried if temperature stability is a concern.

In this quick overview you can see that ignoring non-linearities can result in unpleasant surprises when the actual circuits are built. By using a non-linear design tool such as mwSpice we can analyze effects that would have required a considerable amount of time and equipment to bench test.

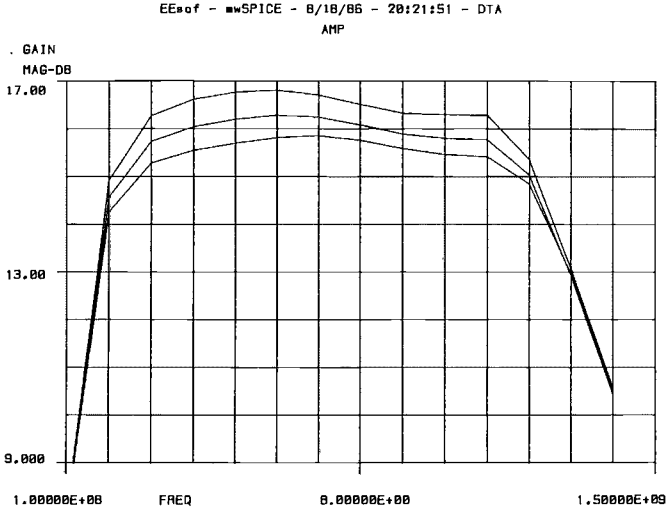


FIGURE 8

Voltage Controlled Oscillator, VCO

Linear analysis programs have been used in the past for oscillator design. Typically, the design procedure is to maximize the small signal S-parameters, S11' or S22', so that the real part of the device reflection coefficient becomes negative. Linear analysis programs use optimization algorithms to maxiaize S11' or S22', as determined by the design. So, to design an oscillator using a linear analysis program requires device small signal S-parameters to characterize the active device.

With non-linear analysis programs such as mwSPICE, device characterization consists of supplying AC and DC parameters, as well as proper biasing conditions as shown in Figure 9.

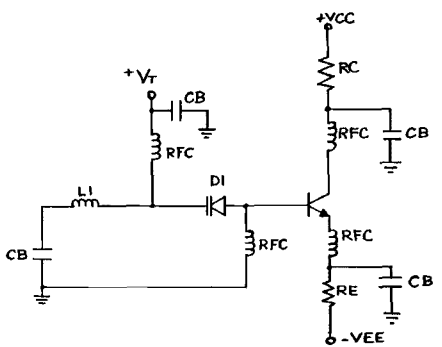


FIGURE 9 VCO Schematic

The idea of the VCO is to vary the tuning voltage applied to diode D1 which will change the junction capacitance of the diode (the diode, when used for it's variable capacitance properties is referred to as a varactor). This will in turn, change the resonant frequency of the equivalent resonant AC network consisting of the series inductance, the internal diode capacitance, and the transistor internal capacitance. The complete circuit description is shown in Figure 10.

```
DIM
  FREQ MHZ          OSC IVS_VEE 31 0 DC=-10
  CAP PF            OSC IVS_VCC 41 0 DC=10
  IND UH            OSC IVS_VT 20 0 DC=10
VAR                 OSC RES_RE 30 31 R=930
  CE=1000           OSC RES_RC 40 41 R=1000
  RFC=100
CKT
  CAP_CBP1 1 0 C*CB
  IND_L1 1 4 L=4.55
  IND_LRFC1 4 20 L*RFC
  CAP_CBP2 20 0 C*CB
  S1PA_D1 4 5 [MODEL=DIODE]
  IND_LRFC2 5 0 L*RFC
  S2PA_Q1 5 6 7 [MODEL=T2N918]
  IND_LRFC3 7 30 L*RFC
  CAP_CBP3 7 0 C*CB
  RES_LN 3 6 L=3.82
  RES_R2 6 0 R=1510
  CAP_CR2 6 0 C=826
  CAP_CN 3 0 C=79.6
  CAP_CBPL 3 7 C=1000
  CAP_CBPC 2 0 C=1000
DEF1P 7 OSC
MODEL
      T2N918 NPN( BF=69.47 C2=39.3 NE=1.5 IK=0.025
+ IS=1.55E-15 VA=100.0 VB=20.0 BR=0.573 C4=0.0 NC=1.5 IKR=0.025
+ CJC=1.75E-12 MC=0.120 PC=0.800 CJE=2.22E-12 ME=0.150 PE=0.500
+ RC=11.500 RE=12.000 RB=8.50 TF=2.14E-10 TR=3.27E-08 )
        DIODE D IS=1E-15 CJO=.5PF TT=.1NS
SOURCE
```

Figure 10. Circuit description of VCO

The *Gummel-Poon* model for a 2N918 bipolar junction transistor is used in thia exaaple, with the parameters indicated in Figure 11.

BF=59.47	Ideal aaxiaum forward beta
C2=39.3pf	B-B leadage saturation current
NE=1.5	B-E leakage emission coefficient
IK=0.025	Forward knee current
IS=1.55E-15	Transport saturation current
VA=100.0	Forward early voltage
VB=20.0	Reverse early voltage
BR=0.573	Ideal aaxiaua reverse beta
NC=1.5	B-C leakage eaiasion coefficient
IKR=0.025	Reverse knee current
CJC=1.75E-12	Zero bias B-C junction capacitance
MC=0.120	B-C grading coefficient
PC=0.800	B-C junction built-in potential
CJE=2.22E-12	Zero-bias B-E juntion capacitance
ME=0.150	B-E grading coefficient
PE=0.500	B-E junotion potential
RC=11.500	Collector resistance
RB=12.000	Base resistance
RE=8.50	Emitter resistance
TF=2.14E-10	Forward transit tiae
TR=3.27E-08	Reverse transit time

Figure 11. BJT paraaeters

The initial transient solution for the VCO, shown in Figure 12, indicates sustained oscillation after approxiaately 8 nanoseconds. Start-up transients don't seem to be a problea.

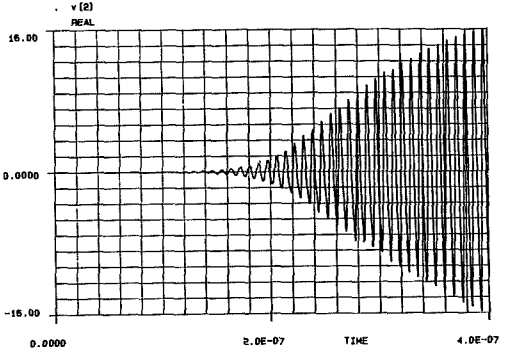


Figure 12. Initial Transient Solution

Another parameter of concern to oscillator designers is the output power versus frequency as shown in Figure 13. By varying the tuning voltage, we can predict the output power for different frequencies of oscillation.

Figure 13. Output power versus frequency

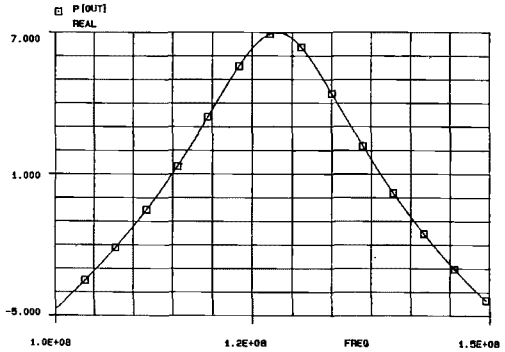


Figure 13. Frequency versus Pout

A response of the collector current versus output power, shown in Figure 14, is useful to evaluate the sensitivity of the oscillator to variations in supply current. Although mwSPICE doesn't really have a "tune" mode, alternately saving S-parameters at different collector currents allow the required data to be graphically evaluated on a single plot.

Figure 14. Oscillator power versus collector current

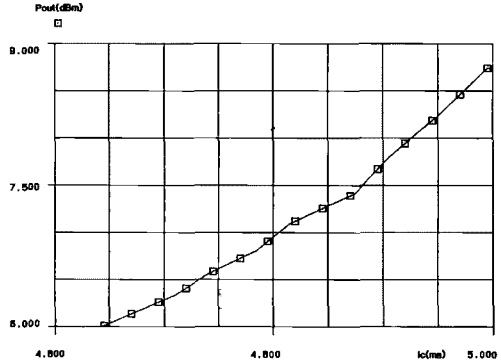


Figure 14. Ic versus Pout

Summary

This is a summary of the non-linear analysis techniques that can help the RF design engineer more exactly predict circuit performance, thus reducing design time, costs and frustration.

References

1. Gary Franklin, "Oscillator Design Using the Device Line Method and Load Pull Method:, RFEXPO 86 Proceedings, pp. 251-259.

2. Hewlett-Packard Application Note 994, "A 2GHz Power Oscillator Using the HXTR-4103 Bipolar Transistor".

3. EEsof

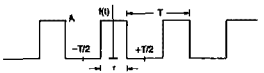
4. Compact Software

A CRYSTAL CONTROLLED FREQUENCY AND AMPLITUDE CALIBRATOR

by
Dan Baker
Tektronix, Inc.

The motivation for creating this circuit was to provide a calibrator for both amplitude and frequency over a reasonable range of the HF band. Most modern receivers use frequency synthesis and would receive little benefit from a frequency calibrator. However, older receivers and spectrum analyzers need frequency calibration and virtually all receivers would benefit from a broad-band amplitude reference. This circuit accomplishes these goals with a simple design that is fundamentally accurate requiring no adjustments.

The design is based on narrow-width pulses with 1 MHz and 100 MHz repetition rate. For a theoretical analysis, consider the following time function:



The double-sided Fourier coefficients for this function are:

$$F_n = \frac{1}{T}\int_{-T/2}^{T/2} f(t)e^{-jn\omega_0 t}dt = \frac{1}{T}\int_{-\tau/2}^{\tau/2} Ae^{-jn\omega_0 t}dt$$

$$F_n = \frac{2A}{\omega_0 nT}\left[\sin\left(\frac{\omega_0 n\tau}{2}\right)\right] = \frac{A\tau}{T}\left[\frac{\sin\left(\frac{\omega_0 n\tau}{2}\right)}{\left(\frac{\omega_0 n\tau}{2}\right)}\right]$$

This is of the general form:

$$F_n = \frac{A\tau}{T}\left[\frac{\sin(X)}{(X)}\right]$$

where $X = \frac{\omega_0 n\tau}{2}$

The famlliar [sin(x)]/x function is shown below:

The function is zero at integral multiples of π. The first zero occurs at:

$$X = \pi = \pi nF_o\tau$$

$$nF_o = \frac{1}{\tau} = \text{first null frequency}$$

A spectrum analyzer or receiver measures the magnitude of F_{ω}. The frequency response $|F(\omega_0)|$ for a rectangular pulse train is a series of impulses in the frequency domain as follows:

$$|F_{\omega_0}| = \sum_{n=1}^{\infty} \left|2A\tau F_o\left[\frac{\sin X}{X}\right]\right| \delta(\omega - n2\pi F_o)$$

where $X = \pi F_o n\tau$

$F_o = 1/t$ = the pulse repetition rate.

The envelope of the frequency response is dependent only on the pulse shape and not the pulse repetition rate (F_o). If the pulse is rectangular and of ahort duration, the resulting response may be quite flat over a portion of the frequency band before the first zero.

The circuit shown in Figure 1 generates a pulse of approximately 8 nsec in duration. The pulse duration is loosely controlled by the propagation delay through the inverter and D flip-flop. A more consistent pulse width could be obtained with a 74S04 instead of the 74LS04. However, as will be shown, this is not neceaaary to meet the design goals.

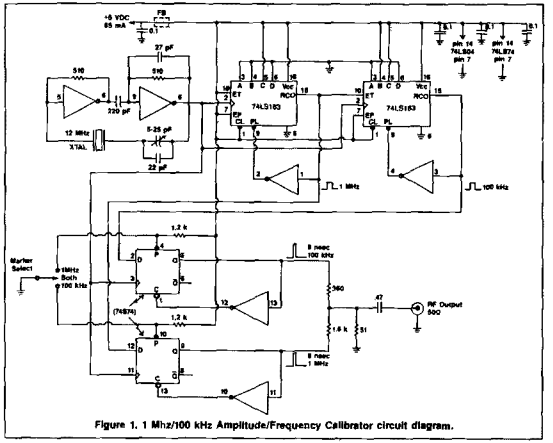


Figure 1. 1 Mhz/100 kHz Amplitude/Frequency Calibrator circuit diagram.

Figure 1. 1 MHz/100 kHz Amplitude/Frequency Calibrator circuit diagram.

An 8 nsec pulse width would provide the following flatness error at 50 MHz.

$$\text{Error} = 20 \log \left[\frac{\sin\left(\frac{50}{125}\pi\right)}{\left(\frac{50}{125}\pi\right)} \right] = -2.4 \text{ dB}$$

This is actually a worst case since 1) the pulse is typically narrower and the first zero greater than 125 MHz, reducing the error at 50 MHz, and 2) the D flop-flop is not capable of generating a very narrow rectangular pulse. The pulse is rounded and, due to slew rate limiting, better approximated by a triangular pulse. This spectrum is flatter than the (sin x)/x frequency response and this effect further reduces the amplitude flatness error at 50 MHz. The measured error of the prototype circuit was < 2dB.

CIRCUIT DESCRIPTION

To provide markers at 1 MHz and 100 kHz, two programmable synchronous counters are used. Crystals at 12 MHz are readily available and most work well in the TTL inverter oscillator shown. The trimmer capacitor is adjusted to calibrate the oscillator to a frequency standard.

The first counter divides by 12 and the second by 10. The two D flip-flops generate the 8 nsec pulses so that 1 MHz and 100 kHz markers can be generated simultaneously or separately. The 12 MHz oscillator synchronously clocks the two D flip-flops as well as the counters. This allows the 100 kHz pulses to occur precisely coincident with every tenth 1 MHz pulse. This is necessary for proper in-phase addition of the two spectra when both 1 MHz and 100 kHz markers are to be generated.

The desired output power for the calibrator is -60dBm for the 100 kHz markers and -50 dBm for the 1 MHz markers (Figure 2.)

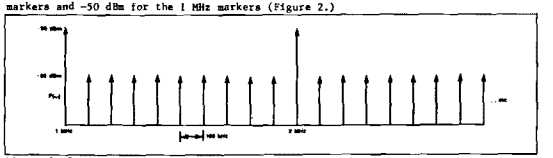


Figure 2. Output spectrum

This is rather high for most narrowband receivers and the output may need padding for "S" meter calibration. For the 100 kHz spectral components, the required output into 50 ohms is:

$$-60 \text{ dBm} = 20 \log \frac{V_{50}}{224 \text{ mV}}$$

$$V_{50} = 224 \ \mu V_{rms} = 317 \ \mu V \text{ peak}$$

This requires an attenuator on the output of the TTL flip-flop. The values are then calculated as shown in Figure 3a. It is desired that the 1 MHz markers be 10 dB above the 100 kHz marker amplitudes. The attenuator for the 1 MHz markers is shown in Figure 3b.

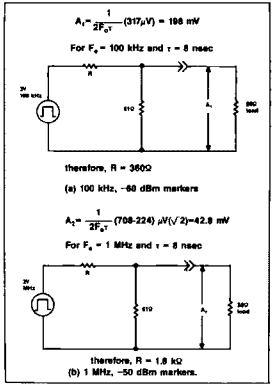


Figure 3. Determination of attenuator resistor values.

Note that when both markers are present, the 1 MHz markers will be 3.3 dB higher than the amplitude when generated alone. This is due to the in-phase addition of the 1 MHz components of both spectra.

PROTOTYPE RESULTS

Figures 4 through 8 illustrate the measured results of the prototype. Figure 4 is the double sided (sin x)/x magnitude response. Note that the first zero is slightly higher than 125 MHz indicating the pulse width is slightly less than 8 nsec.

Figure 5 shows the first 50 MHz of the spectrum and illustrates the predicted flatness error of about 2dB. Note that the 12 MHz component is too high. This is probably due to crosstalk in the hex inverter. A separate XTAL oscillator would probably eliminate this error at the expense of more parts.

Figures 6, 7 and 8 show a 5 MHz segment of the first 30 MHz. Figures 3 and 4 show the 100 kHz and the 1 MHz markers when selected separately. Figure 5 shows the composite calibrator output. Note that the marker amplitudes are about 10dB different, as predicted. Also note that the 1 MHz markers are about 3dB lower (Figure 7) when selected individually, as was also predicted.

One note of caution is in order. Receivers have a limited voltage dynamic range at their inputs. Pulses much larger than the ones used in this design can overload a receiver input. If very fine resolution markers are desired using this technique, it would be prudent to consider a chirp or other more complex technique to obtain a flat spectrum with good signal-to-noise ratio.

This circuit provides a cheap, yet quite accurate calibrator of both amplitude and frequency over the 30 MHz HF band. It can serve as a general purpose reference for a general cover receiver or spectrum analyzer.

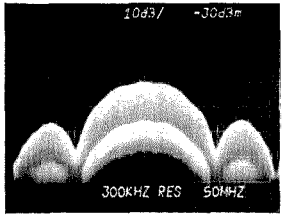


Figure 4. Double-sided (sin x)/x spectrum of the calibrator.

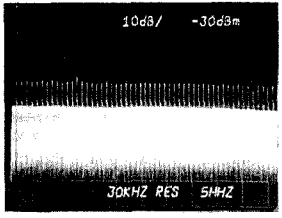


Figure 5. 0-50 MHz markers, showing approximately 2dB flatness error at 50 MHz.

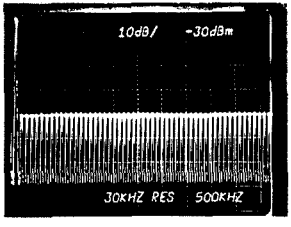


Figure 6. 100 kHz markers, from 0-5 MHz at -60dBm.

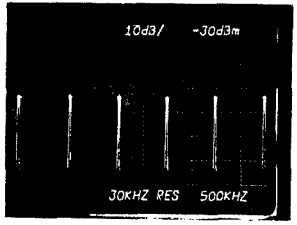


Figure 7. 1 MHz markers, from 1-6 MHz. Note level at about 3dB below -50dBm.

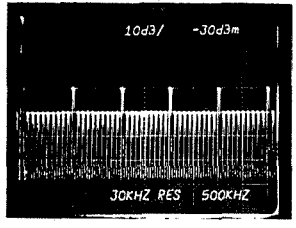


Figure 8. Both markers combined, 0-5 MHz, showing accuracy of amplitude.

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January 15, 1986

GENERAL PRICE DETERMINANTS for R.F. & Microwave Filters

by Dr. R. A. Wainwright, Chief Scientist
Cir-Q-Tel, Inc.

Abstract: Prudent selection of an r.f. or microwave filter in general requires a great deal of forethought.

Price is usually not an insignificant consideration. Function, however, must necessarily take precedence - it is worthwhile for anyone who must necessarily select system components to give substantial consideration to those devices that shape their system's selectivity as to frequency and/or time domain performance. Given tractable specifications then, one can consider price - it goes without saying that one may over- or under-specify the system's filtering-functional responses - both are expensive in many respects. Rational compromises are usually necessary. The following list of items has been generated as a "General Guide" for systems/subsystems engineers. Please retain this list as a "thought jogger" whenever you find it necessary to consider the use of and/or specify selective devices --- filters for use in systems. It is hoped that by reviewing this list you may be reminded of essentially all of the considerations you must weigh as a responsible engineer as you imagine/conceive/engineer/document and pass off to manufacturing "your design" for use and review by your customers. Like it or not, your name, pride, ego and reputation is inextricably connected to every device you pass on for use by others.

If this list will help you through the maze, then perhaps in some way Cir-Q-Tel will have been of good service to you - we certainly hope so. Please review this list frequently. The factors listed here are very important.

LIST OF GENERAL PRICE DETERMINANTS FOR FILTERS

Not Necessarily in Their Order of Importance
and not Necessarily All

For Lowpass, Highpass, Bandpass and Band Reject Filters

1. Topology, i.e., the general network form for realization as might relate to schematic/type of network, i.e., Lowpass, Highpass, Bandpass, Band Reject, Diplexer, Multiplexer, Reflective or Absorptive Filter, etc.
2. fo or fc and tolerances
3. Bandwidth or % BW and tolerances
4. Complexity or n, sometimes called "degree"
5. Zo
6. Connectors or connections for input and output
7. Temperature, range and stability
8. Vibration and shock environment
9. Relative humidity, salt spray, corrosion protection, mold growth, etc.
10. Altitude or pressure requirements
11. Power: peak and average, cooling provisions: conduction, convection, forced air, etc., e.g. fundamental power, harmonics and power levels of harmonics
12. Load and source impedance conditions
13. Minimum expected life of performance (MTBF)
14. Plating or finishes required
15. Mounting requirements
16. Physical form of network and container shape & size of network: filter
17. If tunable then: range, how tuned, range of tuning, control of parameters over tuning range
18. Quantity
19. Delivery: time and method
20. Warranties
21. Inspections: source, destination, qualification, sampling, etc.
22. Documentation: class, level, detail
23. Time (group delay) and phase requirements - frequency domain
24. Step and impulse requirements - time domain
25. Amplitude-Frequency requirements, including noding: absorptive loss, selectivity
26. VSWR: Return Loss-frequency requirements

(continued)

Price Determinants (continued)

27. Leakage of r.f. energy requirements
28. Competitive marketplace influences
29. EMP specifications
30. General class of filter: Butterworth, Chebishev, Elliptic, Gaussian, etc.
31. Switching, if switching is to be used: Electromechanical/Electronic/Mechanical
32. Ultimate rejection,necessary reject band levels and frequency "width"(s) of reject band(s)
33. Functional elements: (a) materials: metals, ceramic, plastics,
    (b) type of resonators, interdigitated, comb line, waveguide, ceramic, (possibly) SAW, etc. or for lowpass and highpass, the physical manifestation of the schematic circuit(s).
    (c) coupling means
    (d) coupling and element tolerances required; generally tolerances required may be estimated from:
    % $\pm$ tolerances: $\pm$ T (L, H): Lowpass Highpass
    $\pm$ T (B, R): Bandpass, Band Reject
    [1] $\pm$ T (L, H) $\sim$ 15/n
    [2] $\pm$ T (B, R) $\sim$ 15/2n
    Where 'n' is the number of elements/resonators: the "degree" of the network - understandably some tuning and tweaking mechanisms/means may necessarily need to be included in the device design to compensate for unavoidable element/coupling variations.

As an aside: one must be fully aware of other methods of construction: ceramic resonators vs. waveguide resonators for example. In general a well constructed narrow band filter using ceramic resonators may well be superior in performance and lower in cost than a waveguide filter that may be suitable for the same application or a SAW filter (in quantity) may be, and usually is, substantially lower in cost and has superior time domain properties over an equivalent helical resonator filter, etc.

A New Double-Balanced Mixer of High Dynamic Range Improves System Performance

by
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ABSTRACT: A new mixer technology which offers low distortions for both inputs enables system designers to significantly improve wideband system performance.

A new mixer technology (patent applied for) has been developed by Bertronics in which each input port has low distortion that is largely independent of the other port signal. This property offers the system designer significant possibilities for improving performance of high performance designs.

To utilize these advantages, this new mixer requires different operating conditions from conventional diode mixers. In order to illustrate how these conditions can be met and how this mixer can be used to advantage, we will illustrate its use in receiving and signal analysis applications.

THEORY

Figure A shows a schematic for a bridge attenuator. If R2*R1=Z*Z, then both ports are matched to Z and the attenuation is

$$V2/V1=(R1-R2)/(R1+R2+2*Z)=(R1-Z)/(R1+Z).$$

A perfect mixer would have V2/V1 proportional to another input voltage. However, synthesizing R1 and R2 to meet the above conditions would be difficult.

Figure B shows a solution to this problem. If port 2 is terminated in 0 ohms and R1||R2=Z/2, then port 1 is matched to Z and the attenuation is

$$I2/V1=(1/R1-1/R2)/2$$

$$I2/I1=(Z/R1-Z/R2)/2.$$

If V2 is a voltage source and port 1 is terminated in Z, then

$$V2/V1=(Z/R1-Z/R2)/4.$$

It is not difficult to make the conductance of circuit elements vary in proportion to a voltage. Hence, a mixer with linearity in both inputs can be constructed.

Since the minimum R1 and R2 is Z/2, the minimum losses are I2/V1=1/Z, I2/I1=1, and V2/V1=1/2. There are hidden sources of loss in linear mixers. In addition to the 3dB image loss, there is an additional 3dB loss due to the fact that the local

oscillator input would be driven with a sine wave and the RMS value is .707 of the peak value. Notice that there are no intrinsic limitations on the conversion loss from the port controlling the conductance of the circuit elements.

THE MIXER

Figure C shows the connection diagram and preliminary specifications for the Bertronics FD50 Mixer. The bias terminals should be biased at about -20 volts (relative to the port 3 pins) to provide an impedance for ports 2 and 3 of 50 ohms. Adjustment of the bias voltages adjusts the port impedance; the greater the voltage, the lower the port impedance. Adjustment of the voltage between the bias terminals (less than 50 millivolts) provides a fine adjustment of Port 2 to Port 3 isolation. The substrate should be connected to approximately +10 volts. Both the substrate and the bias pins are high impedance inputs, and should not be subjected to static charges.

Port 1 of the FD50 mixer is an input with approximately 5 pF of input capacitance and several hundred ohms of parallel input resistance. Port 2 is an isolated winding with an impedance of 50 ohms (as adjusted by the bias voltage). Port 3 should be balanced with respect to the bias and substrate pins. It has an impedance of 50 ohms.

Ports 2 and 3 are similar in that if one is deliberately mismatched to a low impedance, then the other is resistive (VSWR < 1.5). Port 3 has response down to DC but port 2 does not. If the mismatched port impedance is not relatively low, then the conversion loss and noise performance suffer and VSWR is sensitive to port 1 signal level.

One input's distortion products are largely independent of the other input. Hence, the mixer can be modeled as two nonlinear functions of the inputs followed by a perfect multiplier (Figure D). That is why there are two sets of distortion specifications. Port 1 presents a problem for input intercept specification because this input is mostly capacitive. Therefore, we have expressed this number in volts.

Instead of conversion loss we specify a transmission constant and equation relating input and output voltages and mixer impedance. This equation demonstrates the programmability of the mixer. The conversion loss between two ports is proportional to the signal level of the third. Conversion loss is not a meaningful specification, however, as only one port is terminated resistively in normal operation.

INTERFACING

Although these port impedances may seem difficult to work with at first, they can actually be used to advantage in some designs. For lower frequency applications, Port 1's high input impedance allows high signal voltage levels to be reached with little input power. For higher frequency applications, it is desirable to resonate this capacitance in order to reduce the signal power requirements.

Both ports 2 and 3 present 50 ohms and, although one of them is deliberately mismatched, the amplifiers should be designed for good noise performance at 50 ohms. Figure E shows an example of a broadband design. This circuit will have optimum noise performance if biased at the same current as one optimized for common emitter noise performance. FETs can also be used.

SIGNAL RECEPTION / ANALYSIS

Port 1 of the mixer can be used to advantage in receiver applications. For lower frequency RF inputs, the signal can be transformed up, enabling the mixer to have conversion gain (Figure F). This can eliminate the need for RF amplification and enable the system to have a low overall noise figure. The disadvantage of this configuration is that substantial LO power is required.

In heterodyne applications, the low levels of harmonics for both inputs to the mixer reduce the spurious responses of the receiver. If the IF is high, it can be matched to the amplifier with a quarter wave length transmission line (Figure G). The parallel inductor and capacitor are used to short the port at all other frequencies.

Use in direct conversion is where the mixer offers the greatest improvement over conventional mixers. The low level of harmonics of both ports (if the LO has low harmonic content) means that harmonic mixing is greatly reduced. Low level amplification at 50 ohms at baseband can present problems also. Figure H shows a practical circuit for low noise, low impedance amplification. The circuit uses very low noise transistors (PMI MAT-02) in a feedback circuit to lower the input impedance to .04 ohms. Compensation is provided by the shunt input capacitor. This compensation also lowers the input impedance at higher frequencies. Op amps could be used with a penalty in noise performance (Figure I). Here again, compensation is provided by the shunt input capacitor. This pole should be located much lower than any poles in the Op amp transfer function in order to ensure stability.

The independence of the distortion functions of the inputs can be used to advantage in a unique AGC circuit. In a conventional diode DBM, reduction of the LO level results in drastic reduction of the third order input intercept point. This degradation in performance does not occur with the new mixer. Hence, we can reduce the gain of the mixer without affecting impedances or other parameters. Figure J shows a system with a PIN diode attenuator interposed between the local oscillator and the mixer input. If the attenuator were on the RF or IF side, noise and distortion performance would suffer. The performance of the circuit in Figure J is limited by the mixer and the IF amplifier. The amplifier can be designed for fixed gain, for instance using feedback. This allows higher performance than could be achieved with a voltage controlled amplifier.

PHASE COMPARISON

The low DC offset of the mixer suits it to use as a phase comparator. If used with a sine wave phase reference, the mixer can be used to lock onto low level signals with greatly reduced risk of harmonic locking due to its low distortion. In synthesis applications, the reduced levels of harmonics enables spectral purity to be achieved with less filtering.

CONCLUSION

We have introduced Bertronics' new mixer technology. The dissipative mixer should be considered as a new component in order to exploit its advantages for high performance system design. It offers a degree of linearity to RF and Microwave designs which was previously available only below 1MHz.

Bertronics **Model MFD50**

Preliminary Preliminary Preliminary Preliminary Preliminary

Double Balanced Mixer

FEATURES

- o Wide Bandwidth
- o High Power Capability
- o Low Distortion

```
      3 2 1
   4        12
   5        11
   6        10
     7 8 9
    Top View
```

Pin 2 - Port 3
Pin 3 - Port 3
Pin 5 - Substrate and Case
Pin 6 - Bias
Pin 7 - Port 1 input
Pin 8 - Bias
Pin 11 - Port 2
Pin 12 - Port 2

MAXIMUM RATINGS (Voltages relative port 3 common mode voltage)

Bias Terminals	-40	V
Port 1 Voltage	±10	V Peak AC (AC coupled)
Port 2 Voltage	±20	V
Port 2 Current	±100	mA
Port 3 Voltage	±20	V
Port 3 Current	±100	mA
Power Dissipation @ 250C	2	Watts
Derate Above 250C	16	mW/0C

OPERATING CHARACTERISTICS (.5-500MHz)

Port 1 Capacitance:	5 pF
Port 2, 3 VSWR @ 50 Ohms (Port 1=0V)	1.5
Isolation, Port 2 to Port 1:	40 dB
Isolation, Port 2 to Port 3:	30 dB
Isolation, Port 1 to Port 3:	40 dB
Transmission Constant T	.8
I3=T*V1*V2/Z3/(VBIAS-2.5V)	
Two-Tone Third Order Input Intercept Point:	
Port 2 or Port 3 @ 30MHz	+39dBm
Port 1 @ 30MHz	25 VRMS
Current, Bias Pins	10 uA
Current, Port 3 Pins to case	10 uA

Specifications apply with Bias pins @ -20V and case @ +10V

Figure C.

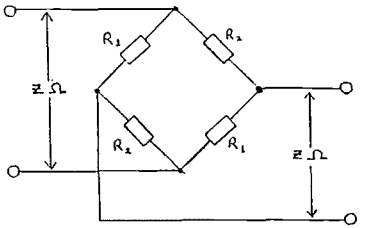


Figure A. Bridge Attenuator

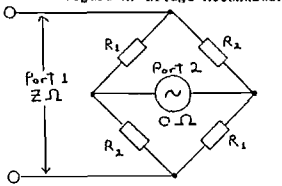


Figure B. Bridge Attenuator with low impedance port

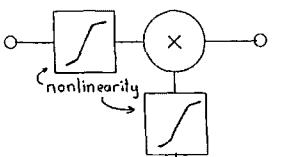
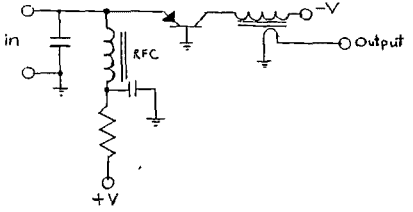


Figure D. Distortion Model



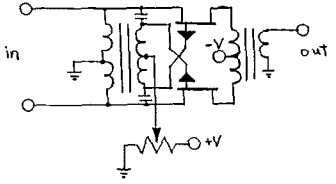


Figure E. Translmpedance Amplifiers

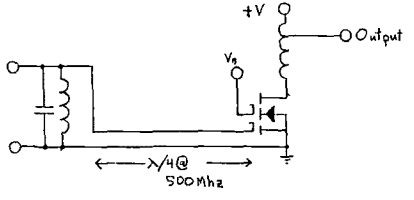


Figure G. Quarter wave matched Amplifier

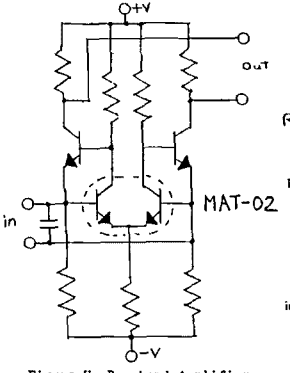


Figure H. Baseband Amplifier

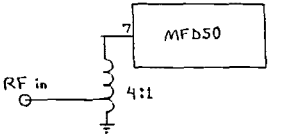


Figure F. Mixer with conversion gain

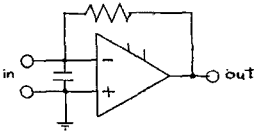


Figure I. Opamp Baseband Amplifier

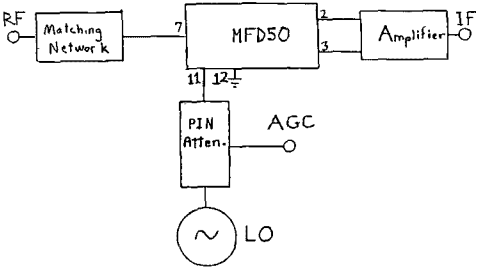


Figure J. Mixer with AGC

THE TACTICAL MINIATURE CRYSTAL OSCILLATOR (TMXO)

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The Tactical Miniature Crystal Oscillator (TMXO), Figure 1, is a high-performance frequency standard intended for use in a wide range of advanced military communications, navigation, and position-determining systems. Key advantages of the TMXO are:

Low Power	-	150 mW typical at 25°C 250 mW max. (-55 to +75°C)
Small Size	-	1.25 in. diameter x 1.55 in. height
Low Weight	-	1.75 oz. max.
Fast Warm-Up	-	4 minutes max. (from -55°C)
Frequency Accuracy	-	$\pm 3 \times 10^{-8}$/yr., all causes

Standard TMXO frequencies are 10 MHz and 10.23 MHz.

While the TMXO is an ovenized crystal oscillator, it uses a radically different mechanical design approach to achieve an order of magnitude reduction in power and size compared to conventional ovenized oscillators. In a conventional oscillator, most of the power required is used by the oven. *Reduction in power is achieved by more insulation* -- and therefore a bigger oscillator. This is fine for many applications, but it does not fit the tactical military environment.

The TMXO takes a different approach. First, the size of the electronics package is minimized by hybridization. The small size makes it easier to reduce the heat loss. A special ceramic package for the crystal resonator gives additional size reduction. Second, a high degree of thermal insulation is provided by an evacuated enclosure. The TMXO is the first production oscillator to use this technique.

Motivated by projected tactical requirements, the present TMXO was developed at Bendix Communications Division under sponsorship of the U.S. Army Electronic Research and Development Command (now the Laboratory Command) in a series of contracts which began in 1971 [1,2]. Concurrently, its unique ceramic flatpack crystal resonator was under development at General Electric, also under ERADCOM sponsorship [3]. In March, 1985, PTI obtained a commercial license from Bendix for the TMXO, and undertook to manufacture both it and its ceramic-packaged crystal. The first PTI-made TMXO was delivered less than fifteen months later. In this paper, we shall describe the TMXO as currently manufactured; then we shall briefly discuss the Improved TMXO (ITMXO), which is being developed under LABCOM sponsorship.

Applications

The TMXO is unequalled in providing a precise frequency reference requiring only a modest input power. This combination makes it well-suited for certain battery-powered applications — for example, a portable time transfer unit which can be synchronized from a reference clock (which might get its time reference from a GPS receiver), and which is used to set the clock of a remote system.

In a somewhat different application, the TMXO has been integrated into an existing cockpit environment, where size and weight are extremely important and where, in addition, the TMXO's high stability and fast warm-up are essential to the mission requirement.

In a third application, developed by LABCOM, the TMXO is used in conjunction with a rubidium secondary frequency standard. Its long-term stability is on the order of 1×10^{-11} per month, while the TMXO's is typically 1×10^{-10} per day, but the rubidium's power consumption is 10 to 20 watts. In one version, the rubidium is energized from time to time — perhaps once a week or once a month. The TMXO is then set to the rubidium frequency, and the rubidium is turned off until the next week or month. This allows even better long-term accuracy than the TMXO on its own provides, without the power penalty of the rubidium. In other versions, the rubidium standard is installed in a separate equipment and is used to re-set a number of TMXO's.

Mechanical and Thermal Design

The mechanical design of the TMXO sets it apart from other ovenized oscillators. Figure 2 shows the most significant aspects of the overall assembly. Except for an optional output buffer, all of the electronics is realized by a thick-film hybrid contained in a hermetically sealed ceramic and metal octagonal package, measuring about 1 inch from flat to flat. An SC-cut quartz crystal resonator in a smaller ceramic flatpack, also octagonal, is vacuum-soldered to the underside of the hybrid, and connected by welded gold ribbons.

This assembly is supported on 6 stiff Inconel wires which extend from the ceramic vacuum header and provide the input/output connections to the hybrid. The output buffer, if used, is located on the bottom, exterior face of this header. Lateral support of the crystal/hybrid assembly is provided by 4 polyimide bumpers which press against the inside wall of the outer enclosure.

The entire assembly is evacuated to eliminate convective heat transfer. Thermal radiation is made negligible by use of a cup-shaped thermal baffle or heat shield which prevents the outer case from "seeing" the hybrid/crystal assembly. As a further measure, the shield, and the inner wall of the outer case are electro-polished and gold-plated for low thermal emissivity. As a consequence of these measures, almost all heat loss is due to conduction along the Inconel wires and the polyimide bumpers. For the former, the thermal resistance is approximately 900 K/W; for the latter, an exact figure is not

easily calculated, due to small but highly significant dimensional uncertainties; however, the Inconel wires are the primary heat transfer path.

In order that gaseous heat conduction be negligible, pressure in the TMXO must remain below 10^{-3} to 10^{-4} Torr. This is assured by a number of processing steps. First, the hybrid and crystal packages are tested for hermeticity. Second, they are joined by reflow soldering in vacuum to elliminate trapped gas, which could, over time, leak into the TMXO cavity causing an increase in pressure. Third, all components are cleaned in an elaborate series of procedures. In the last stage before seal, the TMXO is outgassed in a vacuum-bake cycle. In this process, the TMXO is evacuated via its tubulation to a pressure of about 10^{-8} Torr while being maintained at a temperature of 150°C with a wrap-around heater and proportional controller.

In addition to these measures, the TMXO contains a non-evaporable, refirable getter located just above the vacuum header. The getter's purpose is to adsorb any gases liberated after seal. The getter is activated by an initial firing just prior to seal. During firing, the getter reaches temperatures up to 800°C. A heat shield between it and the header protects the latter, while the crystal and hybrid are protected by their heat shield. Hydrogen is liberated by the getter during activation, and pumping continues until this is completely removed. Finally, the OFHC tubulation is pinched off, completing the sealing cycle. All of the assembly processes are carried out under clean room conditions. In addition, a number of procedures are used to control materials and components used, and are just as important as the steps described.

Electrical Design

Principal electrical functions are the oscillator, the voltage regulator, the temperature controller and heater, and the optional output buffer. The circuit designs used are for the most part fairly conventional and will be only briefly described.

As noted earlier, all circuitry except the optional buffer is contained in the hybrid circuit module. The buffer, when used, is mounted on the outside face of the ceramic vacuum header.

Figure 3 shows the circuit of the oscillator and its voltage regulator. The regulator portion of *U1*, an *LM10*, and *Q9* make up the voltage regulator.

In describing the oscillator, the standard operating frequency of 10 MHz will be assumed. The oscillator sustaining circuit contains 2 stages of gain, *Q1* and *Q4*. The first stage, Q1, drives the pi-section filter consisting of C2, C7, C13, and L1. The crystal unit has a number of resonances, or modes. The filter must select the one which is wanted and reject the others. Thus it must pass the 3rd overtone C-mode frequency of 10 MHz while adequately suppressing the 3rd overtone B-mode which is about 9% higher in frequency. In

addition, it rejects fundamental and fifth overtone modes. At the 3rd overtone C-mode, the phase shift through the filter is 180°.

The second stage, Q4, drives the limiter, which consists of Schottky diodes D3 and D4. The limiter feeds back to the base of Q1 to close the loop. The crystal unit is in the emitter of Q1. Away from resonance, emitter degeneration reduces the first stage gain, so that the loop gain is less than unity. At 10 MHz the series combination of the crystal, blocking capacitor C12, varactor D1, and the load capacitor is resonant, thus determining the frequency of oscillation. The value of the load capacitor is set by grounding some or all of the "Frequency Adjust" points. Varactor D1 allows external frequency adjustment of at least $\pm 1 \times 10^{-7}$. Oscillator output is taken from Q8. The resistor R22 and blocking capacitor C12 prevent the occurrence of a d-c bias across the crystal unit. This is required because the resonant frequency of SC-cut crystals is sensitive to d-c bias, and because a d-c bias can cause frequency aging due to diffusion of electrode metal into the quartz body of the resonator.

A current-efficient bias network is used to keep the power dissipation low. D5 is a constant current diode which controls the bias current. D3 and D4 are forward biased, their current ratio being set by resistors R5, R19, and R9. The same current is used to set the operating points of oscillator circuit transistors Q1, Q8, and Q3, and transistor Q7 in the temperature control circuit.

The temperature controller schematic, shown in Figure 4, is a conventional proportional controller with added power limiting. Temperature is sensed by a glass bead thermistor in a Wheatstone bridge arrangement. Bridge arm resistance is 51K ohms. The unit is set to the crystal's turnover temperature by selecting the value of the thermistor and an external resistor. Q6 is the heater transistor. Gain is provided by the operational amplifier portion of U1. Heater current is sensed as the voltage across R16. The voltage across R21 is proportional to the heater voltage. The sum of these voltages is used to maintain constant warm-up power for a range of supply voltages by setting the base voltage of Q7. When the circuit is first energised, thermistor RT1 is very high in resistance, unbalancing the bridge and driving the current through the heater to a high value. Q7 is therefore turned on, limiting the heater current to approximately 1.5 amp and the rate of temperature change to about 2°/sec. As final oven temperature is approached, the thermistor resistance drops rapidly, which acts to reduce the heater current. The base voltage of Q7 drops, and it cuts off. The bridge comes almost to balance, regulating the heater current to the value required to maintain a stable operating temperature.

Hybrid Circuit Module

Figure 5 shows a completed hybrid circuit module prior to seal. The package is a custom design consisting of a multilayer ceramic base to which a Kovar sidewall is brazed. Connections to the hybrid are via "through" metallization of the ceramic base, terminating at exterior castellations. Pins are brazed to 6 of these. During final assembly, the Inconel support wires will be welded to the pins. The lower surface of the enclosure is metallized to permit subsequent attachment of the resonator package by solder reflow.

The octagonal shape of the hybrid permits linear parallel seam sealing using a stepped Kovar lid, while providing the maximum substrate area. To four side walls are brazed small turrets which hold the polyimide bumpers.

A beryllia heat spreader is bonded to the floor of the hybrid package. The heater transistor is eutectically bonded to a central, metallized pad. This transistor is used to heat the entire hybrid/crystal subassembly; the function of the heat spreader is to reduce lateral thermal gradients in the subassembly.

The hybrid substrate is epoxy-bonded to the top surface of the heat spreader. Both the heat spreader and the hybrid substrate are octagonal, but the latter has a central hole to accommodate the heater transistor. Substrate material is 94% alumina. Metallization is thick film gold; screened-on resistors use standard, ruthenium-based inks. Chip devices are epoxy-bonded to the substrate; connections are made by thermosonic gold ball bonding. Input/output connections are also wire bonded.

Crystal Resonator

The crystal unit is a 3rd overtone SC-cut quartz resonator in a special ceramic flatpack. Figure 6 shows the resonator in its package prior to sealing. The package consists of a ceramic frame and two ceramic covers, not shown. Mounts are brazed onto metallized pads, and support the plano-convex blank at four points. The lowest mechanical resonance is above 2 kHz. Gold electrodes are used. External connection is achieved via co-fired through metallization. Sealing surfaces are metallized and gold plated. Gold gaskets are used between covers and frame. The package is sealed by thermo-compression bonding.

The SC-cut is chosen for several reasons. First, in the vicinity of turnover, the frequency vs. temperature curve of the SC-cut is much flatter than that of AT- or BT-cut crystals, reducing the oven temperature control requirements. Second, very fast warm-up can be achieved due to the SC-cut's insensitivity to thermal gradients. Third, the stress compensation inherent in the SC-cut reduces acceleration sensitivity.

Low aging is obtained by a combination of measures. Electrodes are gold. Mounts are designed for minimum stress. Stringent cleaning procedures are

employed throughout resonator processing. An extensive vacuum bake is used prior to seal to outgas all resonator components. Figure 7 gives the aging results for one of the first TMXO resonators fabricated at FTI. The rate at day 30 is less than 1×10^{-10}/day.

Performance Data

The complete TMXO specification includes a long list of detailed requirements. We wish to discuss the most important of these.

Warm-Up Time. An important feature for many applications is fast warm-up. The TMXO has a specified warm-up time, from an ambient temperature of -55°C, of 4 minutes. Table 1 shows the measured warm-up time for 4 units.

Table 1

Warm-Up Time (from -55°C)

Unit No.	Time (Minutes)
10	1.9
15	3.0
18	2.4
24	2.4

Power Consumption. The maximum specified input power, after warm-up, is 250 milliwats, excluding power required for the optional output buffer. Figure 8 shows typical values measured over the operating temperature range. The buffer power requirement depends upon the output required, but is typically 50 mW or less.

Frequency vs. Temperature. The total frequency error budget includes half-a-dozen items, of which this parameter, and long-term aging, are the two largest components. A variation of $\pm 5 \times 10^{-9}$ is allowed over the operating temperature range. Figure 9 shows a variation of $+0.1, -2.0 \times 10^{-9}$, indicating that the oven temperature has been correctly set very nearly to the crystal's upper turnover point.

Aging. The maximum specified aging rate is 2×10^{-10} per day after 30 days continuous operation. Figure 10 shows frequency change for the first 21 days for TMXO No. 10. The aging rate for days 10 to 21 is already slightly better than the specified value at day 30.

Phase Noise. Figure 11 compares the measured SSB phase noise density, $\mathcal{L}(f)$, with the specification. It should be noted that measurements are exclusive of the output buffer. In some instances, degradation may occur when logic-level buffers are used.

Short-Term Stability. The short-term stability is shown in Figure 12, which plots the Allan variance, $\sigma_y(\tau)$, between 0.1 and 10 sec., and is well within specification.

Improvement Program

Notwithstanding the unequalled combination of low power, frequency accuracy, and size offered by the TMXO, further improvements are needed for a number of applications. Although not all of the following are needed in each instance, these areas have been targeted:

Phase Noise

Acceleration/Vibration Sensitivity

Nuclear Survivability

Manufacturing Cost

Work in these areas are being carried out under LABCOM sponsorship of an Improved TMXO (ITMXO). This 36 month program is still in its initial stage. Tasks concern circuit design and hybrid construction, crystal unit design and processing, and overall mechanical design.

Conclusion

The present TMXO and its unique ceramic flatpack crystal are the result of many years of development by the U.S. Army and its contractors. Previously, there has been no merchant source for the crystal, which is essential to the success of the TMXO. Now, for the first time, the TMXO and its resonator are being manufactured in a single facility and sold commercially.

Acknowledgment

We would like to thank Dr. J.R. Vig, Dr. R.L. Filler, V. Rosati, and S. Schodowski of the U.S. Army Electronic Technology and Devices Laboratory for encouragement and generous support. We would also like to thank the staff members of Bendix Communications and General Electric who provided assistance and the benefit of their experience, especially E. Laszlo, R. McGill, and D. Brown of Bendix, and T. Wagner and J. Keres of General Electric.

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[1] D. Brown, et al, "Manufacturing Methods and Technology for Tactical Miniature Crystal Oscillator," Proc. 38th Annual Symposium on Frequency Control, 1984, pp. 380-386.

[2] H.W. Jackson, "Update on the Tactical Miniature Crystal Oscillator Program," Proc. 36th Annual Symposium on Frequency Control, 1982, pp. 492-498.

[3] J.M. Frank, "Vacuum Processing System for Quartz Crystal Resonators," Proc. 35th Annual Symposium on Frequency Control, 1981, pp. 40-48.

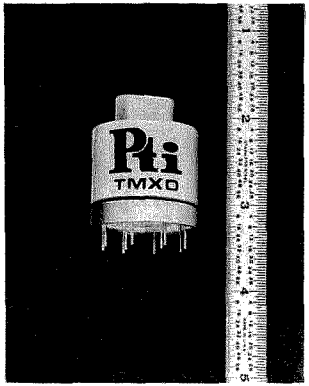

FIGURE 1. The TMXO

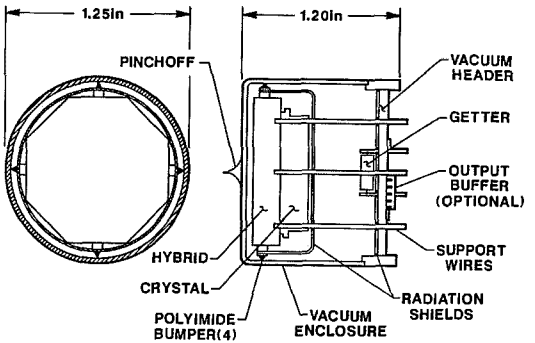

Figure 2. Simplified TMXO Construction

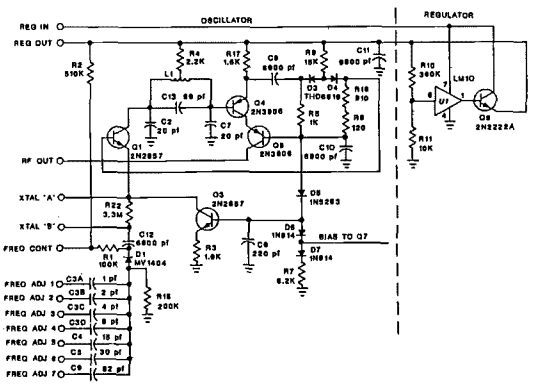

FIGURE 3. Oscillator and Voltage Regulator Circuit Diagram

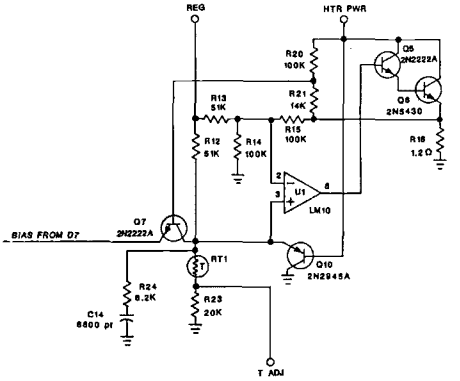

FIGURE 4. Temperature Controller Circuit Diagram

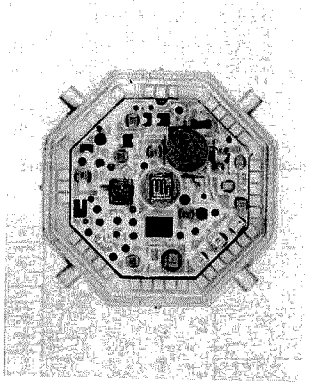

FIGURE 5. Hybrid Circuit Module Prior to Sealing

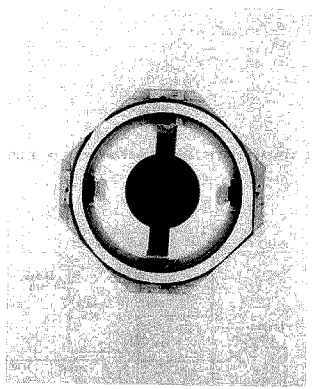

FIGURE 6. SC-Cut Resonator Mounted in its Ceramic Flatpack. Not shown are ceramic top and bottom covers.

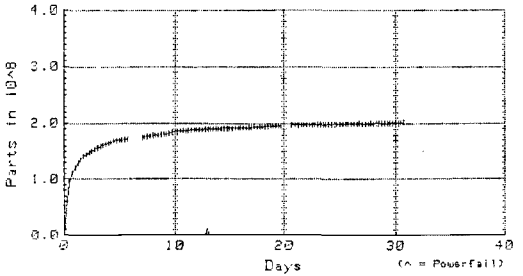

FIGURE 7. Frequency Aging Curve of a TMXO Crystal Unit. The unit is aged in a test oscillator prior to use.

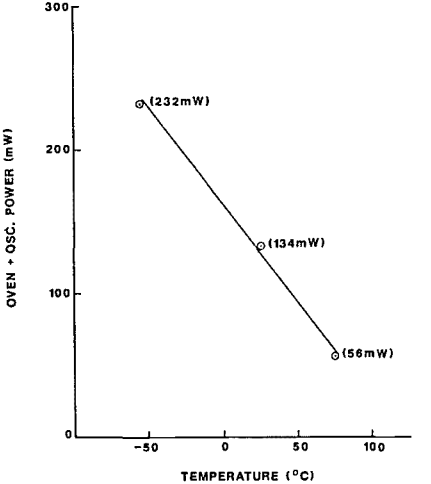

FIGURE 8. Input Power va. Temperature, TMXO No. 10

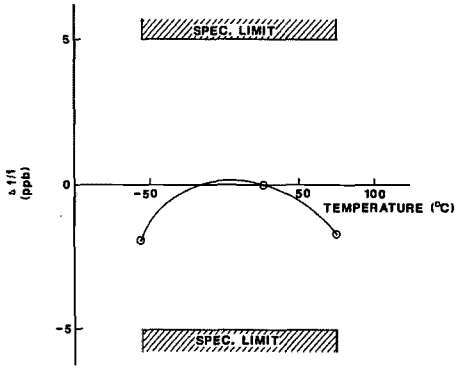

FIGURE 9. Frequency vs. Temperature, TMXO No. 10

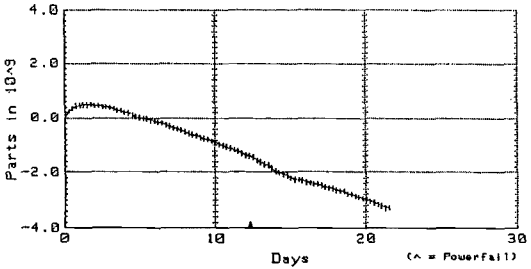

FIGURE 10. Frequency Aging Curve, TMXO No. 10

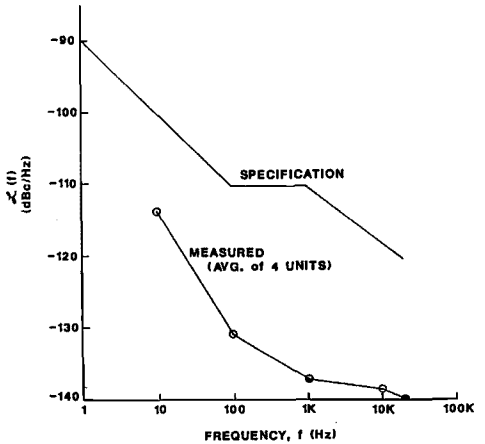

FIGURE 11. SSB Phase Noise Density (without output buffer)

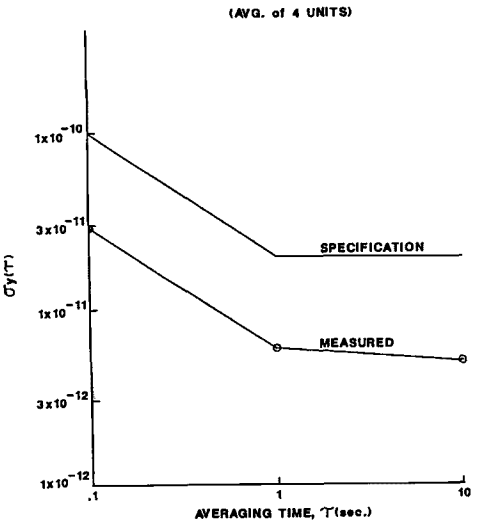

FIGURE 12. Allan Variance

DESIGN CONSIDERATIONS FOR SAWR OSCILLATORS

How to Specify a SAW Resonator From a Manufacturer

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INTRODUCTION

There are three different stages in designing an oscillator circuit using a SAW device: choosing the correct SAW device for the application; specifing the design parameters for the SAW device; and incorporating the SAW device into the oscillator design.

The two types of SAW devices used in oscillator designs are SAW delay lines and SAW resonators. An oscillator circuit using a SAW delay line is capable of being tuned over a frequency range of up to 1 MHz. Larger tuning ranges degrade the tuning linearity, phase noise and temperature stability of the device.[1] An oscillator circuit using a SAW resonator (SAWR) is used for fixed frequency applications. Its tuning range is related to the Q of the resonator. Increasing the Q narrows the tuning range. SAWR's typically have a Q between 5000 and 10,000.[2]

This paper focuses on the specifications for a SAWR device and the design parameters for incorporating the SAWR into an oscillator circuit. Two different oscillator designs are discribed. Their advantages and disadvantages are discussed along with the problems encountered.

DESIGN SPECIFICATIONS FOR SAW RESONATOR

To purchase a SAWR from a manufacturer certain specifications must be considered. Some of these parameters are determined by the manufacturer, others must be specified by you, the engineer. Specifications to consider include manufacture's tolerance, temperature drift, turnover temperature, aging, center frequency, phase shift, insertion loss and spurious rejection. An explanation of these characteristics is given along with some typical figures. It is important to understand these conditions because some of them affect the circuit design.

CENTER FREQUENCY: Center frequency is the resonant frequency of the SAW device. The useful frequency range of a SAWR is from 250 Mhz to 1.2 Ghz. There are SAWR's as low as 50 Mhz, but the physical size of the package is large and therefore expensive.[3] The upper end of the SAWR range is limited by the photolithographic processes. Greater resolution is required for higher frequencies.[4]

Some circuit configurations will not operate very close to the SAWR's center frequency. For this reason, it may be necessary to specify the center frequency at some offset from the operating frequency. SAW oscillator design #1 on page 11 is an example of this type of circuit.

MANUFACTURER'S TOLERANCE: The manufacturer's tolerance specifies the maximum amount of deviation from the center frequency allowed by the manufacturer. The larger the manufacturer's tolerance, the better the yield of acceptable devices. A better yield generally means a lower price per component. A typical manufacturer's tolerance for a SAWR device is 200 ppm (parts per million).

TEMPERATURE DRIFT: Temperature drift is the total amount of frequency deviation from the center frequency over a specified temperature range. The amount of drift is determined by the temperature coefficient of delay and the turnover temperature. Both are related to the type of substrate used to make the device and the type of cut performed on the substrate.

Temperature Coefficient of Delay: Two different substrates are commonly used in SAW devices: quartz and lithium niobate. The temperature coefficient of delay for ST-X quartz is less than 3 ppm/deg C at room temperature. YZ-lithium niobate has a temperature coefficient of delay of 85 ppm/deg C. Since ST-X quartz has a smaller temperature coefficient of delay, it is more stable over temperature. Using lithium niobate as a substrate may require an oven for temperature stability.[5]

Turnover Temperature: The turnover temperature is that temperature where the frequency deviation is minimal. A graph of frequency deviation verses temperature with a turnover temperature at +25 deg C (room temperature) is shown in figure 1. The shape of the response is parabolic with the turnover temperature at the vertex. Notice that the frequency deviation due to temperature is negative.[8]

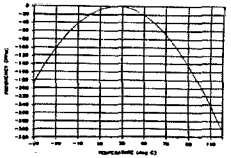

Fig. 1 Frequency vs. Temperature

For this discussion the temperature range of interest will be from 0 deg C to +70 deg C.

The turnover point of the parabola can be positioned anywhere between -25 deg C and +90 deg C.[7] The placement of this turnover point has a large affect on the amount of frequency deviation due to temperature. For example, if the turnover temperature is at +80 deg C, then the frequency deviation between 0 deg C and +70deg C is nearly linear as shown in figure 2. As temperature decreases, frequency decreases.

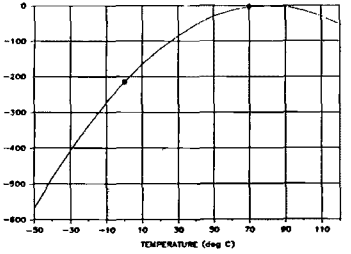

Fig. 2: Turnover Temp at +80 deg C

The amount of frequency deviation

in parts per million due to a specific temperature is calculated using equation 1 shown below.

$$F\ (ppm) = \frac{(T-To)^2}{(Tc)^2} \qquad \text{<Equation 1>}$$

where F = Frequency deviation due to temperature in parts per million,
To = Turnover temperature in deg C,
Tc = Temperature coefficient in deg C^2 per parts per million [8],
T = Temperature of interest in deg C.[9]

For the situation shown in figure 2, the maximum amount of frequency deviation is

$$F\ (ppm) = \frac{(70 - 0)^2}{(5.45)^2}$$

$$= 165\ ppm.$$

Notice that the difference between the two extreme frequencies is substituted in for the quantity "T-To". This substitution is necessary because the turnover temperature is outside the desired temperature range.

The advantage in this example is that the frequency deviation is nearly linear with changes in temperature. This deviation is easily overcome by using a temperature compensating capacitor.

Now look at the example shown in figure 3. The turnover temperature is at +35 deg C which is right in the middle of the desired temperature range. As temperature decreases from the turnover temperature, frequency decreases. But as temperature increases from the turnover temperature, frequency again decreases.

In this example, either extreme temperature can be substituted into equation 1 for "T" since the turnover temperature is exactly in the center of the frequency range. The temperature deviation is

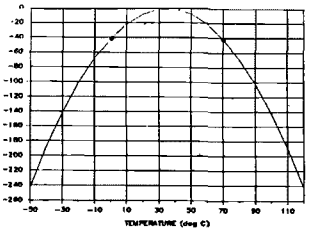

Fig 3: Turnover Temp at +35 deg C

$$F\ (ppm) = \frac{(70 - 35)^2}{(5.45)^2}$$

$$= 41\ ppm.$$

The advantage in this example is a low frequency deviation which can be handled within the pull range of the circuit.

AGING: Aging is the amount of frequency deviation from the desired frequency over a long period of time (years). This type of frequency change is a logarithmic function of time with most of the drift occurring in the first year.[10] For this reason, many manufacturers will only specify aging for the first year. A typical value for aging is 10 ppm/year maximum for the first year.

PHASE SHIFT: The amount of delay in degrees at the output

of the device as referenced to some point (usually the input of the device) is the phase shift for the device. SAW resonators are built with either a 0 degrees phase shift or a 180 degrees phase shift (theoretically).

Phase shift for a SAWR can be specified two different ways. It can be specified at the SAW's resonant frequency or at some other frequency. The latter case is used when the circuit configuration requires a certain amount of phase shift at a particular frequency to operate. Then the phase is specified at that frequency instead of at the center frequency of the SAWR.

INSERTION LOSS: Insertion loss is the ratio of input power to output power, normally expressed in dB [11] and also related to Q.[12] If the insertion loss is high, the Q will be low and the device can be pulled farther from its resonant frequency. For a lower insertion loss, the Q will be higher and the device's pull range will be tighter. Typical insertion losses for SAW resonators range from 8 dB to 14 dB depending on the center frequency.

SPURIOUS REJECTION: Spurious rejection is a measurement of how far unwanted outputs in the frequency domain are suppressed.[13] Manufacturers usually avertise a minimum spurious rejection of 7 dB to 10 dB. Typical values are around 12 dB to 16 dB depending on the insertion loss and Q of the device.[14]

SAWR OSCILLATOR DESIGN CONSIDERATIONS

While designing a SAW resonator (SAWR) oscillator, several considerations should be kept in mind. The most important of these considerations is the way a SAWR is matched into a circuit. Oscillator stability, tuning range, and active device selection are all affected by the input and output matching networks.[15]

MATCHING IMPEDANCE: The bulk of the design effort is focused on the input and output matching elements. The matching elements must place the SAWR in the proper impedance environment, provide the additional phase shift necessary for oscillation, and tune the oscillator to the correct frequency.[16]

If the input and output matching networks present a low impedance to the SAWR device, the loaded Q of the SAWR would be relatively high, the insertion loss would be high and the tuning range for the oscillator circuit would be quite narrow. The high insertion loss requires an active device with a high amount of gain to sustain oscillation. The high loaded Q causes the SAWR device to dominate control of the circuit's frequency whereas other oscillator components have little affect. Because of the SAWR's tight control, the best possible phase noise performance is achieved.[17]

If the matching networks present a high impedance to the SAWR device, the opposite happens. The loaded Q and the insertion loss would be relatively low, and the tuning range

would be wider. A lower insertion loss does not require an active device with a high amount of gain to sustain oscillation. Because of a lower loaded Q, variations in the other oscillator components have a noticable affect on the operating frequency. Phase noise performance degrades slightly.[18]

TUNING ADJUSTMENT: Fine tuning of the SAWR oscillator should be limited to one adjustable component.[19]

MAXIMUM POWER: A good rule of thumb is to limit the power dissipated in the SAWR device to 20 milliwatts. Larger amounts of power cause strong vibrations to occur inside the SAWR that will eventually tear the aluminum transducers from the substrate. Once this separation occurs, the device is ruined.[20]

DC CURRENT: For best reliability, DC (direct current) should be kept off the SAWR device. The SAWR will operate with DC running through it but reliability degrades.[21]

PULL RANGE: The pull or tuning range is determined by the SAWR's characteristics and by the circuit's requirements. Depending on how wide a pull range is needed determines whether matching networks present a high or low impedance to the SAWR.

The oscillator circuit handles the pull range in two different ways. A course adjustment compensates for the manufacturer's tolerance by pulling the SAWR onto the desired frequency when the circuit is first built. A fine adjustment compensates for frequency drift due to temperature changes and aging over time.

If the frequency drift due to temperature is 100 ppm and the overall aging of the SAWR device is 30 ppm, then the minimum amount of fine tuning needed is 130 ppm. If the oscillator is designed for a pull range (fine tune) of 160 ppm to 200 ppm, then the circuit is guaranteed to satisfy the pull range requirement.

PHASE NOISE: Phase noise performance degrades as the deviation from the SAWR's resonant frequency increases. Figure 4 is a plot of phase noise measured 10 Khz away from the operating (carrier) frequency versus the distance between the operating frequency and the SAWR's resonate frequency of a 674 Mhz oscillator. The data for this plot is shown in Table 1.

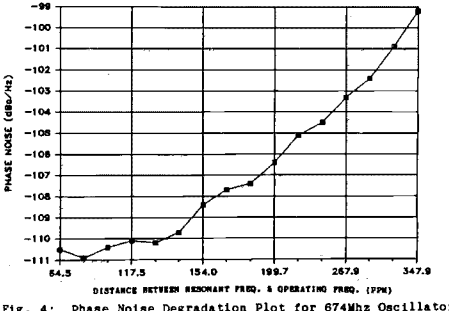

Fig. 4: Phase Noise Degradation Plot for 674Mhz Oscillator

The worst case phase noise situation occurs when the device is at one of the extreme ends of the manufacturer's tolerance. To determine this point (in ppm), add together the manufacturer's tolerance, temperature drift, and aging. If the manufacturer's tolerance is 200 ppm, temperature drift 100 ppm, and overall aging 30 ppm, the worst case phase noise would occur 330 ppm away from the SAWR's resonate frequency.

AFC VOLTAGE (volts)	DELTA FREQ. (Khz)	FREQ FROM RESONATOR FREQ. (PPM)	PHASE NOISE (dBc/Hz)
0.0	12.0	64.9	-110.5
1.0	11.8	86.8	-110.9
2.0	9.1	104.3	-110.4
3.0	9.4	117.8	-110.1
4.0	7.7	130.3	-110.2
5.0	8.3	141.7	-109.7
6.0	8.9	154.0	-108.4
7.0	4.9	167.2	-107.7
8.0	12.1	181.7	-107.4
9.0	14.4	199.7	-106.4
10.0	19.1	221.4	-105.1
11.0	14.3	242.8	-104.3
12.0	17.2	267.9	-103.3
13.0	18.5	293.5	-102.6
14.0	18.2	320.9	-100.9
15.0	18.0	347.9	-99.2

Table 1: Measured Data Taken on the 674Mhz Oscillator

SAWR OSCILLATOR DESIGNS

Two different circuit configurations are discussed along with their advantages and disadvantages. The problems encountered during the design of the second circuit are also mentioned.

SAWR OSCILLATOR DESIGN #1

The circuit shown in figure 5 is designed using a 674 MHz SAW Resonator.

ADVANTAGES:

1. This design contains no tuning coils which could cause microphonics.

2. The number of parts in this circuit is kept to a minimum. Fewer parts means better reliability.

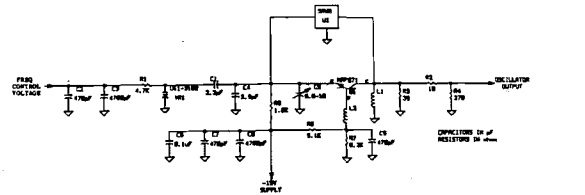

Fig. 5: Ckt Configuration for Design #1

DISADVANTAGES:

1. DC is allowed to run through the SAWR. This condition reduces the reliability of the device.

2. The circuit only oscillates on one side of the SAWR's resonant frequency.

3. If the oscillator is pulled too close to the SAWR's resonant frequency, the circuit experiences a phase reversal and "jumps" to another frequency.

4. The phase noise performance of this circuit is not as good as a circuit that can pull its operating frequency through the SAWR's resonant frequency.

In order to prevent the oscillator from jumping to another frequency, a safety region between the SAWR's resonant frequency

and the frequency determined by the tuning voltage is established. Through experimentation, a safety region of 100ppm was found to be satisfactory.

SAWR OSCILLATOR DESIGN #2

A different oscillator configuration is shown in figure 6. Tbis design uses an 848 MHz SAW resonator.

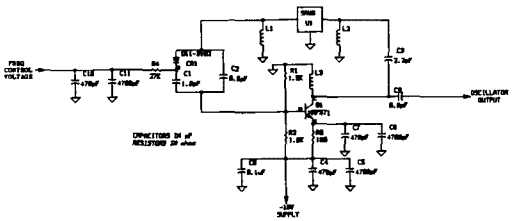

Fig. 6: Ckt Configuration for Design #2

CIRCUIT DESCRIPTION: The biasing network, resistors R1, R2 and R3, set up the necessary conditions for the MRF571 transistor. Note the use of a negative supply. This transistor is a high gain, low noise device with a transitional frequency of 8.0 Ghz at 50 mA.[22] Capacitors C7 and C8 provide an AC ground to the emitter of the transistor.

L3 is a RF choke which prevents the RF signal from shunting to ground.

The frequency control voltage is placed between capacitor C1 and varactor diode VR1. VR1 is a U11-3102 varactor diode; a part specially made for Watklns-Johnson Company. Its capacitance changes as the voltage is varied.

The input matching network consists of capacitors C1 and C2, varactor diode VR1, and lnductor L1. The output matching network consists of capacitor C3 and inductor L2.

The course tune adjustment is done by varlng inductors L1 and L2. This adjustment is very critical because it largely affects the circuit's pull range and amplitude response.

Tbe fine tune adjustment is done by adjusting tbe frequency control voltage. The varactor diode VR1 together with capacitors C1 and C2 changes the amount of capacitance seen by the SAWR in the input matching network. This change pulls tbe SAWR through the circuit's tuning range.

PHASE NOISE: *The single side-band phase noise performance* of the 848 Mhz SAWR oscillator (free-running) is shown in figure 7.

Notice that the offset from the carrier in figure 7 is only shown up to 1.7 Khz. Beyond this offset, the oscillator's phase noise performance approached the limit of the test equipment.

The phase noise performance of the 848 Mhz oscillator at an offset of 10 Khz is about -118 dBc/Hz.[23]

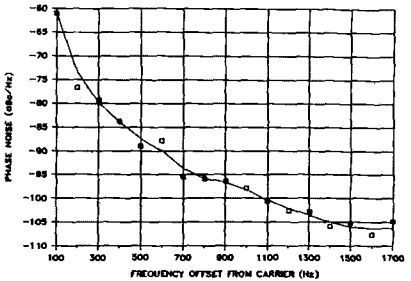

Fig. 7: Frequency vs Phase Noise Plot for an 848Mhz Oscillator

ADVANTAGES:

1. The operating frequency can be pulled through the SAWR's resonant frequency. This feature allows the best possible phase noise response to occur.

2. There is no DC running through the SAWR device.

3. Stray capacitance is tuned out by adjusting inductors L1 and L2.

4. This circuit is very reproducible.

DISADVANTAGES:

1. More components are needed to build this design. The greater number of components reduces the circuit's reliability.

2. The values of the matching network's components are very critical. Small variations in these values have a great affect on the oscillator's performance.

DETERMINING THE MATCHING NETWORK VALUES: The actual values for the matching networks depend on the circuit lay-out. After the circuit is designed and laid out on a PC board, replace matching capacitors C1, C2 and C3 with adjustable capacitors set at the designed values. Once the circuit's performance is satisfactory, replace the adjustable capacitors one at a time with fixed capacitors; rechecklng the circuit's performance after each substitution.

Coupling capacitor C9 may also have to be adjustable (initially) since it influences the output matching network.

The matching inductors are refined in the same manner.

If the circuit does not oscillate, use a network analyzer in the feedback path to determine the amount of gain and phase in the loop. Be sure to zero out the cable effects before connecting the network analyzer to the oscillator circuit. Adjust the matching components until the network analyzer displays a 0 degrees phase shift and a magnitude greater than 0 dB which represents gain in the loop.

Disconnect the network analyzer and close the feedback loop in the oscillator circuit. Minor adjustments on the matching component values may be necessary to cause the circuit to oscillate.

Using the network analyzer prevents a lot of guess work by allowing the engineer to see the effects on amplitude and phase as a component's value increases or decreases.

PROBLEMS ENCOUNTERED: A few problems occurred during the testing of several oscillator circuits. They are mentioned here along with their solutions.

Squegging: Squegging is the oscillator's operating frequency modulated by a low frequency signal. The result is a mass of spurious signals. This squegging problem is solved by bypassing the transistor in such a way that the gain at low frequencies is reduced.

Matching: As mentioned earlier, the values of the matching components are very critical. If the circuit is mismatched, several different problems can occur. These problems are mentioned in the following paragraphs.

Jumping: The phase response around the center frequency of a SAWR is not always linear. The steeper the slope of the phase, the greater the frequency change is per volt. As the voltage changes, the SAWR's phase may pull through one of these nonlinear points and cause a greater frequency change to occur. This frequency change appears as a "jump" in frequency. The size of the jump depends on how much of the phase response has the steeper slope.

The jumping may not always occur at the same operating frequency or control voltage. For example, take a 674 Mhz oscillator with a SAWR resonate frequency at 674.0281 Mhz. As the frequency control voltage is decreased, the operating frequency jumps from 674.0634 Mhz to 633.6751 Mhz (a difference of roughly 40 Mhz). Upon increasing the control voltage, the operating frequency doesn't jump until it reaches 657.297 Mhz. Then it jumps to 674.205 Mhz (a difference of about 17 Mhz).

The matching networks can prevent jumping from occurring by presenting a high impedance to the SAWR device. Figure 8 shows a plot of frequency versus voltage of the same 674 Mhz oscillator (mentioned earlier) after its matching networks were changed to present the SAWR with a higher impedance. The data for this plot is shown in table 1 (page 11).

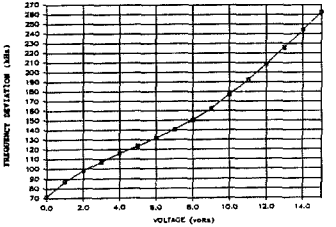

Fig. 8: Frequency Deviation vs AFC Voltage Plot for 674Mhz Oscillator

Notice that the frequency change from 13 volts to 14 volts

is larger than the frequency change from 6 volts to 7 volts. If this frequency change (between 13 volts and 14 volts) were even greater, it could appear as a jump in the frequency range.

Amplitude Variations: Sometimes the amplitude of the operating frequency varies over the tuning range of the circuit. For example, a 872 Mhz oscillator has a pull range of 89 Khz and an amplitude variation of 21.6 dB. After adjusting the values of the matching elements, the oscillator has a pull range of 313 Khz and an amplitude variation of 11.2 dB. Further adjustments on the matching components produce a tuning range of 122 Khz and an amplitude variation of 0.9 dB.

Frequency Range Variations: As seen from the previous example, the matching components have an effect on the tuning range of the oscillator circuit as well as the amplitude response. If the matching networks present a high impedance to the SAWR, the tuning range of the oscillator circuit will increase.

Loop-back in Tuning Range: Normally, as the control voltage increases, the frequency increases. In a loop-back situation, the frequency begins increasing as the control voltage increases but then it "loops-back" and starts to decrease. This situation is extremely undesirable because it can causes a phase-locked loop to be driven to limits in one direction, and the oscillator will never lock onto the correct frequency.

The solution to these problems is to adjust the matching components. The matching coils, L1 and L2, are the easiest to adjust.

CONCLUSION

The type of SAW device used in an oscillator design depends on the requirements of the application. For fixed frequency applications, a SAW resonator is recommended. Once the device is selected, careful consideration is given to its characteristics. Center frequency and turnover temperature are two of these characteristics that affect the way the oscillator circuit is designed.

The most difficult part of designing any SAWR oscillator is finding the appropriate matching component values. Once these values are determined, the oscillator demonstrates an excellent phase noise response, an adequate tuning range, and a minimum amount of amplitude variation.

ENDNOTES

[1] Handbook of Acoustic Signal Processing (Andersen Laboratories, 1984) Vol. IV, pp.12-13.

[2] C.K. Campbell, Surface Acoustic Wave Devices and Their Signal Processing Applications (The George Washington University, Continuing Engineering Education, 1985), p. 9.22.

[3] Robert J. Kansy, Introducing the Quartz Surface Acoustic Wave Resonator (Application Note: No. 1, RF Monolithics, Inc.), p. 1.

[4] Handbook of Acoustic Signal Processing, p. 8.

[5] Campbell, pp. 1.6-1.8.

[6] Handbook of Acoustic Signal Processing, p. 9.

[7] Resonators & Oscillators (Brochure, Crystal Technology).

[8] The temperature coefficient, Tc, varies from manufacturer to manufacturer. For discussion purposes only, 5.45 will be used as the temperature coefficient.

[9] Equation obtained through a telephone conversation with Sawtek Incorporated.

[10] Data sheet for 180 deg quartz SAW resonator (RF Monollthics, Inc., 1984).

[11] Handbook of Acoustic Signal Processing, p. 16.

[12] Q is defined as the center frequency divided by the bandwidth (usually the 3 dB bandwidth).

[13] Handbook of Acoustic Signal Processing, p. 10.

[14] Based on data sheets obtained from Sawtek, Incorp.

[15] Frank Perkins, Jr., Designing UHF SAW Resonator Oscillator (Application Note: No. 4, RF Monolitbics, Inc., 1983), p. 1.

[16] Perkins, pp. 1-2.

[17] Perkins, p. 3.

[18] Perkins, p. 3.

[19] Perkins, p. 3.

[20] Information obtained through a classroom discussion with Dr. C. K. Campbell at the George Washington University.

[21] 1GHz SAW Resonator -Application Note (Handwritten, Stantei Corp., 22 Mar 85).

[22] Motorola RF Device Data (Motorola, Inc., 1983), pp. 6-149 to 6-161.

[23] Extrapolated using data taken from a 1 KHz offset.

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1. Campbell, C. K., Ph.D., D.Sc., F.R.S.C., Surface Acoustic Wave Devices and Their Signal Processing Applications, Washington, DC, The George Washington University School of Engineering and Applied Science, 1985.

2. Handbook of Acoustic Signal Processing, Andersen Labs, 1984, Vol. IV.

3. Kansy, Robert J., Introducing the Quartz Surface Acoustic Wave Resonator (Application Note: No. 1), RFMonolithics, Inc., 1983.

4. Motorola RF Device Data, Motorola, Inc., 1983, pp. 6-149 to 6-161.

5. Perkins, Frank, Jr., Designing UHF SAW Resonator Oscillators (Application Note: No. 4), RFMonolithics, Inc., 1983.

6. Resonators & Oscillators, Crystal Technology.

7. RFM data sheet for 180 degrees Quartz SAW Resonator, RFMonolithics, Inc., 1983.

8. 1 Ghz SAW Resonator -Application Note (Handwritten), STANTEL Corp., 22 Mar 1985.

Monolithic RF Amplifiers for Hybrid Applications

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Monolithic Gallium Arsenide ICs for RF systems have held promise for many years. Yet there has only been a modest list of product offerings of basic functions with relatively high device costs. Using these basic components has implied even higher costs associated with system insertion due to the need for external components and circuitry. This was particularly true of early transistor amplifier products that required extensive bias circuitry or decoupling components to operate. The real promise of integrated circuitry lies in reducing the number of components to minimize assembly costs and unit-to-unit variations while improving reliability and overall system performance.

GaAs Technology has now reached the level of maturity where more complex functions can be integrated onto single analog or digital ICs. With recent advances in the sophistication of technology in materials, processing, design and test, a growing number of firms are capable of designing and building GaAs ICs. Foundry, design, and test services are now widely offered. Yet standard product offerings, addressing high volume "generic" applications, have been slow to emerge. Harris Microwave Semioonduotor has introduced its first two products in a line of GaAs RF ICs for receiver/transmitter and signal processing applications. These are broadband amplifiers chips covering 500 MHz to 5.0 GHz and providing general purpose gain. The HMR-10503 is a fully integrated amplifier requiring no external circuitry other than bond wires to connect the RF input , RF output, +Vdd and DC/Signal ground. The companion HMR-10502 is identical except

that the bias supply decoupling capacitors are not included on-chip. These parts offer the RF systems designer/integrator a new option in system architecture and implementation at UHF frequencies and above. By cascading or individually distributing these ICs throughout the system, there is now available compact and affordable amplification to maximise system performance. System Cost/Performance targets can be more easily met though the use of these complete IC gain blocks, with low $/dB of gain, and the relaxed performance specifications on other system functions that these amplifier ICs allow.

The Product

Fundamental in the offering of an effective GaAs IC is the basic quality of the fabrication process. Harris Microwave Semiconductor uses Its DIGI-1 Process Technology. Harris has been manufacturing GaAs (digital) ICs with this process for over three years. DIGI-1 is a very high performance process technology offering the high gain required for analog circuits and the high repeatibility required for digital circuits. Repeatibility is the secret for both the low cost and consistency achieved in these RF ICs. This process uses a one micron gate length and depletion mode technology with -2 Volt pinchoff. A summary of the basic process electrical parameters is contained in Table 1.

Electrical parameters:	
Shallow implant (n)	1150 Ω/□
Deep implant (n+)	110 Ω/□
Ohmic contact	1 Ω/□
Gate metal (air-bridge)	0.02 Ω/□
Specifications:	
Transistor (L_g = 1μ)	
I_{max} (V_{DS} = 3 V, V_{GS} = 0 V)	200 mA/mm
V_P (V_{DS} = 3 volts I_{DS} = 1% I_{DSS})	-1.9 V
g_{mPK} (V_{DS} = 3 V, V_{GS} = -0.5 V)	150 mS mm
BV_{GSO} (I_{GS} = 100 μA)	10 V
BV_{GSO} (I_{GS} = 100 μA)	10 V
Second metal (air-bridge)	0.02 Ω/□
Diodes	
C Junction	1.6 pF/mm²

TABLE 1. DIGI-1 process technology

The circuitry is designed to exploit the performance characteristics of the process technology to produce consistently achieved performance for the system application. The schematic of the RMR-10503 is shown in Figure 1. The heart of the IC is a 1 X 600 micron GaAs FET "cell". Two of these cells are isolated from each other by Integral MIM capacitors. The source terminals of the RF Transistors and self-biasing implanted resistors, in series with the sources, are decoupled by additional MIM capacitors of approximately 25 pF each. Drain bias on the active RF devices is provided by additional FETs operating as current sources. Each of the current sources Is shunted by an implanted resistor to minimise the bias point sensitivity to process and temperature variations. Consistent broadband RF performance is the result of a series resistor-inductor which is in shunt feedback to the RF transistor. The two stages have been designed as a system to minimise input/output VSWR, maximise gain, and maintain a controlled noise figure.

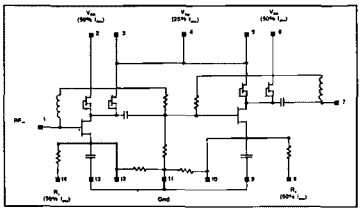


Figure 1. HMR-10503 Schematic

As seen in the schematic, two bias point options are readily available to the user. In addition to the standard 25% Idss, either or both of the two stages can be biased to 50% of the RF transistor Idss with additional wirebonds. Bonding diagrams for two of the four wiring options are shown in Figure 2.

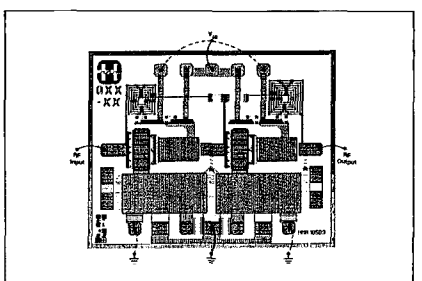


Figure 2. Wire bond diagram for HMR-10503. Solid lines are 25% I_{dss} connections (V_{DD} = +8 V). Dashed lines are additional connections for 50% I_{dss} (V_{DD} = +10 V).

Wide Band Performance

Performance of the typical HMR-10502/HMR-10503 is shown in figure 3. Frequency of operation for the ICs is 500 MHz to 5.0 GHz with extended frequency operation possible at reduced performance level. Power supply limits are from +6.0 Volts to +15.0 Volts although typical applications call for +8.0 Volts or +12.0 Volts for Vdd at 50 mA.

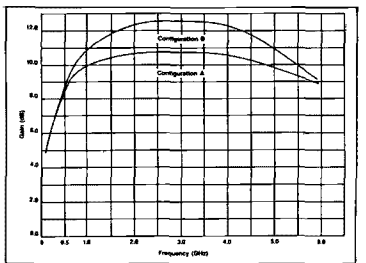


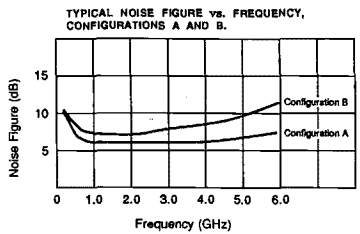
Figure 3. Gain (S21) vs. frequency, configurations A and B. Bias for Conf. A: D_{dd} = 8.0 V, I_{dd} = 50 mA; Bias for Conf. B: V_{dd} = 10.0 V, I_{dd} = 100 mA.

A minimum of 10 dB gain is readily achieved at 8 Volts and 25% Idss with 12 dB typical, (configuration A). Gain flatness is +/- 0.75 dB for the HMR-10502 over the complete 0.5 to 5.0 GHZ frequency range with two 100 pF source decoupling capacitors, one on each source decoupling port. The HMR-10503 has the same +/- 0.75 db gain flatness over a smaller 1.0 to 5.0 GHs bandwidth without optional source decoupling capacitors. Optional

additional source decoupling capacitors of greater than 50 pF result in full band flatness for the HMR-10503. The VSWR of the input and output is always better than 2.0:1 and typically better than 1.7:1 across the specified frequency band when assembled using nomlnal wirebond lengths of 15 to 25 mils.

Noise figure for either unit at 25% Idss is typically 6 db, 7.0 db aaximum. When biased at 10 Volts and 50% Idss (configuration B), the noise figure is less than 10 dB and typically less than 8.0 dB. Figure 4 shows the typical noise figure at both bias conditions versus frequency.

FIGURE 4



The third order intercept point (IP3) versus frequency for both bias options is shown in Figure 5. The minimum of +18 dBm is achieved at the high end of the frequency band at 25% Idss. Typical third order intercept point at 50% Idss is greater than +20 dBm.

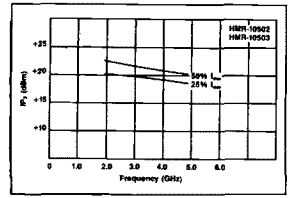
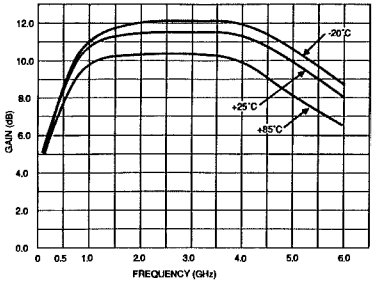


Figure 5. Third order intercept point vs. frequency.

Idd variation at either bias option is consistent unit to unit as well. Typical supply current is 50 mA plus or minus 10 mA at the low bias point for the total unit. DC supply voltage is user defined froa 8 to 15 Volts depending on the specific power supply voltage availability, specific output power desired, and temperature range requlrements. The baslo performance characteristics of gain, VSWR and isolation are relatively lndependant of power supply voltage. Gain variation of gain of typically 0.03 dB/ degree C for this two stage amplifler. Flatness is maintalned across wide temperature ranges. Figure 6 shows the typical gain performance at -20, +25 and +85 degrees C.

FIGURE 6. GAIN (S21) VS. FREQUENCY AT -20°, +25°C AND +85°C, CONFIGURATION A. Bias for CONF. A : Vdd = 8.0V, Idd = 50mA.



Testing and Quality Assurance

To insure consistent and reliable performance, the HMR-10502 and HMR-10503 are tested and qualified under procedures similar to standard FETs produced by Harris Microwave Semiconductor. Samples from each lot are strenuously tested to qualify the lot for mechanical integrity, electrical performance, and reliability. The flow of the product assurance and lot qualification process shown in figure 7 results in product that exceeds the Element Evaluation requirements of MIL-STD-883C, Method 5008 for Class B devices.

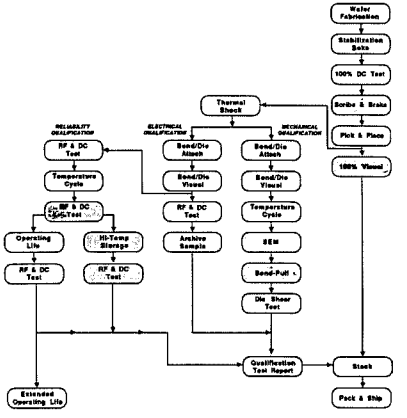


Figure 7. Product Assurance Flow

The Applications

With the combination of low cost , repeatibility, reliability and application flexibility, the HMR-10502 and HMR-10503 can be effectively inserted into many system designs. One of the most obvious applications that can use the basic utility gain characteristics of the ICs is in receiver/transmitter modules. Figure 8 is a block diagram of a typical single channel dual conversion downconverter operating in the 500 MHz to 5.0 GHz frequency range configured with distributed gain in the form of HMR-10503s to maintain noise figure and dynamic range. A significant advantage of using distributed gain is that it

results in reduced specification requirements, and therefore cost, for the various subsystem elements such as mixers and filters.

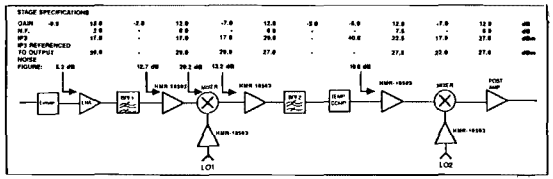

STAGE SPECIFICATIONS
GAIN -0.5 12.0 -2.0 13.0 -7.0 13.0 -3.0 -4.0 12.0 -7.0 12.0 dB
N.F. 2.5 . 4.0 . 4.5 . . 7.5 . 4.5 dB
IP3 17.5 . 17.0 17.5 29.0 . 40.0 32.5 17.5 27.5 dBm
IP3 REFERENCED TO OUTPUT 29.0 . 29.0 29.0 27.0 . . 27.5 22.0 27.5 dBm
NOISE FIGURE: 2.5 dB 12.7 dB 29.2 dB 13.2 dB 19.5 dB
LIMITER
LNA
BPF 1
HMR-10503
MIXER
HMR-10503
BPF 2
IF AMP 20 dB
HMR-10503
MIXER
POST AMP
HMR-10503
LO1
LO2

Figure 8. Downconverter Block Diagram

In this example, the input frequency is assumed to be 3.0 GHz, the intermediate frequency is 800 MHz, and the output frequency less than 150 MHz. This example converter has a reasonable frequency plan for minimising spurious response from the mixer products. A dual conversion approach may not represent an optimum system, but does serve to illustrate the basic elements that affect system performance.

The input limiter is typically a PIN diode assembly for input protection and low insertion loss, normally a coaxial component or a substrate assembly inside the converter module. Since the insertion loss of this device degrades the system noise figure, it is important that it is appropriately specified and designed. For this example, a 0.5 dB insertion loss is assumed.

The low noise amplifier (LNA) defines the sensitivity of the receiver subsystem and therefore its specifications are key. In the typical converter, the output power capability of the first stages of amplification has little impact on system dynamic range due to the relatively low gain. A 2.0 dB noise figure in a module having 18 dB of gain is achievable at 3.0 GHz. Intermodulation performance is not a critical specification for the first stage.

The band pass filter (BPF1) defines the input bandwidth of the receiver and eliminates the "image band" for the subsequent mixer operation. Rejection of this undesired sideband is a strong contributor to the sensitivity of the receiver. Interference signals collected by the antenna in this undesired sideband must be rejected, or they become noise and distortion on the signals of interest. The modest gain levels, before the first mixer, afforded by distributed gain keeps the level of the image band signals low. Therefore the rejection requirements for the filter are minimized, saving overall subsystem volume (size) and cost. A relatively simple microstrip structure with 2.0 dB of loss would usually be adequate.

Between the filter and mixer, utility gain in the form of an HMR-10503 is inserted. The gain and intermodulation performance of this IC complement the use of a low cost mixer and the insertion losses of the mixer are overcome by the gain of the HMR-10503. The reverse isolation of the amplifier limits the undesired LO leakage of the mixer. The specified performance of most mixers is with a condition of all ports terminated in broadband 50 ohm loads. Reactive termination of the inputs or the output with a reactive load such as a filter, can frequently lead to insertion loss ripple and worsened intermodulation distortion. The low VSWR of the amplifier output properly terminates the

input of the mixer to minimise spurious performance. This amplifier would be biased at the 25% Idss level. At this bias level the HMR-10503 would have 12.0 dB of gain with typically 6.0 db noise figure.

A mixer is specified to minimize insertion loss and spurious responses. Spurious response is usually a function of the intercept point of the mixer, which is a strong function of the LO drive capability. In addition, the termination of the LO port in particular, and the RF and IF ports in general, affect the level of spurious mixing products. For reasonably broadband signals, optimization of the termination with reactive elements for all the spurious signals is extremely difficult. In addition, most mixers are specified for 50 ohm terminations over a limited LO "drive" range. This might be 3 to 8 dB around a required LO drive level of +7 to +10 dBm. An isolator would furnish the appropriate termination and isolation. The use of a buffer amplifier in gain compression, such as the HMR-10503, on the LO port also results in predictable spurious response while providing increased and stable power level to the mixer. A relatively simple low cost mixer is assumed in the block diagram analysis. Such a mixer would likely have 7.0 dB insertion loss with a +17.0 dBm third order intercept point, referenced to its input.

On the output of the mixer would be a buffer amplifier to terminate the mixer IF port and also to furnish isolation from spurious signals from the second conversion stages of the converter. This amplifier also furnishes a stable termination for the bandpass filter (BPF2) assuring minimal VSWR induced ripple in the insertion loss. This amplifier would also be biased at 25% Idss. Since the third order intercept point of the HMR-10503 is greater than +20.0 dbm referenced to the output at the IF band, the intermodulation performance is sufficient as to not degrade the subsystem dynamic range.

The second Bandpass filter (BPF2) effectively determines the converter bandwidth. This filter is typically as narrow as the desired signal bandwidth will allow. Since insertion loss is a function of bandwidth, this filter specification would have higher loss than the "frontend filter" BPF1. The out-of-band rejection is set by the need of reverse isolation. Since the HMR-10503s in the IF path each furnish 30 dB of reverse isolation, the bandwidth and number of "poles" for this filter may be reduced. A loss of 5.0 db could be expected from this filter using low-cost implementation technology.

Many converters require that gain variation over temperature be minimized. To correct for the gain variations, temperature compensation circuits are used. Usually these are included in the First IF section between the IF filter BPF2 and the second mixer. PIN Diode networks or attenuators comprised of FET "Tee" or "PI" circuits with silicon opamps for drivers are typically used. The insertion loss of this function is dependent on the amount of gain control required. For this example a nominal loss of 8.0 dB is assummed.

The input to the second mixer is buffered for the same reasons as the first mixer. The needs for good termination and isolation on the input port of the mixer is mandatory for predictible performance. Additional specification constraints on

thia amplifier are associated with output power level as it relates to intermodulation distortion. In this typical system, an HMR-10503 is used with either one or both stages biased at 50% Idss of the RF transistors as described earlier. Its greater than +22.5 dBm third order intercept point is adequate to avoid degradation of the subsystem intermodulation performance. Gain would typically be +13 dB for this stage at the 50% Idss bias point.

The final mixer down-converts the first IF for distribution in the receiver subsystem. Again the performance of the sixer is dependant on the VSWR of the loads terminating the RF, LO, and IF porta. The use of utility gain blocks also satisfies the subsystem needs for thia second mixer. A low coat mixer is assumed for this function. The +17 dBm third order intercept point of such a mixer is the subsystem limiting intermodulation distortion contribution. The use of a higher performance mixer would enhance subsystem performance. The HMR-10503 used as a LO buffer would furnish adequate power drive for a higher dynamic range mixer.

The post amplifier function isolates the mixer output from the converter output and eatablishes the output VSWR. The dynamic range specification requirements for this block are the most stringent of any of the circuits in the converter. A well designed, high intercept point amplifier is needed. This example assumes an amplifier with 12 dB of gain and a noise figure of 8.0 dB.

The example demonstrates the use of distributed gain in nominal 12 dB increments to facilitate the design of RF converters. The analysis contained on the block diagram, shows that utility gain blocks, and other RF functions of nominal performance, can result in reasonable overall performance of the subsystem. Each subsystem function, whether it be a filter or mixer, benefits from reduced component performance specifications while maintaining dynamic range. Repeatibllity, consistency and compliance to design are more easily achieved with the use of distributed gain ICs and their controlled, predictable interfaces with the other subsystem functions.

The introduction of Harris Microwave Semiconductor's HMR-Series of RF IC products offers subsystem designers a unique opportunity for high performance frequency converters. Key attributes offered by amplifier stages, distributed through s subsystem design, can now affordably be inaerted into communication, EW and radar systems supplying more functions in smaller packages at lower cost. The promise of more highly integrated RF IC-based subsystems can now be realised.